Abstract

The distinctive switching spikes seen in single memristors are suppressed in networks of memristors. Instead oscillatory behaviour interrrupted by spontaneous irregular bursting spike patterns are seen. An investigation of two and three memrisor circuits was undertaken to elucidate the origin of these rich dynamics. No spiking is seen in circuits where all the memristors face the same way. Spiking is seen in circuits where memristors are arranged anti-parallel. These dynamics may be due to chaos and are potentially useful for neuromorphic computing.

Spontaneous Bursting Spike Patterns Seen in Simple Three Memristor Circuits

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1 Introduction

The memristor is the fourth fundamental circuit element predicted to exist from symmetry arguments in 1971[Chua 1971]. It is a two terminal and passive device. It is stateful and the internal state is related to past history of the device. Because of the memristor's ability to learn it has been proposed that the memristor would be a route to neuromorphic or brain-like hardware[HP2008]. As the achievement of this is widely anticipated to lead to a step-change in not just computing, but science and even society itself (if it works we would be able to make a true machine intelligence which could enable us to answer fascinating philosophical questions about hte nature of consciousness, intelligence and mankind).

The relation between memristors and neuromorphic computing dates back to 1976 when Chua expanded the idea of the memristor to a memristive system (two state variables rather than one) and suggested that the Hodgkin-Huxley model of hte nerve axon could be improved by in corporating memristors in place of the non-linear time dependent resistors: an idea that wasn't demonstrated until 2012[Chua2012a,b]. Meanwhile the scientific community concentrated on memristors as synapses rather than axons, simulations have shown that memristive connections could be used to reproduce spike-time dependent plasticity[ref!] (the process by which synapses adjust their connection weight to implement Hebbian learning) and even implemented as synapses in evolved spiking networks simulations[Howard]. Recently, it has been noted that both our and other groups memristors possess a current-spike reponse to a change in voltage[N0]. Thus we thought that memristors ought to be able to replicate neuronal architecture and produce dynamics associated with neurons, such as brainwaves or spike trains.

Once we stop investigating the mechanism and behaviour of single memristor circuits and start building more complex systems an area of interest is what sort of circuits have theorists and simulationists been interested in designing for memristors, and overwhelmingly simulationists have been interested in Chua circuits. The original Chua circuit[ref!] was created to demonstrate that chaos was a real phenomena and not merely due to rounding errors in the computer simulations. It is known that brain waves are chaotic in structure. Specifically, Chua's paper [2012b] suggested that neurons are poised at the edge of chaos. And thus, in trying to make neuromorphic circuits, it is worth investigating chaotic dynamics. There have been a plethora of different versions and

alterations, such as the canonocial Chua's oscillator[10years of mems?]. However, Chua's circuit is the simplest electronic circuit that can exhibit chaotic behaviour [Chua and itoh[Maclan 1993]]. This circuit consists of 1 inductor, 1 resistor, 2 capacitors and a component called Chua's diode which is a nonlinear circuit element usually fabricated from several other circuit components including op amps.

Chua and Itoh were the first to replace Chua's diode with a memristor; they worked on the concept of an active memristor. A memristor is a passive device, but a circuit of a negative resistance and memristor can be viewed as an active memristor. This is because the negative resistance is an op-amp powered by a battery and it is the battery that adds energy to the circuit. By replacing Chua's diode with an flux-controlled active memristor they made a series of chaotic oscillator circuits.

There have been many papers since detailing the rich behaviour and chaotic properties of Chua circuits containing memristors (eg. [**?**], [**?**], [**?**], [**?**]] but the simulations all used either Chua's equations for the perfect theoretical memristor and the electronic experiments replaced the memristor with a circuit equivalent, presumably due to the difficulty in obtaining an actual memristor to use. A step forward in the direction of real world functionality was Buscarino's paper [**?**]] where Chua's diode in Chua's circuit was replaced with a pair of memristors modelled using Strukov et al's phenomenological model[!!!] which is based on real world measureables. The resulting simulation demonstrated chaotic behaviour. This paper used a pair of Strukov memristors connected in anti-parallel to give a symmetrical I-V curve as a replacement for Chua's diode. They then used a voltage frequency that put the memristor up to its limits ot introduce assymetry and richer behaviour. Thus questions could be asked as to whether the chaotic behaviour they observed in their similations arose from the memristors or from the interaction of the errors in the model (which even with windowing functions is weakest at the edges of the memristor) between two anti-parallel memristors. Despite this, paper [**?**] represents and important step towards modelling real world memristor systems. Another area of interest in this feild is how few components a chaotic circuit can be made with. A recent paper suggested that the simplest circuit capable of producing chaos could be made with three components: a capacitor, an inductor and a memristor [**?**]. HP have created a neuristor, which is circuit of two memrstors and two capacitors (and a load resistor) which they stated gave 'brainwave'-like dynamics from a constant voltage source. This circuit also had the memristors in anti-parallel.

Thus, circuits involving memristors, capacitors and inductors look likely to product interesting dynamics. According to Chua[ref?] the linear combination of memristors in a circuit with only one input and one output to that circuit is indistinguishable from memristor, i.e. the memristors add up in series and in parallel similarly to resistors, which would suggest that a circuit made up of only memristors would be a trivial and boring circuit.

As the brain lacks inductors [Chua2012a], if we're trying to create neuromorphic circuits by copying neuronal architecture, that leaves only capacitors and memristors out of the fundamental circuit elements. From behaviour observed in our lab[n0] we decided to test combinations of memristors in circuits as we expected this might give rise to rich enough behaviour that we wouldn't need further complications of adding in capacitors or op amps.

In this paper we are interested in a neuromorphic computing and possible

apperance of chaotic behaviour. Therefore we shall do a study on the effects of interacting memristors using real world memristors. Our memristors are titanium dioxide sol-gel memristors based on [G-H] as described in [M1,nature conf abstract]. By using real world memristors we are able to make use to the memristor's actual behaviour, whereas theoretical models of the memristor are less useful in this regard as the utilisational behaviour can be abstracted out or the utility may arise from erroneous theoretical assumptions rather than memristors true behaviour.

We shall investigate how pairs of memristors interact and test Chua's asertion that 2 mems in series (or parallel) addressed only by their joint one port entry (ie there is one wire coming out and going in to that part of the circuit) are indistinguishable from form a single memristor with a memristance value calculable by standard series and parallel resistor adding rules. We will look at the three combination 3 memristor circuits.

2 Methodology

All experiments were performed with a Kiethley 2400 Sourcemeter. For the I-t curves, the memristor circuits were taken to +0.4V for [x] timesteps, the voltage source was then switched the 0V and data gathered for a further [y] seconds. For some tests -0.4V or +0.8V was used instead. For the slow I-V test, a sinusoidal voltage of [z]timesteps, with a frequency was used to see how the system would response to a slow change. Voltages were kept very low to avoid the creation of filaments via Joule heating which would lead to filamentary memristors switching into lower resistance states.

3 Single Memristors

The D.C. response of a typical memristor is given in figure **??**. For this experiment the memristor was taken to the test voltage at 0 seconds and the current recorded as the memristor 'equilibrated'. This was done for two voltages, +1V and -1V.

When voltage is changed we expect a current spike, as this has been seen in all our tests [**?**] and this the D.C. action of memristors [forthcoming paper]. For the long time experiments shown later in this paper, the single memristor response is shown in figure []. The spike from the original voltage switch occurs at the start, and then negative spike at []s that results from the change from +0.4V→0V can be clearly seen.

4 Memristor Circuits

According to [Poincare] 3 [state/phase] variables are needed for chaos, so we chose to create a circuit with three memristors, which gives us the following three separate state variables, the current through the circuit, and the voltage across two of the memristors (the third being determined by the other two in a system kept at a constant voltage). In order to maximise the compositional complexity of the circuit, the memristors were wired up, two in series in reversed order, with one in parallel to the two in series as shown in figure[!!!]. This gives us a circuit

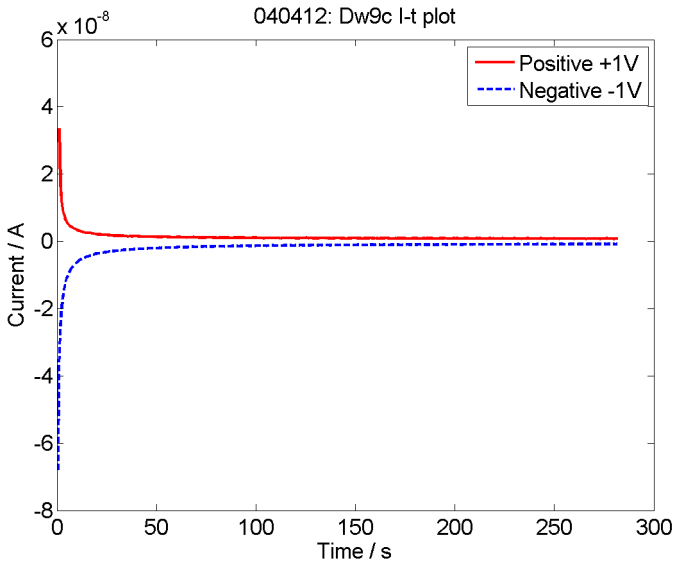

Figure 1: Memristor reponse under both positive and negative voltages. The voltage is switched on at 0 seconds, causing the current spike, which then equilibrates. The voltages are +1V and -1V.

with two anti-parallel interactions. It was thought that the memristors would spike with the change of voltage and this would cause a change in resistance within a single memristor, which, with this circuit set-up would lead to a voltage change across the other memristors and thus further spikes.

Typical results for this circuit are given in figure **??**. Comparing this with the expected curve in for one memristor, shows quite a few differences. The large spike at the start has vanished, as has the one at the end. We see oscillations in the base line, with spontaneous spiking overlaid over the top. Figure **??** shows a later run where we see sections of oscillations of different frequency. Several runs of this circuit were done to see if there was a repetition in the spiking pattern and thus if the circuits were following an long-term periodic dynamics, this was not the case.

Attempts to effect this osciallation by running a very slow I-v curve is shown in figure **??**. This does not show the expected response for a single memristor[picture!], or any change in the 'baseline' as a result of the voltage variance. The expected spikes from the one memristor circuit have been surpressed or delayed.

5 Two Memristor Circuits

To try and understand this, the two memristor circuits shown in figure[!!!] were made. Figures **??** amd **??** show that two memristor circuits are capable of producing similar behaviour.

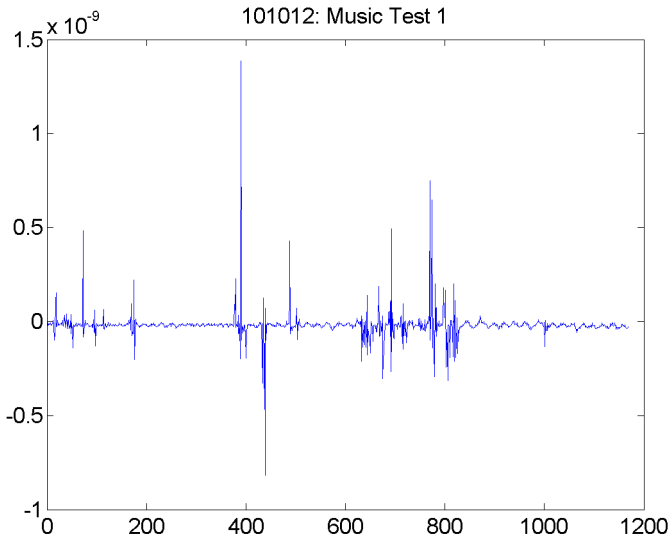

Figure 2: The current response for our first three memristor circuit. There seems to be an oscialltory behaviour as well as periods of spiking that resembles spike-trains in neural networks.

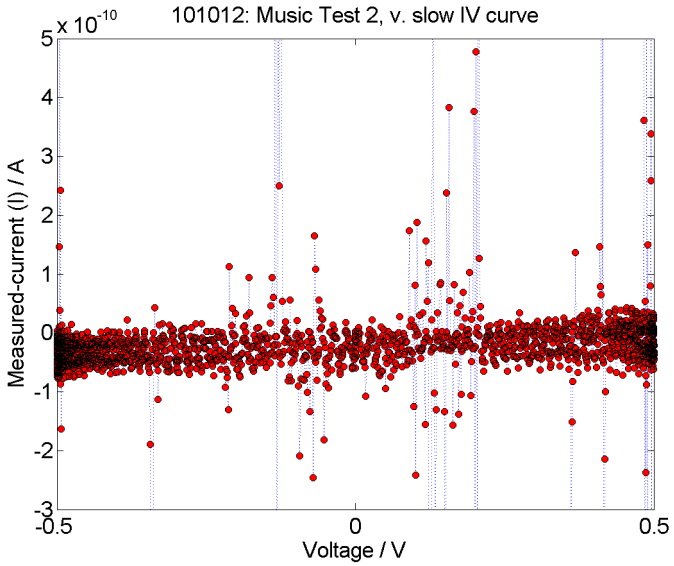

Figure 3: An I-t curve for a very slow sinusoidally varying voltage.

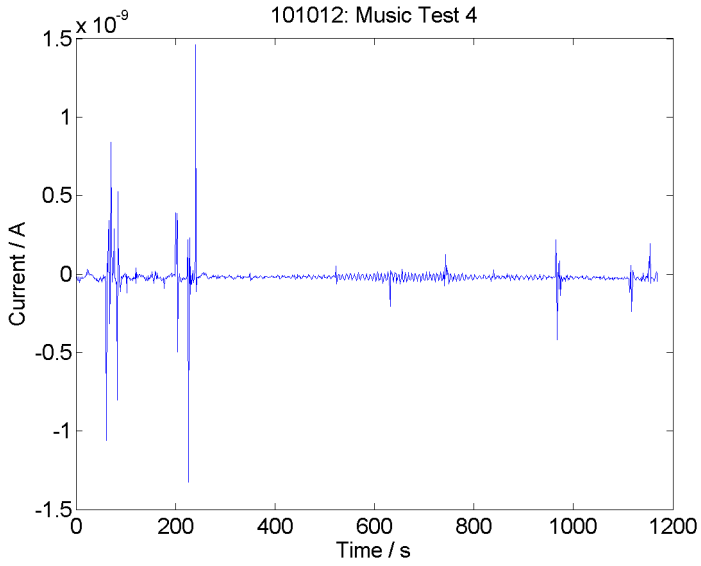

Figure 4: Another typical I-t profile for the circuit shown in figure[!!!].

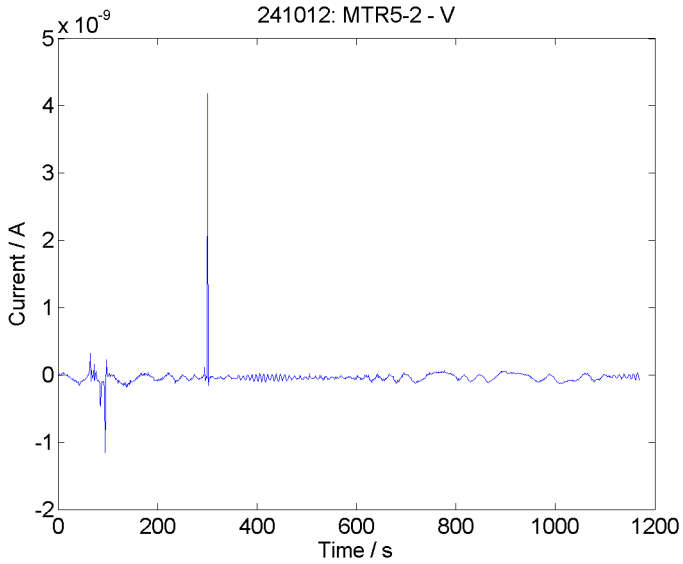

Figure 5: Two R-series memristors in parallel.

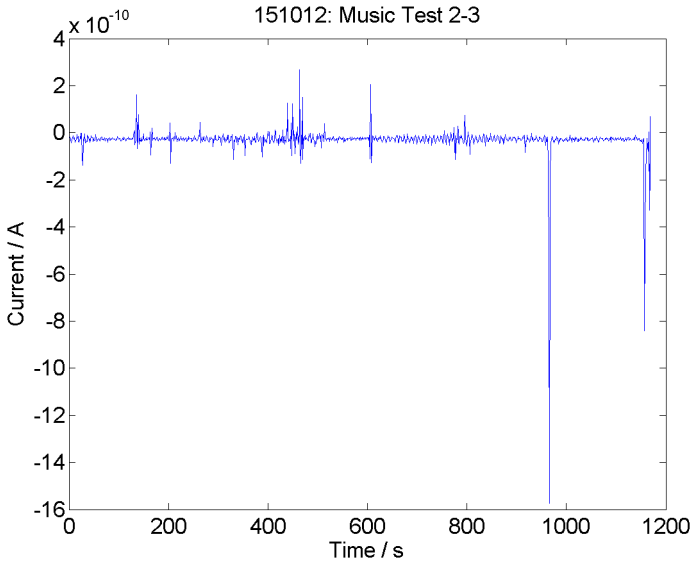

Figure 6: Two R-series memristors in a series circuit wired up with opposite polarity.

6 Memristor circuit rules - using D series.

Does this mean that memristors do not add up as expected? Not necessarily. Using which are closer to the theoretical perfect Chua memrsitors (type A from paper [M1]), we see that three mems in a circuit behave qualitatively just like one mem, see figure **??**. These three particular memristors were picked out of hte batch as they have very similar I-V curve responses. Figure **??** shows the same memristors with the mem in series faceing the other direction. This figure shows some tantalising hints of small scale, longer terms switching.

However, the same memristors, wired in parallel with the same polarity and series, different directions, as shown in figure **??** and **??** show behaviour similar to the three memristor circuit above.

7 Discussion

We have shown that three memristors can produce rich behaviour, inclusing brain-wave like oscillations and spiking events. An interesting question is where has the large spike at the start gone and hwere have the spikes expected from the I-V curve gone to. We beleive that the energy of the current spike, in fact the current itself, has been 'absorbed' into hte memristor network and is the cause of hte latter spiking events.

We have shown that for two or three memristors that are very similar to each other and wired up with the same polarity, Chua's prediction that they would behave exactly like a single memristor is true. We have also shown that when there is either parallel interaction or a polarity difference between the memristors, there is a higher chance of richer behaviour. From these circuits

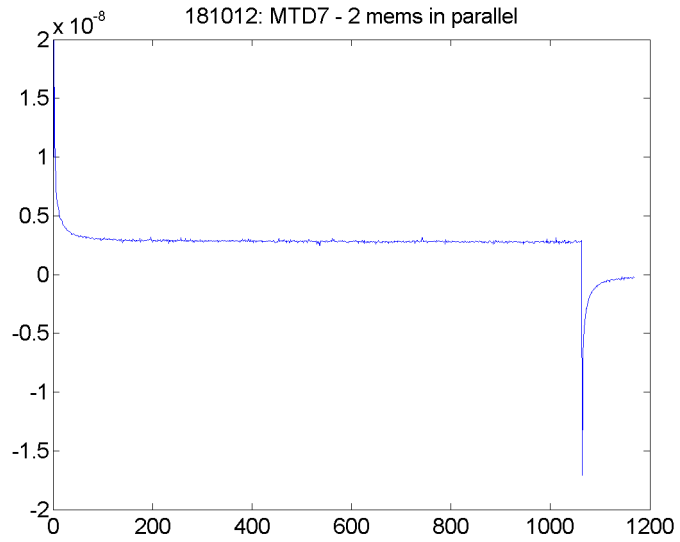

Figure 7: Three memristors set up as for figure [] except that all the memristors are wired up the same way round. This shows that without the anti-parallel wiring, the memristors do not interact.

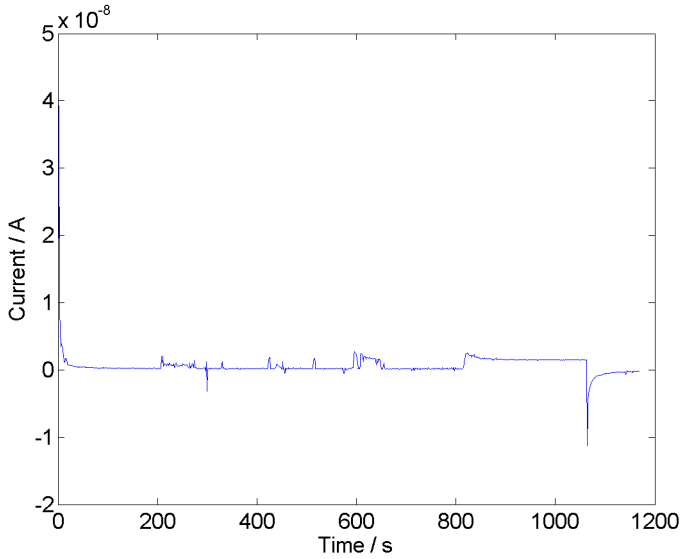

Figure 8: Two mems in series wired up opposite direction to the one in parallel.

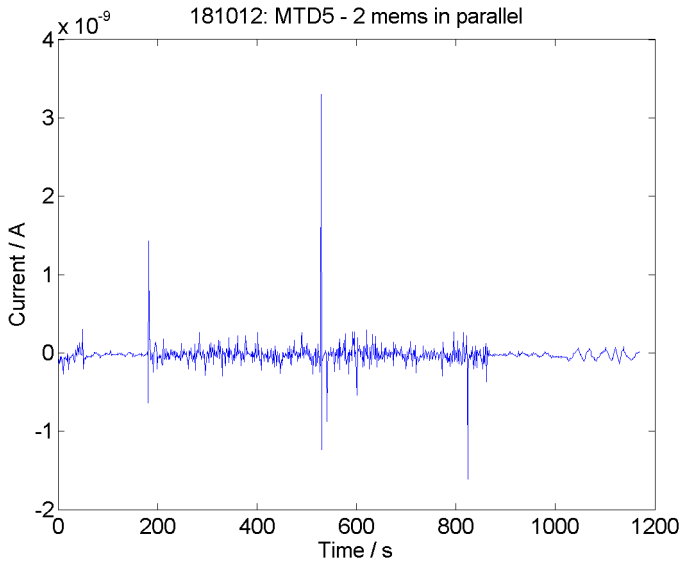

Figure 9: Two D-series mems in parallel, same direciton

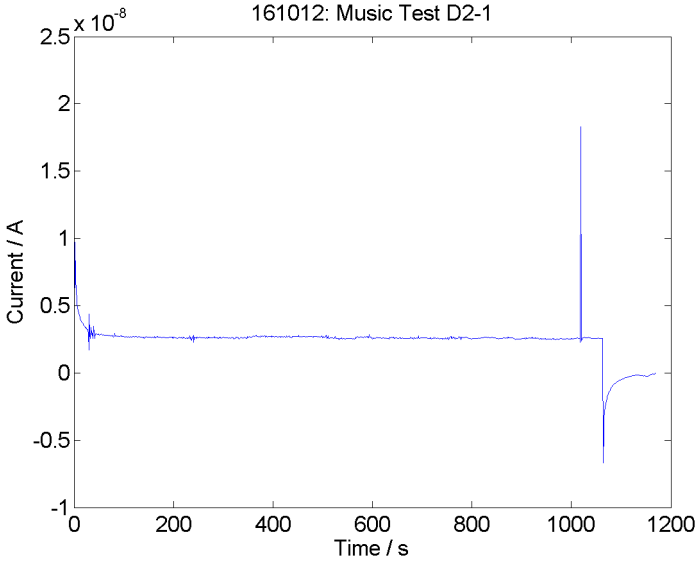

Figure 10: Two D-series mems in series, opp direciton

it is apparent that the circuit fragment of two memristors in antiparallel (i.e. in parallel with opposite polarity) has the highest chance of neuromorphic-like rich dynamics. This is supported by the results reported in the literature.

The background oscillations are interesting. Although they could be dismissed as sampling noise or background noise, we do not beleive this to be the case as they are not seen in the single memristor circuit. They could be some low level emergent phenomena related to the spikes. Instead, we think it's to do with the movement of the boundary, $w(t)$. These oscialltions appear similar to oscillators interacting, and thus we think its possibly related to the boundary which may be osciallating due to the movement of ions around the equilibrium point, and it is this oscialltion that adds up and interacts in the circuit with more than one memristor in it.

8 Further Work

This letter represents preliminary work in this area. Although the dynamics look rich, we need to do further analysis to discover whether the trajectory is chaotic. We are currently undertaking futher investigations, both experimental and theoretical, into the mechanism of this behaviour.

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