Analyses of Parasitic Capacitance Effects and Flicker Noise of the DAC Capacitor Array for High Resolution SAR ADCs

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***Abstract*—With the increasing number of bits, parasitic effects and flicker noise of switching transistors in the DAC capacitor array of the SAR ADC are getting relatively bigger when compared to the exponentially decreasing error budget. This paper analyses the effects of parasitic capacitances related to the top-plate and bottom-plate of unit capacitors on the accuracy and the noise performance of the DAC capacitor array, showing that thermal noise of the whole capacitor array decreases when parasitic capacitances are considered while in the meantime an unexpected gain error is introduced. Although the parasitic-capacitance-induced gain error is almost independent of the number of bits, parasitic effects should be minimized for high resolution SAR ADCs since the dynamic range of the high resolution ADC is severely reduced due to the gain error. The post-layout parasitic capacitance extraction of a 10-bit poly-poly DAC capacitor array shows that the value difference between the top-plate and bottom-plate related parasitic capacitances is large so that the parasitic-capacitance-induced gain error can be decreased by 152 times when top-plates of unit capacitors are connected together as the output node of the capacitor array. The switching transistor's flicker noise calculation for a 10-bit SAR ADC shows that flicker noise can be safely ignored for 10-bit 1MSPS SAR, while the calculation for an 18-bit 1MSPS SAR ADC shows that flicker noise should be considered for the higher resolution SAR ADCs.**

***Key words*—Successive approximation register (SAR) ADC, DAC capacitor array, parasitic capacitance, thermal noise, flicker noise**

I. INTRODUCTION

The successive approximation register (SAR) ADC has been reported as the lowest power consuming ADC [1] which is particularly useful in low-power, low data rate biomedical applications (such as acquisition of physiological signals of ECG, EEG [2, 3] and biometric signal of fingerprint [4], human-computer interface [5] and eye gaze tracking [6]). A typical SAR ADC is composed of four functional blocks: the sample and hold circuit which stores the sampled signal, the DAC capacitor array controlled by charging switches to generate voltage levels to be compared to the sampled signal, a comparator which performs decision-making by comparing the amplitude of the sampled signal to that of the DAC signal producing binary results, and a SAR control block to provide converting timing of reset, sample and hold, and the charging switching control for the conversion of each individual bit.

The absolute accuracy of the capacitor value in the DAC capacitor array is relatively poor in a CMOS process. Special layout techniques, such as the common centroid one [7], are commonly employed for the implementation of the binary-weighted DAC capacitor array in order to achieve the required accuracy. The accuracy parameters of the binary-weighted DAC capacitor array considered in literature are the matching error only [8] and both of the matching error and thermal noise [9], which are adequate to accuracy calculations since parasitic effects are generally relatively low. However, with the application demands for high resolution SAR ADCs, the required measurement accuracy increases exponentially (such as 0.0004% for the newly emerged 18-bit SAR ADC), raising an accuracy concern of whether current accuracy considerations, which do not include parasitic capacitances (which may reach 20% of the nominal capacitance value [10]) of the DAC capacitor array, is good enough for high resolution applications. Parasitic capacitance effects on power consumption and the linearity of the DAC capacitor array have been calculated and simulated in [11], and the work on the reduction of parasitic capacitance impact by adding more switching devices has been reported in [12] where both top-plate and bottom-plate related parasitic capacitances have been involved but have not been treated differently. With the consideration of different roles of the top-plate and bottom-plate related parasitic capacitances, a simple layout solution to lower parasitic effects is reported in this paper. Moreover, as the measurement accuracy increases, there is another concern of whether flicker noise produced by switching transistors in the DAC capacitor array is small enough to be neglected in the high resolution SAR ADC design, because flicker noise of switching transistors in charging branches increases as a result of the increasing bandwidth of the SAR ADCs when the number of bits increased [13].

This paper analyses different types of parasitic effects on the DAC capacitor array, and then presents an example layout of the poly-poly DAC capacitor array to demonstrate that the parasitic-capacitance-induced gain error of the SAR ADC could be largely decreased. The bandwidth of the SAR ADC is estimated to

evaluate the general figure of flicker noise, showing that for a high resolution SAR ADC design flicker noise of switching transistors should not be ignored.

II. PARASITIC CAPACITANCE EFFECTS

2.1 The roles of the parasitic capacitances

The block diagram of the SAR ADC is shown in Fig.1a. Analog input signal is sampled by a sample clock and this sampled value (V_{in}) is hold within the sample clock period to successively produce the digital output of D_{N-1}, D_N…D_0 at the data converting clock (CLK) which is the sample clock divided by N+1 (there is an extra clock for reset). The DAC array is controlled by SAR to produce a comparison voltage to the sampled value V_{in}. To convert bit i, the bit i in SAR is set as 1, resulting a DAC voltage output of $v(i) = \frac{V_{ref}}{2^{N-i}} + \sum_{k=i+1}^{N-1} D_k \frac{V_{ref}}{2^{N-i}}$ (where the first term of $\frac{V_{ref}}{2^{N-i}}$ is the voltage weight for the i^{th} bit and the second term is the voltage contribution from already converted bits of D_{N-1}, $D_{N....}$ D_{i+1}). When $V_{in} > V(i)$, $D_i = 1$ otherwise $D_i = 0$.

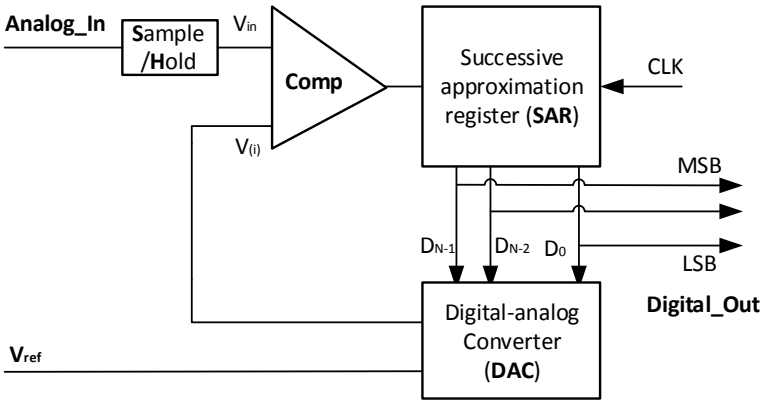
The typical N-bit DAC circuit of the binary-weighted capacitor array of the SAR ADCs is shown in Fig. 1b, where N charging branches with capacitances of C, 2C, 4C …… $2^{N-1}C$ are connected to the charging switch (implemented by the switching transistor) corresponding to their own branch, and one branch with the capacitance of C but without the charging switch. The branch with the charging capacitor of $2^{N-1}C$ corresponds to the most significant bit (MSB) and the branch with the charging capacitor C corresponds to the least significant bit (LSB). The error budget for an N-bit ADC is +/- ½LSB which equals +/- $V_{ref}/2^{N+1}$, so the error budget of the SAR ADC decreases exponentially with N.

In a CMOS process the DAC capacitor array is usually implemented by means of poly-poly structures due to their accuracy and stability [10]. However, a parasitic capacitance exists between the bottom-plate of the capacitor and the substrate due to imperfect shielding. Similarly there exists a parasitic capacitance relevant to the top-plate of the capacitor and the substrate which is usually connected to ground. These parasitic capacitances vary with the fabrication process, affecting the accuracy of the SAR ADCs. The inaccuracy caused by parasitic capacitances can be neglected in low resolution applications but it might be relatively bigger when compared to the available error budget for high resolution applications. Assuming that the output of the capacitor array shown in Fig. 1b is connected to the same plate of the poly-poly unit capacitors, the capacitor array circuit including parasitic capacitances is shown in Fig. 1c where C_{p1} denotes the parasitic capacitance seen from the output node of the capacitor array while C_{p2} denotes the parasitic capacitance related to another plate of the charging capacitor.

The parasitic capacitance C_{p1} of each charging capacitor are in parallel forming an equivalent parasitic capacitance of $\sum C_{p1}$ which is in parallel to the capacitor C in the branch without the charging switch,

introducing a gain error by changing the voltage division ratio in the capacitor array. For the M[th] charging branch, the gain error introduced by C_{p1} can be calculated as:

$$G\_Error_{\_C_{p1}} = \frac{2^M C}{2^N C} - \frac{2^M C}{2^N C + \sum C_{p1}} = \frac{2^M}{2^N} \times \frac{\sum C_{p1}}{2^N C + \sum C_{p1}} \qquad (1)$$



(a)

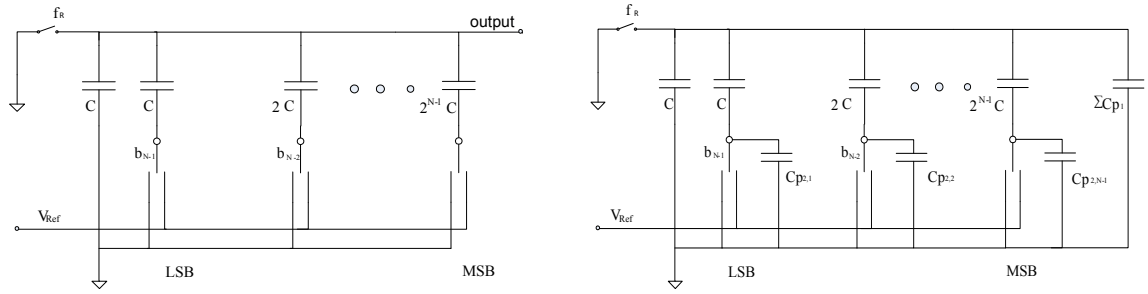


Fig. 1 (a). Block diagram of the SAR ADC. **Fig. 1(b).** A binary-weighted DAC capacitor array which has N changing branches with the capacitance of C, 2C……, 2^{N-1}C, and each charging switch is implemented by a switching transistor, switch f_R is for reset. **Fig. 1(c).** DAC capacitor array circuit modified by the inclusion of parasitic capacitances

The first term $\frac{2^M}{2^N}$ in relation (1) corresponds to the ideal voltage division ratio for the M[th] branch, while the second term $\frac{\sum C_{p1}}{2^N C + \sum C_{p1}}$ corresponds to the gain error introduced by the parasitic capacitances $\sum C_{p1}$. The total error of the DAC capacitor array contributed by the parasitic capacitances $\sum C_{p1}$ can be calculated as,

$$G\_Error_p = \sum_{M=0}^{N-1} \frac{2^M}{2^N} \times \frac{\sum C_{p1}}{2^N C + \sum C_{p1}} = \frac{2^N - 1}{2^N} \times \frac{\sum C_{p1}}{2^N C + \sum C_{p1}} \qquad (2)$$

Relation (2) indicates that the role of the parasitic capacitor C_{p1} in the capacitor array is to introduce an unexpected gain error of $\frac{\sum C_{p1}}{2^N C + \sum C_{p1}}$ ($the\ term\ \frac{2^N - 1}{2^N} \rightarrow 1$ when N is big), affecting the accuracy of the capacitor array.

Parasitic capacitance from a given plate of the capacitor can be roughly estimated by the nominal capacitor value and its parasitic factor α which is a constant determined by the fabrication technology. Therefore for a given fabrication process the parasitic-capacitance-induced gain error can be estimated as

$$\frac{\sum C_{p1}}{2^N C + \sum C_{p1}} = \frac{\alpha \times 2^N C}{2^N C + \alpha \times 2^N C} = \frac{\alpha}{1+\alpha} \quad (3)$$

Since parasitic factor α can be as big as 0.2 [14, 15], the worst case gain error introduced by C_{p1} can be estimated as high as 16.6% which is too large to be ignored even compared to the 0.1% accuracy requirement for a 10-bit SAR ADC, and therefore parasitic effects of the gain error should not be ignored for high resolution SAR ADCs.

Although relations (2) and (3) show that the gain error introduced by the parasitic capacitor is almost independent of the number of bits, when the number of bits increases the dynamic range of the SAR ADC reduces severely due to the gain error. In practice, the gain error of the SAR ADC can be calibrated in post-processing, but the reduced input dynamic range which affects the signal to noise ratio (SNR) of the ADC could not be compensated in post-processing and therefore parasitic effects from C_{p1} should be minimized for high resolution applications.

Unlike C_{p1}, the C_{p2} of each individual charging branch (denoted as $C_{p2,m}$ for the Mth branch in Fig. 1(c)) acting as a low-pass filter in the charging process, does not change the voltage division ratio but affects thermal noise of the capacitor array. To calculate thermal noise of the Mth charging branch, assuming that the on-resistance of the switching transistor (denoted as r in Fig. 2) is the only noise source of the capacitor array and that the other charging branches are ideal switches, the equivalent circuit for thermal noise calculation without parasitic capacitance is shown in Fig. 2a where V_R^2 denotes thermal noise of $4KTr\Delta f$ produced by the switching transistor with the on-resistance of $r = \frac{L}{\mu C_{ox} W(V_{GS}-V_T-V_{DS})}$, K denotes the Boltzmann constant of 1.38×10^{-23} JK^{-1}, T denotes the absolute temperature value, W and L denote the width and the length of the switching transistor respectively. Thermal noise of the Mth charging branch of the capacitor array without considering parasitic capacitances has been calculated as [9]

$$Err_{n\_m} = \sqrt{\frac{2^M}{2^N - 2^M}} \times \sqrt{\frac{KT}{2^N C}} \quad (4)$$

The equivalent circuit of the Mth charging branch of the DAC capacitor array including parasitic capacitances for thermal noise calculation is shown in Fig. 2b. Thermal noise of the Mth charging branch with parasitic capacitances can be calculated as:

$$Err_{n_m} = \frac{2^M C}{2^N C + \sum C_{p1}} \sqrt{\frac{KT}{\frac{2^M\left(2^N C - 2^M C + \sum C_{p1}\right)}{2^N C + \sum C_{p1}} + C_{p2,2^M}}} < \frac{2^M C}{2^N C + \sum C_{p1}} \sqrt{\frac{KT}{\frac{2^M C\left(2^N C - 2^M C + \sum C_{p1}\right)}{2^N C + \sum C_{p1}}}}$$

$$= \sqrt{\frac{2^M C}{2^N C - 2^M C + \sum C_{p1}}} \sqrt{\frac{KT}{2^N C + \sum C_{p1}}} \quad (5)$$

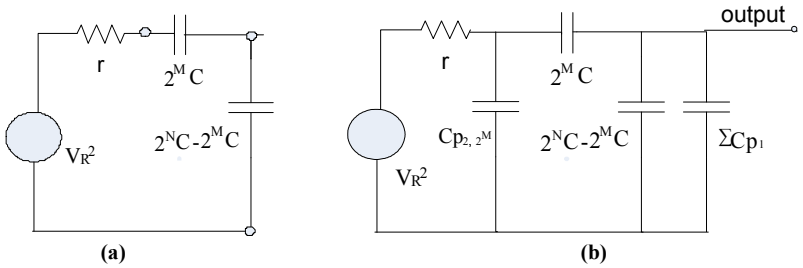


Fig. 2. The equivalent circuit of the capacitor array for thermal noise estimation. (a). Ideal circuit. (b). With parasitic capacitances

Thermal noise shown in relation (5) is smaller than that of the ideal capacitor array shown in relation (4) since

$$\sqrt{\frac{2^M C}{2^N C - 2^M C + \sum C_{p1}}}\sqrt{\frac{KT}{2^N C + \sum C_{p1}}} < \sqrt{\frac{2^M}{2^N - 2^M C}}\sqrt{\frac{KT}{2^N C}} \tag{6}$$

Therefore parasitic capacitances C_{p2} make thermal noise of the capacitor array smaller. Relation (6) also reveals that parasitic capacitance C_{p1} is involved in reducing thermal noise as well, uncovering another role C_{p1} plays in the DAC capacitor array.

It is understandable that parasitic capacitances play different roles in the DAC capacitor array. The parasitic capacitance C_{p1} enlarges the value of the total capacitance of the capacitor array and consequently it affects both of the accuracy and thermal noise performance. The enlarged total capacitance of the capacitor array not only affects the charging redistribution process resulting in a gain error, but also reduces thermal noise of the capacitor array since thermal noise of a charging capacitor is inversely proportional to the square-root of the value of the capacitor. Parasitic capacitance C_{p2} does not involved in the charging redistribution process therefore it does not directly affect the accuracy of the capacitor array. It acts as a low-pass filter to reduce thermal noise of the capacitor array by narrowing the bandwidth of each charging branch.

2.2 Layout considerations

A DAC capacitor array of a 10-bit SAR ADC under the reference voltage of 1V is designed and laid out to investigate parasitic effects. The calculated reliable minimum unit capacitance (at a confident level 0f 99.9%) for the 10-bit SAR ADC is 76.4 fF in the 0.35 μm AMS process [9], corresponding to a poly-poly capacitor with an area of 88.8 μm^2 (about 9.43 μm by 9.43 μm). A 10 μm by 10 μm poly-poly unit capacitor corresponding to 89.44 fF is chosen in this design.

Poly-poly unit capacitors with different characteristics, one with an N-well and another without the N-well, were implemented to evaluate their parasitic capacitances. The results listed in Table I show that the poly-poly capacitor with an N-well has smaller parasitic capacitances than that without. An individual N-well is also known to be less noisy than the underlying substrate. For these reasons, N-well poly-poly capacitor is chosen as the form of the unit capacitor. Also note that the terminals of each capacitor in the capacitor array's

layout are not exchangeable if parasitic capacitances are taking into account, since the parasitic capacitances existing in each plate are different. The bottom-plate related parasitic capacitance (C_{pb}) is much bigger than the top-plate related one (C_{pt}) in Table 1.

Table I. Parasitic capacitance for poly-poly capacitors

	C_{pb} (fF)	C_{pt} (fF)
Without an N-well	22.85	1.33
With an N-well	21	0.51

Two possible layouts, the compact layout where bottom-plates of unit capacitors are connected together as the output node of the capacitor array and another one where top-plates of unit capacitors are connected together, are implemented. Since the dimension of the bottom-plate of the poly-poly capacitor is larger than that of its top-plate, it is easy to directly connect bottom-plates together to form a whole plate acting as the output node of the capacitor array for a compact layout without extra clearance distance among top-plates of unit capacitors. However, relation (2) indicates that a small parasitic capacitance connecting to the output node of the capacitor array is a better way of maintaining the accuracy of the capacitor array. As shown in Table I, $C_{pb} >> C_{pt}$, it is recommended here that in the layout of the capacitor array the top-plates of unit capacitors should be connected together as the output node of the capacitor array to lower the parasitic-capacitance-induced gain error. Fig. 3 demonstrates the recommended layout for the 10-bit poly-poly DAC capacitor array where top-plates of all 2^{10} unit capacitors are connected together as the output node. Additional dummy capacitors are added around four edges of the capacitor array to improve matching as well as acting as a guard ring shielding the capacitor array from external noise. Moreover, one row and one column of dummy capacitors formed a central “cross” avoiding wires routing across the unit capacitors to prevent capacitor array from unexpected interference. The layout of the DAC capacitor array comprised 35 rows by 35 columns of unit capacitors, occupying an area of 480 μm by 480 μm which is a 23% area increase compared to the case of connecting the bottom-plates together with an area of 420 μm by 420 μm.

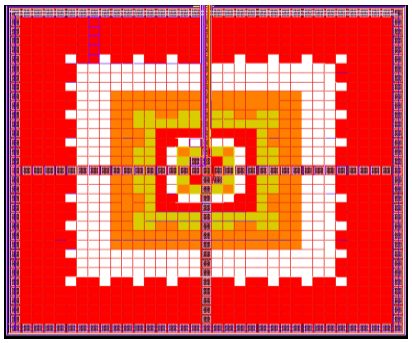


Fig.3. Recommended layout of a 10-bit binary-weighted DAC capacitor array. Top plates of the unit capacitors are connected together for minimizing the parasitic effects (different colour in the figure represents the capacitor in different charge branches from outside to the inner of the layout represent the charging capacitor values of 2^9C, 2^8C……C).

Parasitic capacitances of the capacitor array have been extracted from the layout shown in Fig. 3, which gives $\sum C_{P1}$ =112.7 fF and $\sum C_{p2}$= 20.8 pF. The detailed figures of C_{p2} in each charging branch are listed in Table II, which show a parasitic factor of 0.24 +/-10%. According to relation (2), a total C_{p1} value of 112.7fF will introduce a gain error of 0.00122 and a full scale error of 1.25 LSB when the layout shown in Fig. 3 is adopted. If without considering the effects of parasitic capacitances prior to the layout, the area efficient compact layout of connecting bottom-plates of unit capacitors together as the output node of the capacitor array would probably be adopted. This would bring a large gain error of 0.185 and a full scale error of 190 LSB, which is 152 times bigger than that of the recommended layout.

Table II. Extracted parasitic capacitances of C_{p2}

Nominal	Parasitic	Nominal	Parasitic
C	23.7 fF	32C	640.2 fF
2C	44.4 fF	64C	1.27 pF
4C	85.7 fF	128C	2.55 pF
8C	167.1 fF	256C	5.09 pF
16C	324.3 fF	512C	10.18 pF

Post-layout simulations for the effects of the parasitic capacitances on different layouts are summarized in Table III, which demonstrate that the recommended layout has much lower parasitic effects on gain error and consequently on the gain-error-induced effects on dynamic range and SNR, although the compact layout promises more thermal noise improvement. There are two reasons to support the recommended layout. The first one is that thermal noise of the capacitor array has been restricted within the acceptable level in the design process [9], so the improvement in thermal noise is not necessary while parasitic-capacitance-induced gain error is the extra error source which directly affects the accuracy of the capacitor array and therefore it should be minimized. Secondly, researches have shown that the matching error is the dominant error in the SAR ADC [8, 9]. The parasitic-capacitance-induced gain error is similar to the matching error in the capacitor array therefore a higher priority should be granted to reduce the gain error rather than to improve the thermal noise performance.

Table III. Parasitic effects on different layouts of a 10-bit DAC capacitor array

	Top-plates connected	Bottom-plates connected
Thermal noise improvement	0.06%	11.3%
Gain error	0.12%	18.5%
Dynamic range	0-1021 LSB	0-871 LSB
SNR reduction	0.02 dB	1.72 dB

It is worth noting that the gain error in the recommended layout can be further reduced. The extracted parasitic capacitance C_{p1} from the recommended layout is 112.7 fF, which is slightly bigger than the unit capacitor of 89.44 fF in this design. If the branch containing the unit capacitor without a charging switch is disconnected

in the layout of the capacitor array, the equivalent parasitic capacitance for C_{p1} will become 112.7-89.44 = 23.26 fF. The gain error induced by the equivalent parasitic capacitance will be reduced to 0.025%, which is about 5 times less than the figure shown in Table III and the dynamic range reduction can also be further reduced from 1.25 LSB to 0.25 LSB.

III. FLICKER NOISE ANALYSIS

3.1. Flicker noise

As mentioned previously, the on-resistance of the switching transistor employed in the DAC capacitor array is the source of the thermal noise of the capacitor array. The switching transistor also produces flicker noise which can be generally expressed as [15]:

$$V_n^{\,2} = \frac{K_n}{fC_{ox}WL}\Delta f \tag{7}$$

where K_n is a manufacturing process-dependent constant in the order of 10^{-25} V^2F, and C_{ox} is in the order of 10^{-15} F/μm^2. Flicker noise voltage within a bandwidth ranging from low cutoff frequency f_L to high cutoff frequency f_H can be calculated as:

$$V_n = \sqrt{\int_{f_L}^{f_H} \frac{K_n}{fC_{ox}WL} df} = \sqrt{\frac{K_n}{C_{ox}WL}\ln(\frac{f_H}{f_L})} \tag{8}$$

3.2. Bandwidth estimation and flicker noise calculation

Ideally, the output voltage of the DAC capacitor array for a SAR ADC is a multi-level signal which is a linear combination of the output voltages from each of the N charging branches within each sampling period. Let the sample and hold frequency be f_s, and the output voltage of the Mth branch denoted as V_{out_m} be a pulse of variable duration. The duration (τ) of the pulse is either 1/(N+1) or (N-M+1)/(N+1) times 1/f_s depending on the intermediate ADC conversion result ADC_{out_m}. The output voltage of the capacitor array at the end of converting a sampled signal can be expressed as:

$$V_{out} = \sum_{m=0}^{N-1} V_{out\_m}$$

$$V_{out\_m} = \begin{cases} 0, & 0 \le \mathrm{t} < \dfrac{M+1}{(N+1)f_s} \\ \dfrac{2^M}{2^N}V_{ref}, & \dfrac{M+1}{(N+1)f_s} \le \mathrm{t} < \tau \end{cases}$$

$$where \quad \tau = \begin{cases} \dfrac{M+1}{(N+1)f_s}, & ADC_{out\_m} = 0 \\ \dfrac{1}{f_s}, & ADC_{out\_m} = 1 \end{cases} \tag{9}$$

The square pulse waveform

$$S(t) = \begin{cases} 1, -\dfrac{1}{2} \le t \le \dfrac{1}{2} \\ 0, \ others \end{cases}$$

Can be expressed as the following Fourier series,

$$S(t) = \frac{1}{2} + \frac{2}{\pi}\left(\cos \pi t - \frac{1}{3} cos\ 3\pi t + \frac{1}{5} cos\ 5\pi t - \cdots\right) = \frac{1}{2} + \frac{2}{\pi}\sum_{r=1}^{\infty} \frac{(-1)^r \cos[(2r-1)\pi t]}{2r-1} \tag{10}$$

Relation (10) shows that a pulse is composed of its fundamental frequency, with odd harmonics each contributing $\frac{\pm 2}{(2r-1)\pi}$ to the amplitude of the waveform. To achieve the charging amplitude accuracy of +/- ½LSB for an N-bit DAC, the highest harmonic should be at least equal to:

$$\frac{2}{(2r-1)\pi} \frac{2^m}{2^N} V_{ref} \le \frac{V_{ref}}{2^{N+1}} \frac{2^m}{2^N} V_{ref} \Rightarrow (2r-1) \ge \frac{2^{N+2}}{\pi V_{ref}} \tag{11}$$

This indicates that in order to achieve a less than +/- ½ LSB error in DAC output amplitude, the highest harmonic (2r-1) should be at least equals $\frac{2^{N+2}}{\pi V_{ref}}$. Given that the highest frequency varies as $(N+1)f_s$ (N bits plus a sample and hold time slot) in a SAR ADC, the required bandwidth of the capacitor array should be at least,

$$B = \frac{2^{N+2}}{\pi V_{ref}} (N+1) f_s \tag{12}$$

As an example, a bandwidth of 14.3GHz is calculated from relation (12) for a 10-bit capacitor array working at a sampling rate of 1 MKSPS, which is challenging to understand the resulting high bandwidth. However, since the output V_{out_m} for SAR ADCs does not need to be a perfect square pulse, relation (12) almost certainly overestimates the required bandwidth.

An alternative way to estimate the required bandwidth for a DAC capacitor array is possible by means of charging analysis. Considering the capacitor array as a charging "black-box", its step response can be expressed as:

$$V_0 = V_i(1 - e^{-\frac{t}{RC_t}}) \tag{13}$$

where R and C_t are the equivalent charging resistor and the equivalent total charging capacitor so the bandwidth of the charging network is determined by: $f = \frac{1}{2\pi RC_t}$.

For an N-bit DAC array, the charging time to achieve the charging accuracy of +/- (½) LSB can be calculated from (13) as:

$$e^{-\frac{t}{RC_t}} = \frac{V_i - V_0}{V_i} \leq \frac{\frac{1}{2^{N+1}}V_i}{V_i} = \frac{1}{2^{N+1}}$$
$$t \geq (N+1)ln2 \times RC_t = (N+1)ln2 \times \frac{1}{2\pi f} \quad (14)$$

Relation (14) reveals the relationship between the time taken to achieve the charging accuracy of +/-(1/2)LSB and the required bandwidth of the charging network, providing an alternative way to determine the required bandwidth for a given charging time. In the case of charging the DAC capacitor array of an SAR ADC, the charging time is limited to $\frac{1}{(N+1)f_s}$ for each bit. Thus the minimum bandwidth required can be calculated from relation (14) as:

$$f \geq \frac{1}{2\pi}(N+1)^2 \times ln2 \times f_s \quad (15)$$

However, the equality in relation (15) applies only when the output waveform has an error of +/-(1/2)LSB at the end of the charging process. This is clearly not appropriate for an SAR ADC in which a precise voltage level should be established much earlier in order to have enough time to implement the subsequent comparison and decision-making. Therefore the bandwidth of the capacitor array should be larger than the minimum bandwidth determined by relation (15). To establish a precise output value within just 10% of the available charging time, the bandwidth of the capacitor array must be at least 10 fold the minimum bandwidth determined by relation (15).

The required bandwidth calculated from relation (15) for the 10-bit, 1 MSPS DAC capacitor array is 13.3 MHz. This should be increased 10 fold to f_H = 133 MHz to allow the establishment of a steady-state voltage early enough in the ADC cycle. The low cutoff frequency f_L in (8) can be chosen lower than the $1/t_{on}$ [16] where t_{on} is the on-time of the switching transistor, so 100 KHz has been chosen as the f_L since the maximum on-time for converting a sampled signal is $\frac{N}{(N+1)f_s}$. If a switching transistor with the area of 100 μm^2 is employed, the flicker noise of the switching transistor for the 10-bit SAR ADC can be estimated as 2.68μV (RMS). Given that the error budget of +/-(1/2)LSB for the 10-bit SAR ADC under V_{ref}=1 V is +/- 488 μV, flicker noise could be safely ignored for this application case. However, in the high resolution case of the 18-bit, 1 MSPS SAR ADC, the 10 fold of the required bandwidth calculated from relation (15) is 396.4 MHz. The estimated flicker noise of the same switch transistor for this case is 2.88 μV (RMS) which is a little bit larger than that of the 10-bit case, showing flicker noise is dominated by the low frequency band. Given that

the error budget of +/-(1/2)LSB for an 18-bit under V_{ref}=1 V is +/-2 μV, flicker noise could not be ignored for this application case.

3.3 Discussion

The calculated flicker noise increases 7.5% when the number of bits changes from 10 to 18, while the error budget reduces 256 times for the same change in the number of bits. This indicates that the main element making the flicker noise be considerable in high resolution SAR ADCs is the exponentially decreasing error budget with the increasing number of bits.

The flicker noise calculation for an 18-bit, 1MSPS SAR ADC shown in this work is for an extreme design case where high resolution requirement comes together with high speed one. Fortunately, SAR ADCs are usually employed in low data rate applications where large size of switching transistors can be employed (the aspect ratio of the transistor (W/L) should be kept the same for consistent thermal noise). Employing a large switching transistor can reduce flicker noise of the switching transistor (refer to relation (8)) and consequently make flicker noise of the switching transistor ignorable, but employing a large switching transistor for low data rate high resolution SAR ADCs implies that flicker noise has already been considered.

The reported work on using switched transistor to lower flicker noise in CMOS ICs [17, 18] reflects a fact that the switched transistor has lower flicker noise than that calculated from relation (7), since flicker noise expressed in (7) is from a stationary model in frequency domain while switching behaviors make the switched transistor not always stay in the stationary state in frequency domain. The purpose of the flicker noise estimation in this work is to demonstrate in general that flicker noise cannot be simply ignored for high resolution SAR ADCs, but for the application case where a precise flicker noise evaluation is in need, the more complicated flicker noise model for periodically switched transistor [16] should be employed.

IV. CONCLUSION

Parasitic capacitances have both sides of effects on the DAC capacitor array. The positive one is that with parasitic capacitances thermal noise of the entire capacitor array decreases, which eases the noise restriction of the capacitor array. On the other hand, the accuracy of the capacitor array decreases when parasitic capacitances are taken into account. Since parasitic capacitances related to each plate of the unit capacitor are different, it is recommended to connect top-plates of unit capacitors together as the output node of the capacitor array to lower parasitic effects for high resolution applications. Although flicker noise can be ignored in low resolution SAR ADC designs such as less than 10-bit ADCs, the opposite tendencies of the increase in flicker noise and the decrease in error budget with the increasing number of bits, suggests that flicker noise should be evaluated for the high resolution SAR ADC design.

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