



An implantable mixed-signal CMOS die for battery-powered *in vivo* blowfly neural recordings

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ABSTRACT

A mixed-signal die containing two differential input amplifiers, a multiplexer and a 50 KSPS, 10-bit SAR ADC, has been designed and fabricated in a 0.35 μm CMOS process for *in vivo* neural recording from freely moving blowflies where power supplied voltage drops quickly due to the space/weight limited insufficient capacity of the battery. The designed neural amplifier has a 66 + dB gain, 0.13 Hz–5.3 KHz bandwidth and 0.39% THD. A 20% power supply voltage drop causes only a 3% change in amplifier gain and 0.9-bit resolution degrading for SAR ADC while the on-chip data modulation reduces the chip size, rendering the designed chip suitable for battery-powered applications. The fabricated die occupies 1.1 mm^2 while consuming 238 μW , being suitable for implantable neural recordings from insects as small as a blowfly for electrophysiological studies of their sensorimotor control mechanisms. The functionality of the die has been validated by recording the signals from identified interneurons in the blowfly visual system.

1. Introduction

Insects such as blowflies are among the most acrobatic fliers nature has created, which are the inspiration for the engineering of autonomous micro air vehicles. However, the analysis of neuronal activity related to visual information processing in insect model systems has been confined to restrained animals, limiting the understanding of the underlying neural control strategies. With the technological development in CMOS neural amplifiers [1], wireless power and wireless data transmission [2], recording neural signals from freely-behaving animals has been achieved in cat [3], marmoset [4], and locust [5] by the implantable chips.

The area available for implanting neural recording systems in freely-behaving animals is limited. The reported size of the neural recording die for the marmoset is 4.84 mm^2 [4], while for the locust is 3.54 mm^2 [5]. The available area in the head capsule of a blowfly is even smaller (about 1 mm^2 in each side of the blowfly brain, Fig. 1). Area limitations in turn, restrict the power consumption of the design. The heat density in the recording area should be low to prevent the detrimental effect excessive heat has on neural tissue [6]. To maintain a tolerable heat density of less than 800 $\mu\text{W}/\text{mm}^2$ for implantable neural recording [7], the reduction in area must be accompanied by a proportional reduction in power consumption.

The implantable neural recording IC can be powered either by

batteries or by a wireless power transmission link [8,9] to reduce the risk of infection and to eliminate the impact on the animal's movement dynamics when wires are used for power feeding. The restricted area for the implant, however, limits the size of antenna and coils, which reduces the efficiency of the inductive coupling mechanism, making it difficult to achieve wireless power transmission especially for *in vivo* neural recording in insects. Therefore, a battery is usually employed to power the recording circuits. The reported lightest weight of an assembled neural recording system with a battery is 172 mg for the case of locust [5]. It is worth stressing that 75% of the weight of that excellent locust recording design corresponds to battery weight. When considering the weight of 2 g for an adult locust, this load should not significantly affect its mobility given that it corresponds to less than 10% of its weight. However, for the blowfly with a typical weight of 50–100 mg, a payload of that order of magnitude would entirely disable the animal's free flight behaviour. More recently, the RFID inspired fully passive communication using microwave backscattering method has been introduced to neural recording [10], but system accuracy improvement and further reducing in size are required for this application.

Previous experiments have demonstrated that the blowfly is able to fly while carrying light loads under semi-free flight conditions with little impact on its manoeuvrability [11]. The load consisted of thin wire coils (0.8 mg each) [12], used for sensing position and orientation of the

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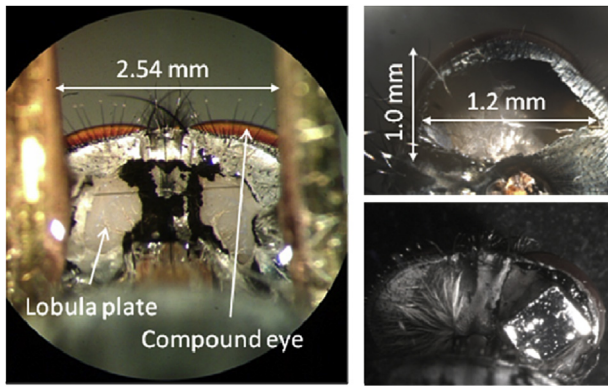


Fig. 1. Blowfly and the available implantable area. Left: Back view of the opened head capsule of a blowfly. Top right: Available implantable area for one side of the opened area (1.2 mm by 1.0 mm). Bottom right: a dummy die placed inside one side of the blowfly brain.

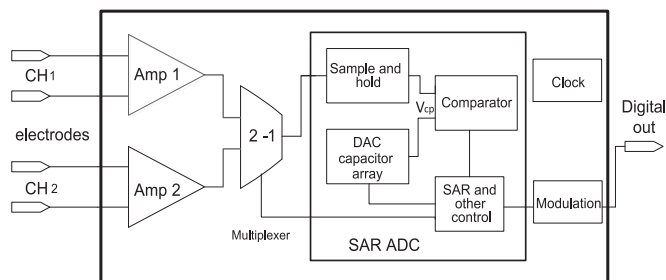


Fig. 2. Block diagram of the blowfly neural recording IC.

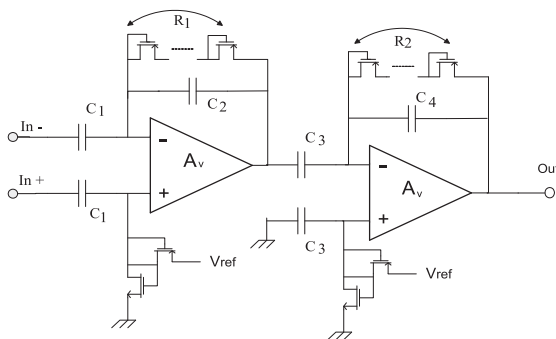


Fig. 3. Diagram of the two-stage amplifier.

blowfly's head and thorax. The coils were connected to ADC via a wire, which meant the blowfly was lightly tethered when flying. On the other hand, newly emerged light-weight solid-state thin film micro-batteries [13] make it possible to record neural signals *in vivo* from a freely-moving blowfly at least for a short period of tens of seconds. This will enable neural recordings from identified cells during flight and gaze stabilization behaviour. Directly powering up neural recording probes with batteries can decrease the recording noise, but the battery's supply voltage will keep decreasing during the recording session when the capacity of the battery is insufficient due to the size/weight restrictions. Accordingly, the decrease in supply voltage would affect the performance of the analog and mixed-signal circuits, such as degrading the gain of the amplifier, altering the clock frequency and affecting the accuracy of the ADC, while the digital circuits are fairly insensitive to supply voltage changes. Therefore, special efforts are required to evaluate the performance of directly battery-powered neural recording circuits when supply voltage keeps decreasing.

This paper presents a CMOS chip suitable for *in vivo* neural recording from the small brain of a blowfly. The designed die includes a neural amplifier whose performance is insensitive to a decreasing battery supply voltage, and a successive approximation register analog to digital converter (SAR ADC) with systematic performance analysis for battery power supply voltage dropping considerations. Neural recordings to validate the suitability of the design for studying identified neurons in the blowfly brain are also presented.

2. System design

2.1. System architecture

Neural recording systems are designed to record signals from high impedance (up to several MΩs) electrodes. Neural signals, such as local field potentials with a frequency less than 1 Hz or an action potential with bandwidth of several KHz [14], are $\mu\text{V} \sim \text{mV}$ level analog signals. Multi-channel recording ICs have been implemented thanks to the tiny layout area of a single channel CMOS neural amplifier. Wireless transmission has been integrated on-chip in some designs [3–5,8,15–19] adding to the potential mobility of the systems, while neural recording chips reported in Refs. [20–23] have been designed without on-chip wireless transmission.

The block diagram of the designed blowfly neural recording IC is shown in Fig. 2, where neural signals obtained from two channels are amplified and multiplexed and then converted into digital form by a SAR ADC. Given that the available area for implantation is of the order of 1 mm^2 (see Fig. 1), the feature-size of the process used was $0.35 \mu\text{m}$ and the fact that at least two recording channels (one for sensory and another one for motoring) are desirable for biologically meaningful experiments, wireless transmission has not been integrated in this design due to the power density considerations.

2.2. Blowfly neural amplifier

The AC-coupled capacitor feedback topology is a commonly adopted CMOS neural amplifier structure [1]. CMOS neural amplifiers have been widely reported [16,17,24–31] with design emphasis put on, for example, low-power, tunable cut-off frequency of the high-pass filter and digitally tunable gain.

The blowfly neural amplifier has been designed as shown in Fig. 3 to amplify the $50\text{--}300 \mu\text{V}$ peak-peak neural signal of the blowfly [32]. Two-stage CMOS amplifier was designed to achieve a 66 dB gain and a bandwidth of 0.1 Hz–6 KHz which covers the neural signal bandwidth from slow electro-encephalogram (EEG) (0.5 Hz–100 Hz for clinical use) to fast neural spikes.

The reference voltage (V_{ref}) of the on-chip ADC has been borrowed in order to supply constant bias (V_{gs}) to the amplifier preventing the gain from fluctuation when the supply voltage changes, since the open-loop gain A_v ($A_v = \frac{g_{m1}}{g_{m5} - g_{m3}} \times \frac{g_{m7}}{g_{d47} + g_{d48}}$ [32]) is proportional to the input transistor's g_m while the g_m is determined in weak inversion as,

$$g_m = \frac{1}{nV_T} I_D = \frac{1}{nV_T} I_{\text{DSAT}} \frac{W}{L} \exp\left(\frac{V_{\text{GS}}}{nV_T}\right), \quad V_T = kT/q \quad (1)$$

here $n = 1.2\text{--}1.6$, $V_{\text{gs}} < V_T$, hence the term g_m is almost linear to the V_{gs} (since $\exp\left(\frac{V_{\text{GS}}}{nV_T}\right) \approx \frac{V_{\text{GS}}}{nV_T}$). If V_{gs} were ordinary derived from a changing power supply, the open-loop gain of the amplifier would change with power supply, resulting in a change gain of the amplifier which is expressed as $A = \frac{A_v}{1 + (A_v + 1) \frac{C_2}{C_1}} \approx \frac{1}{A_v + 1} \frac{C_2}{C_1}$ for the first stage of Fig. 3.

The voltage reference-based bias adopted in this design makes the gm independent to the supply voltage (as shown in formula (1)), depressing the effects of the supply voltage on the gain. Also the 1.2 V supply voltage (20% dropping from 1.5 V analog supply) will not limit the dynamic

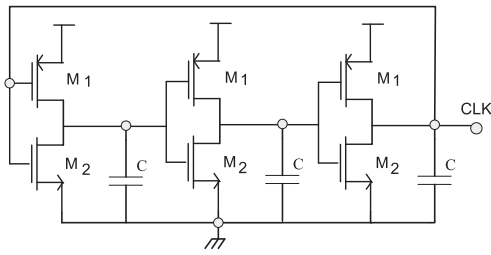


Fig. 4. The oscillator circuit for clock signal generation.

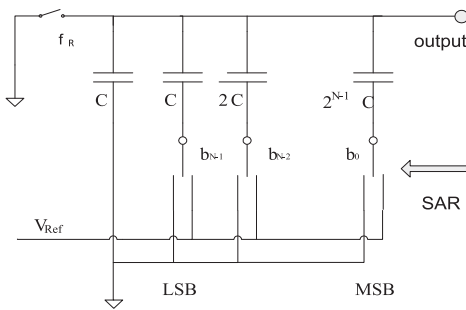


Fig. 5. Binary-weighted DAC capacitor array. Capacitors are charged by Vref through charging switches controlled by the SAR.

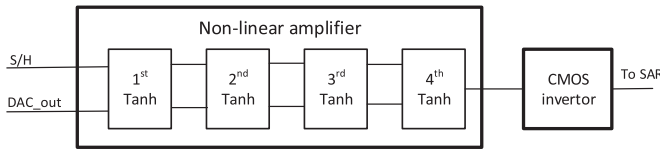


Fig. 6. Block diagram of the comparator.

range of the amplifier since with the maximum input amplitude of $300 \mu\text{V}$ the output dynamic range is 0.6 V under the gain of 66 dB gain.

2.3. SAR ADC

The SAR ADC has been chosen for its lowest power consumption in all types of the ADCs [33]. Under a 1 V reference voltage, an eight effective bit ADC can provide 4 mV resolutions, corresponding to the input neural signal of $2 \mu\text{V}$ when the gain of the amplifier is 66 dB (~ 2000 times). Therefore a 10-bit SAR ADC has been designed aiming to achieve more than 8 effective bits. The block diagram of the SAR ADC has been shown in Fig. 2.

2.3.1. Clock generator

A 1.3 MHz clock signal is generated by a ring oscillator for the digital part of the mixed-signal IC to control the 10-bit SAR ADC working at a sample frequency of 50 KSPS (determined by the practical adoption of 3–4 times of the signal bandwidth, 2 channels) as shown in Fig. 4. The frequency of a ring oscillator (F_{clk}) is expressed as [34],

$$F_{clk} = \frac{1}{nT}, \quad T = \frac{2C_{ox}L^2(k+1)(V_{DD} - 2V_T)}{(V_{DD} - V_T)^2} \left(\frac{1}{kK_{PP}} + \frac{1}{K_{PN}} \right) \quad (2)$$

where n denotes the number of the inverters in the loop, V_T denotes the threshold voltage, V_{DD} is the power supply voltage, L is the length of the transistor, others are known constants.

Given that the digital supply $V_{DD} = 3.3 \text{ V}$ and $V_T = 0.6 \text{ V}$ in the $0.35 \mu\text{m}$ AMS process, a 20% supply voltage drop results in 19.8% frequency decrease according to formula (2). Since the sampling frequency for a measurement channel is 25 KSPS , 19.8% decrease in frequency

results in a 20 KSPS sampling rate, which is still fast enough for sampling the several kHz bandwidth neural signals. Therefore the 20% supply voltage dropping can be tolerant in blowfly neural recording with respect to the sampling frequency.

2.3.2. DAC capacitor array

A common structure of the N -bit DAC capacitor array is the binary-weighted DAC capacitor array as shown in Fig. 5, which is implemented by 2^N matched unit capacitors and laid out in common centroid form [35,36]. Since there are 2^N unit capacitors in the common centroid layout structure, choosing a small unit capacitor value which is able to meet the accuracy requirements is the key to reduce the chip size. The unit capacitance in this design has been chosen as 89.44 fF (corresponding to a $10 \mu\text{m}$ by $10 \mu\text{m}$ poly-poly capacitor) based on the systematic calculation of the reliable minimum unit capacitance of the DAC capacitor array for SAR ADC [37].

The changing supply voltage affects the performance of the DAC capacitor array through the changing resistance of the charging switch. The resistance (R) of a CMOS charging switch can be expressed as,

$$R = \frac{L}{\mu C_{ox} W (V_{gs} - V_T)} \quad (3)$$

given that $V_{DD} = 3.3 \text{ V}$ and $V_T = 0.6 \text{ V}$, a 20% battery supply voltage drop results in 32% increasing resistance of the switch which slows down the charging process.

The charging process can be expressed as,

$$V_o = V_{ref} (1 - e^{-t/\tau}) \quad (4)$$

where C denotes the equivalent charging capacitance, and V_0 denotes the charged voltage of the capacitor C .

For the designed 10-bit SAR ADC, the relationship of charging time, the switching resistance and the DAC accuracy can be derived from formula (4) as,

$$\frac{V_{ref} - V_o}{V_{ref}} = e^{-\frac{T_0}{RC}} \leq \frac{1}{2^{10}} \quad (5)$$

where $T_0 = 1/F_{clk0}$.

When supply voltage changes 20%, the resistance of the charging switch increases 32% while the clock frequency decrease 19.8%. Under the new condition, formula (4) becomes

$$\frac{V_{ref} - V'_o}{V_{ref}} = e^{-\frac{T'_0}{RC}} = e^{-\frac{1-0.198T_0}{1.32RC}} = \left(e^{-\frac{T_0}{RC}} \right)^{\frac{1.25}{1.32}} \leq \frac{1}{2^{10 \times \frac{1.25}{1.32}}} < \frac{1}{2^{9.4}} \quad (6)$$

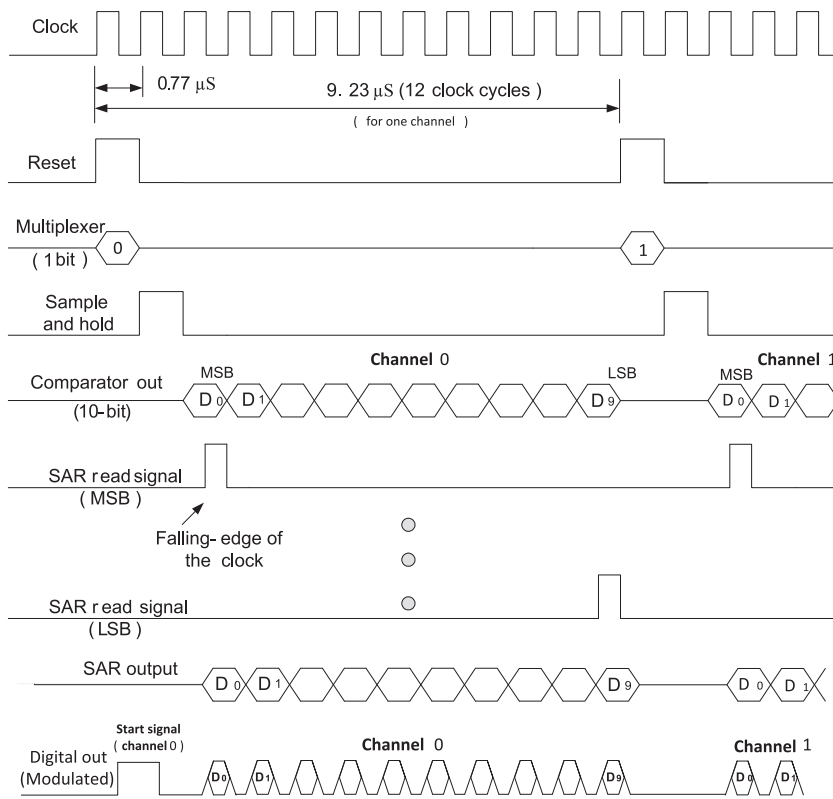
Therefore when power supply voltage drops 20%, the accuracy of the DAC decreases less than 0.6 bit .

2.3.3. Non-linear preamplifier-based pure analog comparator

Unlike the traditional mixed-signal compactor where a clock signal is necessary, the non-linear preamplifier and CMOS inverter based pure analog comparator [38] adopted in this design ensures that the performance of the comparator is independent of the clock signal whose frequency changes with supply voltage.

A strongly non-linear differential pair operating in weak inversion and characterized by an abrupt “tanh” characteristic, is adopted in this design to amplifies small input signals with a high gain and restricts the output of the large input signals to a pre-set ceiling voltage to get rid of the overdrive problem existing in the preamplifier of the conventional comparator. Similar to Section 2.2, the ADC reference voltage has been borrowed to provide a constant bias current to the preamplifier and the ceiling voltage of the preamplifier has been set as 1.2 V , consequently the 20% supply voltage drop from 1.5 V would not affect the gain of the overdrive-free non-linear preamplifier.

Fig. 7. Control timing of SAR and the format of the modulated output data stream (bottom).



To achieve a high pre-amplification, 4 stages of preamplifier have been adopted as shown in Fig. 6. The output of the first three stages is differential and the last stage is single-ended to connect to the following CMOS comparator. A 20% supply voltage drop from 1.5 V to 1.2 V does not affect the output of the differential stages but it introduces a 150 mV DC offset in the last amplification stage. Given the fact that the pre-amplification gain for small signal is larger than 700 times [38], the accuracy of the comparator will become 9.7 bits when supply voltage drops to 1.2 V since $150\text{mV}/700 = 0.22\text{ mV}$ corresponding to less than 0.3-bit error.

Although the designed comparator is a pure analog comparator, the decreasing clock frequency (due to the dropping supply voltage) eases the comparison task a bit since another input signal of the comparator, which is the output of the DAC capacitor array, has been slowed down.

2.3.4. SAR control and data modulation

The timing control of the SAR is shown in Fig. 7, which illustrates that a full conversion procedure for a sampled signal of a channel takes 12 clocks including reset, sample and hold, and 10 data conversion clocks. It seems that no special considerations are required for the 20% drop of the supply voltage for this pure digital part. However as mentioned in Section 2.3.1 that the clock frequency changes with supply voltage, the code format of the sole digital output pin shown in Fig. 2 has had to change from no-return-to-zero (NRZ) to return-to-zero (RZ) to make sure that the multiplexed digital output signal can be recovered correctly. Directly using NRZ code without clock information will wrongly recover the 5 unchanged consecutive bits as 6 bits when clock frequency decreases 20%. Also, to avoid interference of the switching activities, the output data is registered in the falling edge of the clock while switching activities are triggered by the rising edge of the clock.

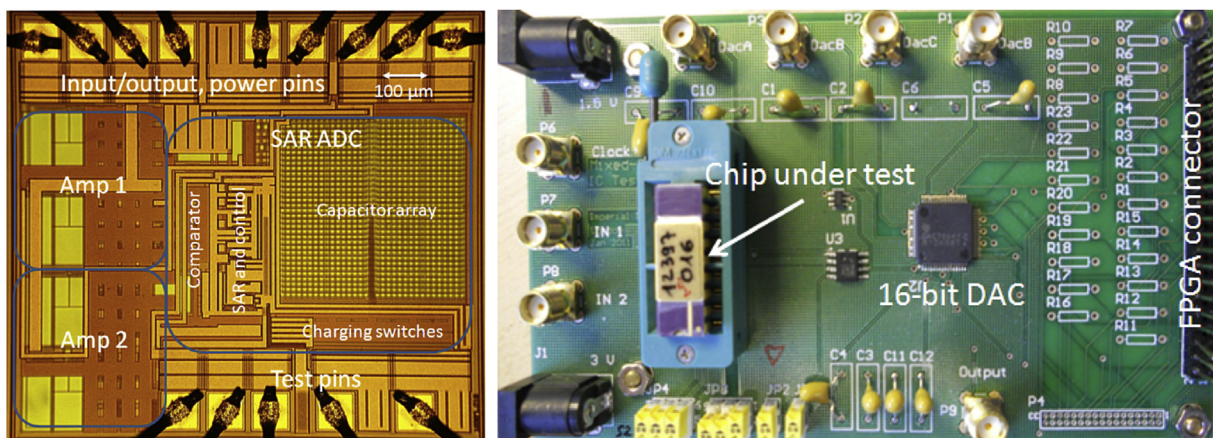


Fig. 8. Left: Layout of the mixed-signal 2-channel neural recording chip occupying an area of 1.1 mm × 1.0 mm. Right: Test set-up: the PCB designed for Chip tests.

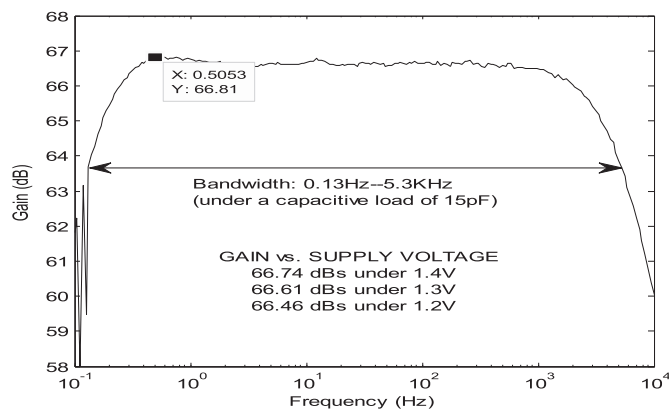


Fig. 9. Measured gain and bandwidth of the neural amplifier.

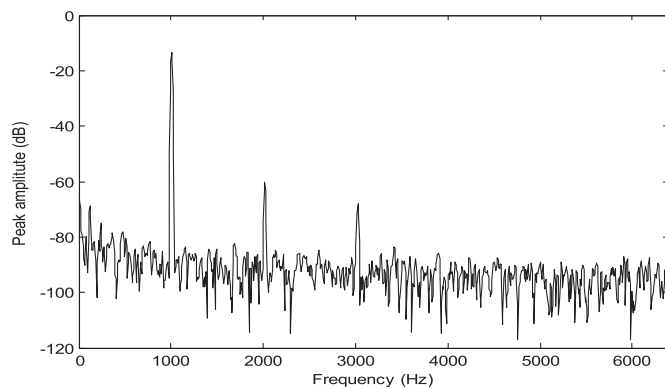


Fig. 10. THD tests: output spectrum for 1KHz input signal.

Data modulation is an exclusive function of the SAR ADC, in which the NRZ code is converted to RZ code to perform a modified serial communication protocol. The frame format of the data stream is shown at the bottom of Fig. 7. Data modulation is implemented by setting the output signal to a high level for a full clock period within the “reset” and the “sample and hold” periods of the first channel to generate a “start” flag and in the meantime to convert output digital bits from NRZ code to RZ code. As shown in Fig. 7, a full output data stream for a single sample of the input signal contains a “start” flag followed by 10 data bits from channel 0 and another 10 bits from channel 1. The modulated output data stream will be demodulated at the receiving side which is not power- and profile-constrained in most cases.

The above analysis indicated that the performance of the SAR ADC is not significantly affected by the power supply voltage decreasing: when supply voltage drops 20%, the SAR ADC will run at a clock signal slowed down to 20 KSPS for each recording channel (still fast enough for the less than 6 KHz bandwidth of the neural amplifier). The 20% supply voltage

Table 1
Performance summary of the neural recording die.

Amplifier	
Gain	66 dB
Bandwidth	0.13 Hz–5.3 KHz
Noise	0.17 $\mu\text{V}/\sqrt{\text{Hz}}$
THD	0.39%
Gain variation	<3% @ 20% drop in analog supplying voltage
SAR ADC	
ENOB	9.1 (8.3@20% drop in analog and digital supplies)
Sample speed	50 KSPS
Total die	
Area	1.1 (0.82 active) mm^2
Power consumption	238 μW (2 amps, a 2-1 multiplex, ADC, data modulation)

drops will introduce 0.3-bit error in comparator, 0.6-bit error in DAC capacitor array. Therefore the resolution of the SAR ADC is 9.1-bit when supply voltage drops 20% which has 1.1-bit redundancy to achieve the targeted more than 8 effective bits for blowfly's neural recording, while the clock extraction for off-chip data demodulation is not affected by the changing clock frequency due to the adopted RZ code.

3. Measurement results

The layout of the fabricated chip is shown in left of the Fig. 8. It measures 1.1 mm \times 1.0 mm with an active area of 0.82 mm^2 . The input/output and power pads are placed on one edge of the chip for ease of connection. The pads placed on the opposite edge are used exclusively for testing. As shown in Fig. 1, the available implantable area in one side of the blowfly head capsule is about 1.2 mm \times 1.0 mm. Thus the fabricated die, occupying an area of 1.1 mm \times 1.0 mm, can be fitted in the animal's brain for *in vivo* neural recording. It can also see that the DAC capacitor array for SAR ADC (shown in middle right of the left of Fig. 8) occupies 1/3 of the active area of the die, so choosing a reliable minimum unit capacitor is the key to make the chip size suitable for blowfly's neural recording. The confident level of the chosen unit capacitor in this design is 99.9% which almost certainly gets rid of both matching error caused by the manufacture deviation and the thermal noise of the capacitors in DAC capacitor array, resulting a very high yield rate (all 20 chips from a small batch fabrication running work well [37]). The small die area is also benefited from the on-chip data modulation to share one output pin for all measurement channels.

A test PCB shown in the right of the Fig. 8 has been designed, which contains a commercially available 16-bit DAC (DAC7664 from Texas Instruments) to test the designed SAR ADC. The test PCB is connected to a commercially available FPGA board to demodulate the ADC data in real-time and to provide USB communication to the host PC.

3.1. Amplifier

The performance of the designed neural amplifier has been tested using a spectrum analyzer (SR785 from Stanford Research Systems). The measured gain and bandwidth of the amplifier is shown in Fig. 9, which confirms that the designed neural amplifier achieves a gain of 66 + dB with a bandwidth of 0.13 Hz–5.3 KHz under a 1.5 V supply. Considering the fact that the input capacitance of the spectrum analyzer is 15 pF, the real bandwidth of the amplifier should be a bit wider since the capacitor load of the amplifier, which is the sample and hold capacitor of the ADC, has a value of 6 pF in this design.

The gain and bandwidth of the amplifier were measured when decreasing power supply levels from 1.5 to 1.2 V with a step of 0.1 V. The results listed in Fig. 9 confirm that when the supplied voltage dropped, there was little change in gain. The maximum gain difference between 1.5 V and 1.2 V supplies was 0.35 dB corresponding to a 3% of gain change.

Total harmonic distortion (THD) is a tricky point in the low-power design. Most of the low-power neural amplifiers are reported without a THD figure therefore it is difficult to directly compare their low-power performance since a low THD always comes with high power consumption. For neural applications such as spike detection, THD is not important, but for general neural recording applications, the linearity of the amplifier should be taken into consideration. The linearity of the designed neural amplifier has been tested by applying a 1KHz input signal and measuring the output spectrum. The THD calculated from measured output spectrum shown in Fig. 10 is 0.39%, which can be roughly translated to the ADC parameter of the effective number of bits (ENOB) of 7.7.

As shown in Fig. 2, the amplifier designed here is part of the neural recording ASIC, therefore conventional linearity requirements of 1% THD for neural amplifier [39] which corresponds to 6.4 ENOB may be suitable for general neural recording applications where a typical 8-bit

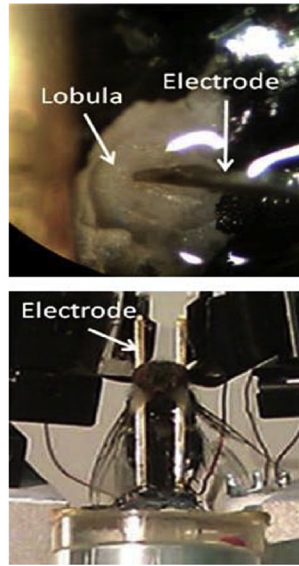
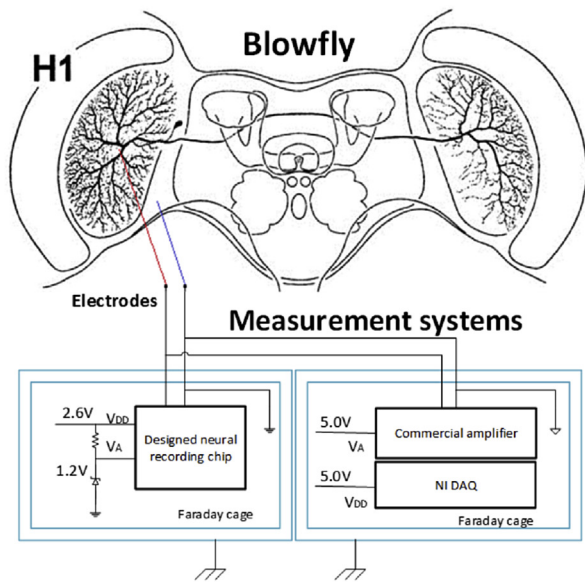


Fig. 11. Experimental set-up for extracellular neural recording. Left: measurement set-up (designed chip in parallel to a commercial system). Right: electrode inserting in the brain (top) and a blowfly with electrodes placed for neural recording (bottom). H1-cell reconstruction adopted from [42].

ADC is adopted. A higher THD is required in this design when considering that the following ADC is 10-bit, resulting in a power consumption of 16.5 μ W in this design.

3.2. SAR ADC

A 5 KHz test signal was applied to the ADC and the demodulated ADC results were recorded. The signal to noise ratio (SNR) of the SAR ADC has been calculated as 56.68 dB which corresponds to 9.1 ENOB [37]. Decrease 20% for both analog and digital supply voltages, SNR has decreased by 4.61 dB, resulting in an 8.3 ENOB. The performance of the designed chip is summarized in Table 1.

3.3. Neural recording experiments

Calliphora vicina (blowfly), a model species for studies on insect gaze and flight control [12,40], had been selected for neural recording tests of the designed die. The commercial electrodes used (FHC Ltd, catalog number UEWSHGSE3P1M) were 1.2 mm tungsten microelectrodes with an impedance of 1–1.2 M Ω . They were inserted into the posterior part of the blowfly's third optic lobes (lobula plate) as shown in Fig. 11, while the reference electrode was in contact with the animal hemolymph. The neural recording tests focused on the motion sensitive H1-cell [41]. Spontaneous action potentials were recorded extracellularly.

To evaluate the performance of the designed IC, the properties of the newly designed recording IC introduced here, have been compared to

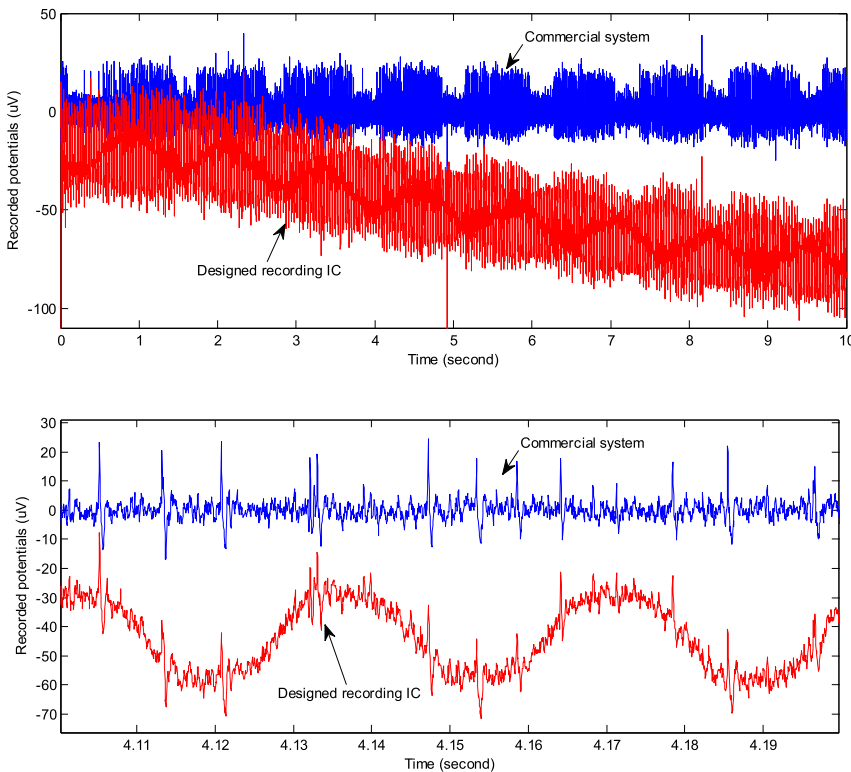


Fig. 12. Ten-second neural recordings from the H1 interneuron of the *Calliphora vicina* by the commercial system and the designed neural recording IC. Top: normalized recording data. Bottom: zoom-in showing that the designed IC can pick up extra low-frequency in-band signals.

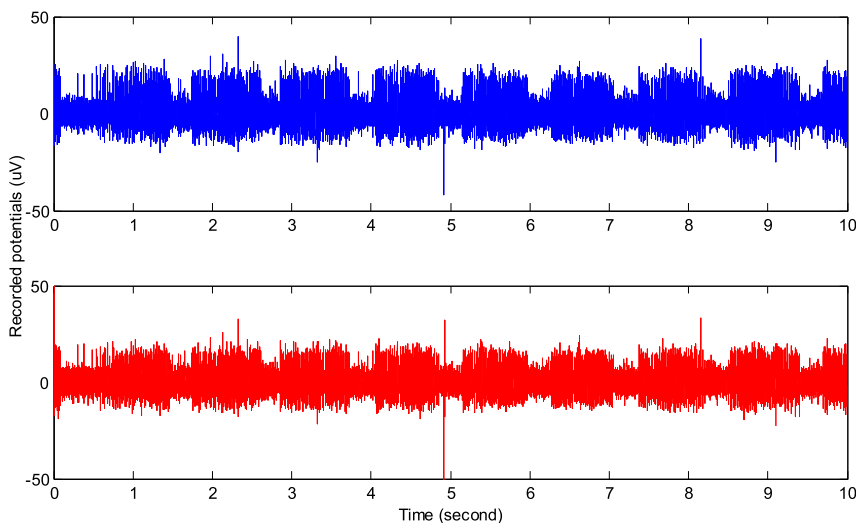


Fig. 13. Top: data recorded from the commercial system. Bottom: data recorded from the designed IC after filtering with a 100 Hz high-pass filter.

that of another neural recording system built from commercially available components (INA332 from Texas Instruments; AD8607 from Analog Devices and National Instruments DAQ card of NI USB-6215 [43]). The measurement set-up is shown in Fig. 11. To measure μV neural signals, electromagnetic interference (EMI) and the system grounding should be considered. Due to the relatively large size of the electrode, only one pair of electrodes (one for signal, another one for reference) is adopted. As shown in Fig. 11, both measurement systems have been electromagnetically shielded by metal enclosures connected to the earth ground to reduce electromagnetic noise. The analog ground and digital ground in the commercially available system have been connected at one point to form the commercial system ground, which is also connected to the system ground of the designed IC. This linked system ground is then connected to the reference electrode of the blowfly to complete the “star grounding” avoiding unexpected ground loop formed in neural recording systems shown in Fig. 11.

Fig. 12 illustrates concurrently recorded neural signals from the H1-cell. Both recorded signals were normalized for the gain of the corresponding recording system and the DC offset was subsequently removed to enable the comparison. Apparently the neural signal recorded by the designed recording IC (red in top of Fig. 12) is larger than that recorded using the commercial system (blue in top of Fig. 12). When zooming in on a time window of 100 ms shown at the bottom of Fig. 12 (corresponding from 4.1 to 4.2 s at the top of Fig. 12) it reveals that the designed neural recording IC picked up additional signals in the low-frequency band (the dominant frequency shown in Fig. 12 is about 30 Hz). This low-frequency signal makes the output signal range of the designed IC appear larger

than that of the commercial system. The commercial system, specifically designed to record neural spikes, has high pass properties. Hence no drifting is recorded by the commercial system, while the designed IC being almost DC coupled (with the low cut-off frequency of 0.13 Hz), also records low-frequency signals and exhibits baseline drifting shown in the second trace of Fig. 12.

To further compare signals recorded from the two systems, an FFT was applied to both recorded signals. The power spectrum of signals recorded from the designed IC showed peaks at 0.4, 29.0 and 86.6 Hz in the low-frequency band while that of the signals of the commercial system did not show visible low-frequency peaks. It has been confirmed that low-frequency signals picked up by the designed recording IC resulted from interference with the DAQ card (NI USB-6215, National Instruments Corporation, Austin, TX, USA) when both recording systems are attached to the same blowfly. After incorporating a 100 Hz high-pass filter, the resulting post-processed signals of the designed IC are shown at the bottom of Fig. 13, while the recorded signals from the commercial system are shown at the top of Fig. 13 for comparison. The two traces shown in Fig. 14 are zoomed-in for a 50 ms time window of Fig. 13 (corresponding from 4.10 to 4.14 s), demonstrated that the neural activities (eg. 20 $\mu\text{Vp-p}$ spikes) have been successfully recorded by the designed chip.

The auto correlation R_{xx} and the crosscorrelation R_{xy} are calculated to determine the similarity of the two signals. The calculated $R_{\text{bottom-bottom}}(0)/R_{\text{top-bottom}}(0)$ for signals recorded with the designed IC (shown at the bottom of Fig. 14) and the commercial system (shown at the top of Fig. 14) is 87%, which confirms the similarity of the two signals and

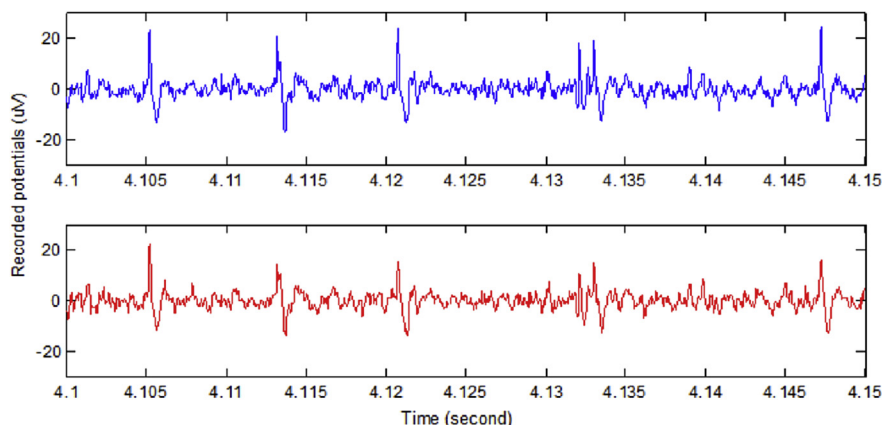


Fig. 14. Comparison of the recordings. Top: neural signals recorded by the commercial system. Bottom: post-processed neural signals of the designed die.

Table 2
Performance comparison of animal neural recording ICs.

	Assembled system size (weight)	Tech.	Power Consumption (power supply)	Wireless Transmission (distance/telemetry frequency/antenna)	Battery (weight/nominal capacity)	Die size (weight)	Animal targeted
Mohseni [4] (2005)	17 mm × 12 mm (1100mg)	1.5 μm CMOS	2200μW	Yes (~0.5 m/85MHz no info)	2×	4.84mm ²	Marmoset
Harrison [19] (2010)	13 mm × 9 mm (720 mg)	0.6 μm Bi-CMOS	3600μW	Yes (~2 m/900MHz/>4cm)	2 × E337 (260mg/8 mAh)	6.5 mm ² (4mg)	Elec. fish, locust
Harrison [5] (2011)	5 mm × 6 mm (172 mg)	0.35μm CMOS	1000μW	Yes(~2 m; >4cm)	1 × E337 (130mg/8 mAh)	3.54 mm ² (3mg)	Locust, dragonfly
This work	N/A (die only)	0.35μm CMOS	238μW	No	1 × CBC012 (8mg, 12 μAh)	1mm ² (<2mg)	Blowfly

therefore the designed chip could capture blowfly neural signals.

4. Discussion

The designed chip has a power density of 290 μW/mm² in the active area, which is lower than the 800 μW/mm² power density limitation for implantable neural recordings. Therefore the designed chip meets the power density restriction for implantable neural recording in blowfly. However, the power consumption of the chip is expected to be further reduced to ease the battery capacity requirement for blowfly's neural recording. The state-of-the-art circuit design technologies in low integrated noise/low noise-efficiency-factor (NEF) amplifier design [44] when combined to the low 1/f noise technology of chop amplifier [45] will be helpful for further improvement of the performance of the amplifier for the special application requirements of high THD and ultra-low cut-off frequency for neural recordings. The state-of-the-art SAR ADC design [46] will help for further reduce the power consumption of the chip. Unlike the general neural recordings where lower electrode impedance are welcomed, in blowfly neural recording the electrode impedance has been deliberately designed as 1 MΩ, therefore the capacitance C₁ in Fig. 3, which occupies 50% area of the amplifier in Fig. 7, can hardly go smaller due to the high electrode impedance. A high capacitance density CMOS process can reduce the capacitor size and accordingly reduce the area of amplifier. Another possible way to reduce the size of the amplifier for accommodation more measurement channels is to exploit direct coupling totally getting rid of the area consuming capacitors, where the DC level of neural signals (offset and drifting) is extracted and then fed-back to the neural amplifier via an ADC and a DAC loop so that neural signals could be amplified without considering the offset and DC drifting [47]. However, the direct coupling method is reported with off-chip signal processing in its feedback loop. Therefore it can be hardly adopted for *in vivo* neural recordings in blowfly since it requires two-way communication (one for data output and another one for close-loop control).

The fabricated die constitutes the first critical step for the realization of a wireless stand-alone probe for blowflies. Ideally, two recording chips per blowfly would be needed: one for the left and one for the right part of the blowfly brain. Each die would be bound with a blowfly-specific microelectrode array comprising an array of 2 × 3 tungsten electrodes. The distance between the rows of electrodes should be close to 50 μm while the distance between electrodes in a row should be ~200 μm. The length (height) of the electrodes should be ~500 μm and their impedance restricted between 1 and 1.2 MΩ. The realization of such an electrode array is ongoing. It involves various micro-engineering processes and has led not yet to a prototype which meets all the specifications in full. The 50 μm × 400 μm electrode array chip should be attached under a very specific angle with respect to the recording die in order to record neural signals from both the correct site and “depth” of the brain. It is the attachment of the electrode array under an angle that allows the fitting of the two chips (neural die + blowfly electrode array) within the available area in the head capsule of 1.2 mm × 1.0 mm. Regarding the power supply, the thorax of the blowfly could be exploited for accommodating a thin-film battery, a simple short range transmitter and light weighted

elementary antenna. The size of blowfly's thorax (~2.5/3 mm × 4 mm) could host a custom-made unpackaged die such as the 2.8 mm × 3.5 mm 12 μAh rechargeable bare die of EnerChip CBC012 from Cymbet: a low capacity (in the range of 10–50 μAh) thin-film battery, which would support a short duration of an *in vivo* neural recording from a freely moving blowfly. Placing the power and data storage circuits on the thorax has the additional advantage that the animal's flight dynamics should be affected less than when placed elsewhere. With the restricted battery size/weight in implantable neural recording, a notable supply voltage dropping when low capacity battery working in a relatively high current (eg. in this case a 12 μAh battery working at several mA current for full recording circuits including low-power short range wireless communication) is expected, and therefore special considerations to deal with the supply voltage dropping are necessary for the battery-powered *in vivo* blowfly neural recordings.

The performance of the designed neural recording die has been compared to the performance of other neural recording chips for animals. The results are listed in Table 2. This work has achieved the smallest chip size, extending the types of the animals for neural recording under freely moving to animals as small as the blowfly, for the *in vivo* studies of flying control.

5. Conclusions

A neural recording die which is small enough in size and consumes enough low amounts of power has been designed for battery-powered implantable neural recordings into the head capsule of a blowfly. The systematic circuit performance analysis for both amplifier and SAR ADC circuits demonstrated that the designed mixed-signal chip meets the application requirements for blowfly's neural recording where supply voltage drops quickly due to the space/weight limited insufficient battery capacity. The gain of 66 + dB, 0.39% THD and the bandwidth of 5.3 KHz make the chip suitable to record neural signals generated by identified visual interneurons. The on-chip 10-bit SAR ADC provides sufficient measurement resolution for neural recording under a wide supply voltage range. The low power density of the die enables implantation within an insect as small as a blowfly for studying the neural basis of behaviour in freely moving animals. Furthermore, the performance of the chip does not fluctuate with a 20% decreasing supply voltage, therefore the designed chip is suitable for directly battery-fed *in vivo* neural recordings.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at <https://doi.org/10.1016/j.mejo.2018.01.022>.

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