Design and Analysis of a Novel Multi-Input Multi-Output High Voltage DC Transformer Model

By

Mais Alzgool

A thesis submitted in partial fulfilment of the requirements of the University of the West of England, Bristol for the degree of Doctor of Philosophy

Faculty of Environment and Technology, Department of Engineering Design and Mathematics, University of the West of England, Bristol September 2018

Thesis Advisory Committee

DOS. Dr. Hassan Nouri

Dr. Chris Toomer

ABSTRACT

A novel Multi-Input Multi-Output (MIMO) step-up DC transformer for applications in high voltage renewable energy sources is designed and presented. This design topology can provide a high step-up conversion gain without using an internal AC transformer, to supply different DC output voltage levels from integration of various input power sources. MIMO DC transformers provide flexibility in terms of choice and availability of the power source, reduction in the number of power lines used to transfer power to pre-specified locations as well as enhancement in system reliability. The comprehensive operating principle, theoretical analysis and design criteria of the proposed MIMO step-up DC transformer have been discussed. The proposed DC transformer has the advantages of simple configuration, fewer components, high conversion gain and high efficiency. The relations between the inputs and outputs are expressed mathematically in terms of passive components and the duty cycle of power switches. Also discussed is the sizing of the employed inductors and the capacitors for a particular application. The derived input and output expressions for ideal and non-ideal DC transformer are solved numerically and the results are validated against those obtained through MATLAB-SIMULINK simulation. Tentative analysis of the numerical and simulation results shows a close correlation.

The Proportional Integral Derivative (PID) controllers have been used to control and operate the proposed MIMO step-up DC transformer in Continuous Conduction Mode (CCM) utilising the concept of closed loop Voltage Mode Control (VMC). As the behaviour of the proposed MIMO DC transformer resembles a nonlinear plant performance, hence Small Signal Modelling (SSM) and linearization of the plant are required to obtain a linear model for ease of analysis and to achieve a more stable and regulated output voltages. To obtain the SSM of the plant to be controlled, the mathematical modelling and the state space representation in a matrix form of the proposed MIMO DC transformer have been derived within the DC transformer's switching states. This yields the transfer function presentation of the designed DC transformer which have been used to determine the system's stability.

The robustness of the DC transformer's controller is demonstrated through MATLAB-SIMULINK simulation under different scenarios. The scenarios are dependent on the type of utilised input sources. The simulation results demonstrated the flexibility and robustness of the designed controller under input and load variations through adaptability of the controllers for ensuring the system produces the desired output voltage level. This is achieved by controlling the ON and OFF time of the power switches. The system's performance further scrutinised under line to ground short circuit faults across the switches

and open circuit faults across the diodes. Furthermore, a comparative performance and cost analysis has been carried out between the proposed MIMO and two selected published DC transformers. The selection criteria is discussed in details. The main parameters used for analysis are size, weight, voltage conversion gain, duty cycle and efficiency. Also considered are the cost of utilised semiconductors and passive components.

The simulation results of the proposed MIMO (e.g. three-input two-output) step-up DC transformer revealed that the proposed DC transformer achieves the predetermined output voltages $8\ kV, 11\ kV$ with small voltage ripple factors of 0.178% and 0.129% respectively, with $100\ mA$ peak ripple current and no observation of overshoot in the DC bus voltage. These findings confirm the flexibility and adaptability of the controller designed for the proposed MIMO step-up DC transformer.

Dedication

This work is dedicated to my husband, **Ghaith,** and our girls, **Meera** & **Ghina**

Acknowledgments

First, praises and thanks to the God, the Almighty, for his blessings throughout my studies. I would like to acknowledge all the invaluable help from my supervisor, Dr. Hassan Nouri, without whom this work would not have been possible. This dissertation comes from numerous discussions with him, from his keen insight and guidance in a productive research area. I want to thank him for consistently encouraging me no matter under what kind of situations.

I also want to thank Dr. Chris Toomer, for her help and guidance during my study at UWE, no matter in the researches, the stages of my dissertation work or other aspects. And also to show her my great appreciation for her great support.

I owe more than thanks to my family members for their support throughout my studies; I would like to thank my father Dr. Bassam Alzghoul, my mother Heyam Alawneh, as well as I would like to thank my father and mother in law for their encouragement. Without them I would not have reached this point.

A special thanks to my husband, Ghaith, for his encouragement, patience and endless support over the years. Thank you for helping me and for being by my side all the time.

Finally, I am grateful to my friends and colleagues at UWE. Not only the knowledge, but also the research experience and friendship I gained here will be beneficial for the rest of my life.

List of Publications

(1) Alzgool, M. Alzghoul, G. Nouri, H. and Toomer, C. (2016). *A Novel Multi-Inputs-Single-Output DC Transformer Topology.* Coimbra: 51st International Power Engineering Conference, ISEC Portugal. “Cited by 2”.

(2) Alzgool, M. and Nouri, H. (2017). *Design, Control and Modelling of a Novel Multi-Input Multi-Output Boost Converter Hub*. Amman: the 10th Jordan International Electrical and Electronics Engineering Conference (JIEEEC).

(3) Alzgool, M. and Nouri, H. (2018). *PID Controller Design for a Novel Multi-Input Multi-Output Boost Converter Hub*. Journal of Electrical Engineering (JEA), Vol 2, No 1.

Table of Contents

Glossary

AC	Alternating Current
DC	Direct Current
MIMO	Multi-Input Multi-Output
SISO	Single-Input Single-Output
MISO	Multi-Input Single-Output
DISO	Double-Input Single-Output
HVDC	High Voltage Direct Current
FACTS	Flexible Alternating Current Transmission System
MOSFET	Metal–Oxide Semiconductor Field Effect Transistor
FET	Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
GTO	Gate Turn OFF Thyristor
ZVS	Zero Voltage Switching
FLC	Fuzzy Logic Control
P	Proportional Controller
PI	Proportional Integral Controller
PID	Proportional Integral Derivative Controller
M	Conversion Ratio
D	Duty Cycle of power Switch
DCM	Discontinuous Conduction Mode
PWM	Pulse Width Modulation
MIC	Multi-Input Converter
CCM	Continuous Conduction Mode
CMC	Current Mode Control
VMC	Voltage Mode Control
k_d	Derivative gain
k_i	Integral gain
k_p	Proportional gain
LPF	Low Pass Filter
SMC	Sliding Mode Control

SSM	Small Signal Model
Z-N	Ziegler-Nichols tuning method
MATLAB	Matrix Laboratory
PFM	Pulse Frequency Modulation
SCR	Silicon Controlled Rectifiers
BJT	Bipolar Junction Transistor
SEPIC	Single-Ended Primary Inductance Converter
PV	Photovoltaic
WVR	Wind Voltage Regulator
D/A	Digital /Analogue converter
A/D	Analogue/ Digital converter
CMOS	Complementary Metal Oxide Semiconductor

CHAPTER ONE

INTRODUCTION AND RESEARCH OBJECTIVES

1.1. High Voltage Direct Current (HVDC) Transmission Technology

1.1.1. Reasons for HVDC

In the future the size of offshore wind farms and the distance to shore are expected to increase, which leads to higher losses in the Alternating Current (AC) collection grid and AC transmission [19] Whereas the use of AC technology is applicable and financially feasible for wind farms located less than $50\,km$ offshore [2]. Direct Current (DC) technologies can provide lower losses and use cheaper cables than for AC. High Voltage Direct Current (HVDC) transmission systems have already been proven technically beneficial and cost-effective over AC transmission for distances longer than $60-70\,km$ according to [3], and applying DC technologies not only to the transmission systems but also to the collection grid of offshore wind parks could prove additionally effective according to [4]. It has been identified in several previous studies such as in [3] and [7] that HVDC transmission systems, have a number of advantages for integrating large offshore wind farms over AC connections. So, DC transmission starts to become cost-competitive, mainly due to the large capacitive current losses associated with AC links. For this reason, HVDC transmission technology becomes a feasible and economical solution compared to HVAC transmission. Furthermore, the HVDC transmission can alleviate the propagation of voltage and frequency fluctuations which occur due to variations in wind strength. This can result in significant economic and environmental benefits. Figure 1.1 shows that the HVDC transmission technology enables the efficient transportation of electrical power over large distances and for subsea applications with losses of around two percent, excluding cable losses [5].

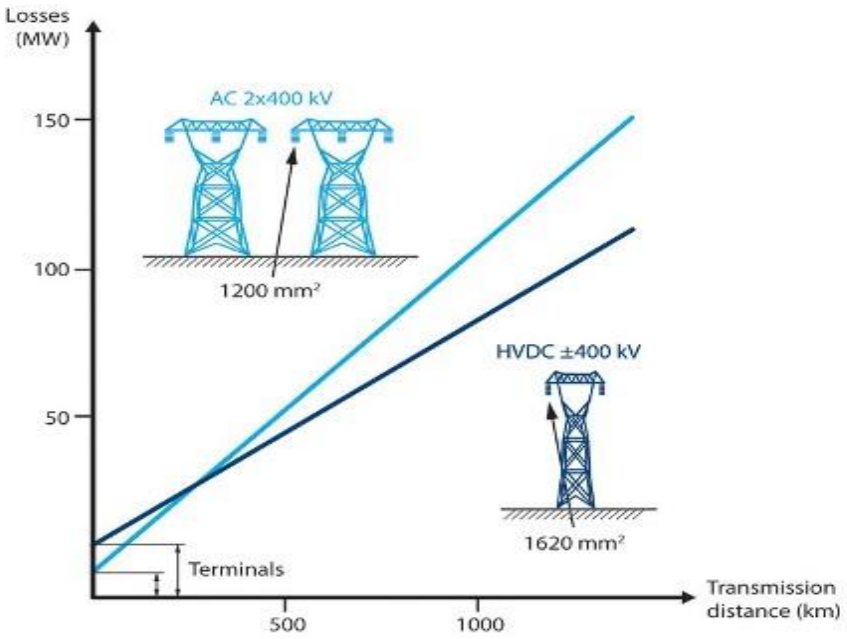


Figure 1.1 losses in AC and DC transmission technology with the transmission distance- Image Credit ABB [6]

A HVDC transmission line costs less than an AC line for the same transmission capacity. However, it is also true that HVDC terminal stations are more expensive because of the fact that they must perform the conversion from AC to DC, and DC to AC. But over a certain critical distance (approximately $600 - 800\ km$) the HVDC alternative will always provide the lowest cost [6] as shown in figure 1.2.

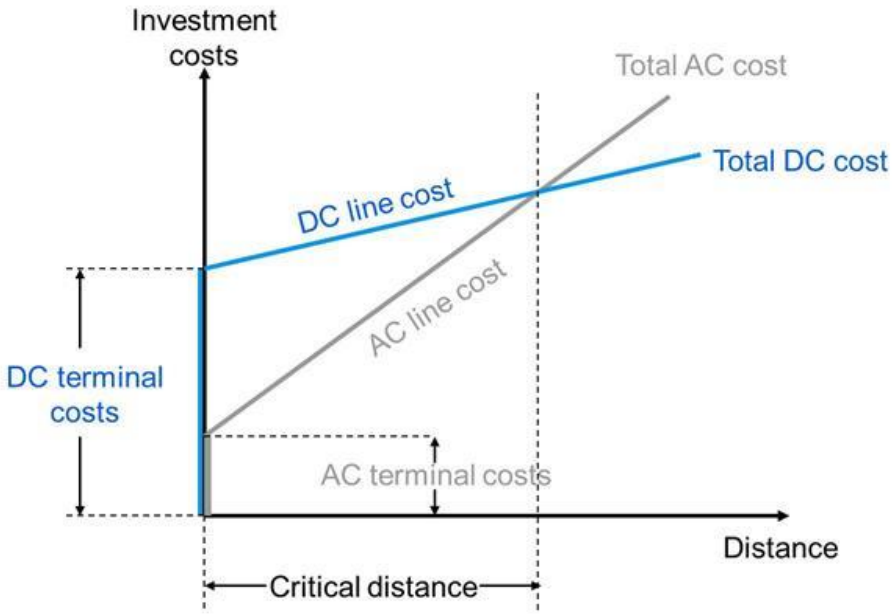


Figure 1.2 total AC and DC transmission technology cost with the transmission distance- Image Credit ABB [6]

It could be summarised that the HVDC technology becomes more desirable for the following reasons as listed in [7]:

1. Environmental advantages where HVDC systems have a lower environmental impact because they require fewer overhead lines to deliver the same amount of power as HVAC systems. And HVDC is a key component in the future energy system based on renewable energy sources such as wind and solar power which are remotely located.
2. Economic advantages where HVDC is the cheapest solution compared with the conventional HVAC transmission over long distances because the construction costs of DC lines are cheaper than for AC lines, in spite of the extra cost of a converter station.
3. Asynchronous (Non-synchronous) interconnections with HVDC technology. Asynchronous interconnection between adjacent power systems.
4. Fast control of power flow, which implies stability improvements, not only for the HVDC link but also for the surrounding AC system.
5. Direction of power flow could be changed quickly (bi-directionality) for storage elements applications.
6. No limits in transmitted distance. This is valid for both overhead lines and sea or underground cables.
7. Reinforcing of an AC network which is heavily loaded.
8. The elimination of AC collector system at the remote generating stations can result in better efficiency in the operation of turbines which are free to run at speeds independent of the system frequency.

The aforementioned reasons led researchers to focus on HVDC technology and its applications.

1.1.2. Background to offshore Wind farms and (the Role of) why MIMO DC Transformers

The demands of a growing worldwide population on the electricity supply, alongside concerns regarding fossil-fuels, greenhouse gases and climate change have led power engineers to seek alternative energy sources. Hence, renewable energy has received much attention in recent decades. The government of the United Kingdom has set out a target to develop $25\ GW$ of power from offshore wind farms by 2020 and more than $40\ GW$ by 2050, according to the country's grid operator, national grid [2]. At a European level, it is expected

that there will be 40 GW of installed offshore capacity by 2020, rising to 150 GW by 2030 [9]. In the USA, about 85% of the gross offshore wind resource (4000 GW) occurs in areas of transitional depths ($30-60\ m$) or deep-water areas ($>60\ m$) located up to more than 90 km from the shore [10]. To integrate such a large amount of remote offshore energy generation into the existing onshore networks creates a number of technical, economic and environmental challenges for the developers and system operators [12]-[14].

In general, offshore wind strength is greater than onshore strengths and many large-scale wind farms (greater than $1GW$) are constructed in offshore locations. Offshore generated power is normally transmitted over long distances. In the future, proposed wind farms at distances of over 60 km from the shore will be connected to the mainland grid only through DC links [2]. As stated in section 1.1.1 DC can transport relatively more power at the same voltage/insulation level than AC. Therefore, HVDC transmission is considered an effective way of connecting offshore wind farms to the main grid. The European super-grid is proposed to interconnect the existing HVDC lines in the North and Baltic seas and to provide transmission access for offshore wind farms [15]. Many large HVDC links experience limitations on power levels and the sending and receiving ends of the DC networks have difficulties in accommodating the number of injections or distributions of high powers at a single point. The HVDC limitations are driving the demand for Multi-Input and Multi-Output (MIMO) DC transformers or DC sub-stations by highlighting the significant incentive of a technology that can provide additional access points (input and output). Figure 1.3 highlights the general structure of offshore wind farm HVDC technology with and without MIMO DC transformers, where MIMO DC transformers provide an integration of m number of wind farms to supply n number of loads in different locations through submarine DC cables with various voltage levels.

The proposed offshore MIMO DC substation (or DC transformer) is more flexible than the currently used parallel connected mesh type multi-terminal HVDC and also with the older version of AC collector points which employ AC transformers. The offshore MIMO DC transformer could be assembled offshore as modular parts which are easy to combine whereas the AC transformers are bulky which will add more problems to integrate them from shore to offshore.

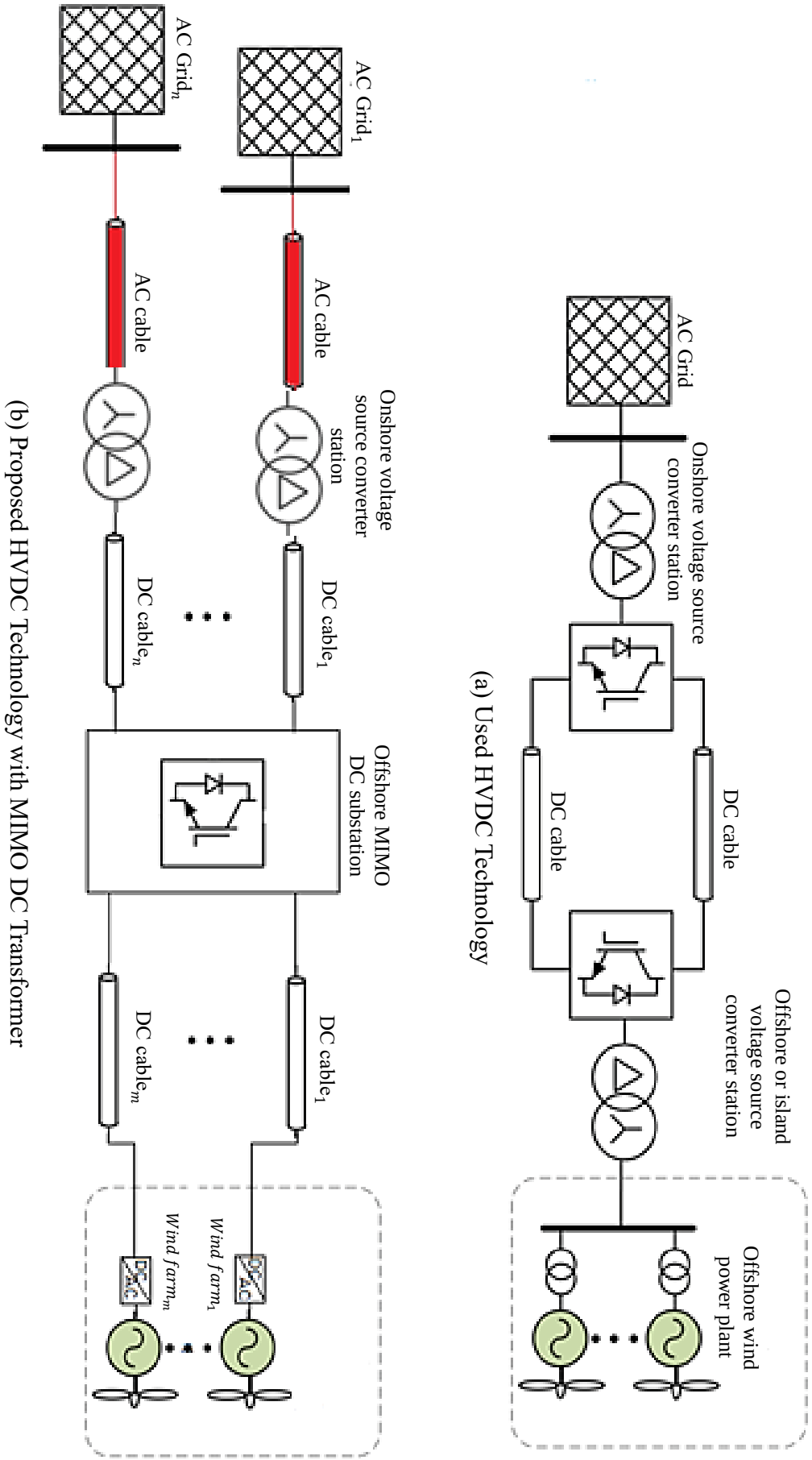


Figure 1.3 general structure of wind farms (a) used HVDC technology [18] and (b) the proposed HVDC technology with MIMO step-up DC transformer

Furthermore, a suitable megawatt DC transformer would enable tapping of HVDC lines and hence the development of multi-terminal HVDCs which are favourable conditions for submarine DC transmission, which requires DC voltage stepping at megawatt power levels. A high-power DC transformer would also aid the development of Flexible AC Transmission System (FACTS) technology by enabling connection to a wide range of DC sources.

Also the proposed MIMO DC transformer will be useful for onshore wind farms where the energy supply infrastructure will face severe shortages in the future and will require integration and increased diversity of energy sources, such as photovoltaic cells, fuel cells, and batteries as shown in figure 1.4 which will have different voltage and current characteristics. This increase in the type and the rating of these sources suggests their direct connection to medium or high voltage DC grids at the MIMO collecting point is desirable [16]. Also remote rural communities, which are in relative proximity of DC lines would significantly benefit from accessing the power supply through tapping into the DC grid [17].

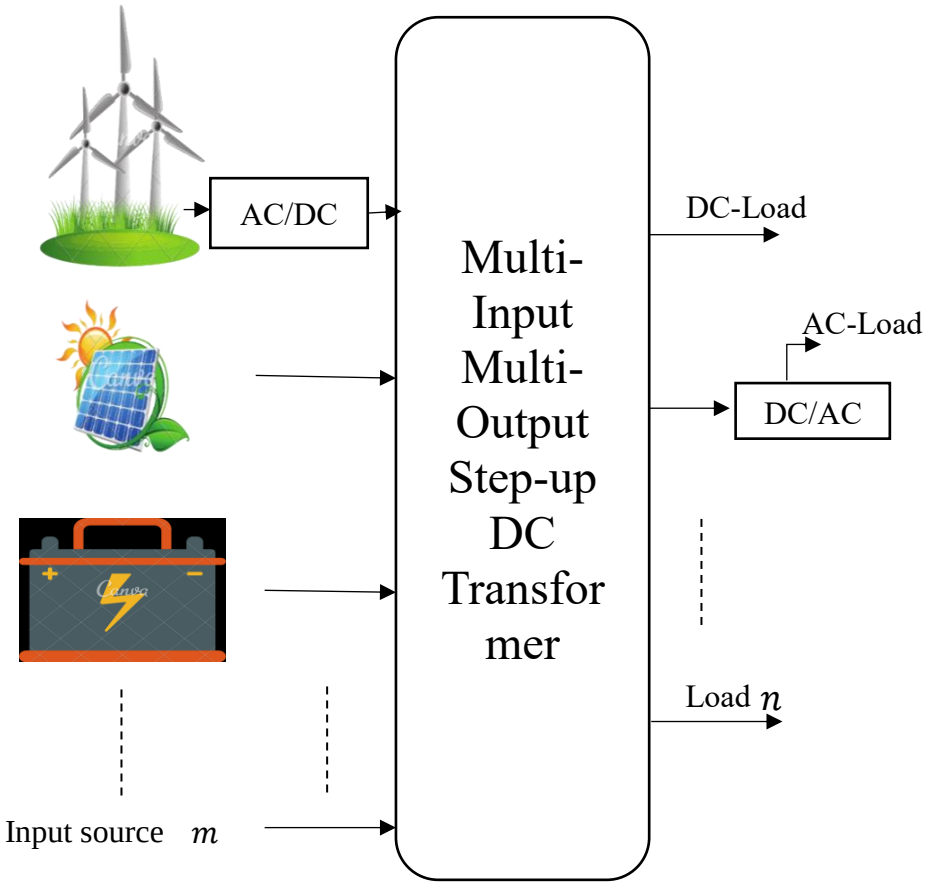


Figure 1.4 the block diagram of MIMO DC transformer technology with different renewable and non-renewable energy sources- Image Credit © Canva [170]

The interfacing of multiple sources to DC collecting points will provide improved reliability and flexibility. Nowadays, such DC collecting points are known as Multi- Input (MI) DC

Converters, having the capability of diversifying different energy sources. To date, most direct DC-DC conversion is based on Single-Input Single-Output (SISO) basic topologies. As most electrical storage and load levelling devices in power systems use a DC type storage media (battery, super capacitor, capacitors, superconducting magnetic energy storage, etc) with widely varying DC voltage levels, their integration into the power grid has, until recently, been difficult.

1.2. Research Objectives

The purpose of this PhD research is to design a Multi-Input Multi-Output (MIMO) step-up DC transformer topology with the advantages of simple configuration, fewer components, and high efficiency compared with the available published topologies. The new topology will encompass high efficiency, high reliability and simple control. The project needs to be developed to a point where a detailed description of the proposed MIMO step-up DC transformer topology, operation principles, theoretical analysis, design criteria and its control strategy are provided. Various strategies for controlling and co-ordinating the source and load sides of the DC transformer, based on closed-loop DC voltage control characteristics, need to be investigated to provide adequate DC voltage regulation and power sharing among the connected sources and loads from the concept of power management control through a dedicated, flexible control algorithm.

The robustness of the designed controller needs to be tested under different scenarios of faults, dynamic change in power demand or supply, and in the availability of the input sources.

The detailed digital simulation of the proposed design on a MATLAB-SIMULINK platform needs to confirm satisfactory operating principles under various scenarios. This will ensure verification of the feasibility of the proposed scheme where a MIMO step-up DC transformer will be highly controllable and flexible since it will be based on power electronics.

The main aims of this project are:

1. The development of optimal topology for high-ratio MIMO DC Transformers or DC substations.
2. The development of a switching algorithm; highly efficient, simple and reliable.
3. The development of reliable and efficient power management control.
4. The development of local control for each terminal of the MIMO DC transformer.
5. The development of a master control for DC voltage regulation within the overall MIMO DC transformer.

1.3. Research Methods

A scientific approach [8] has been used to obtain the aims of this project as shown in figure 1.5. At the beginning of this research work, the relevant subject information was collected using the available sources, including published papers and books. Familiarisation with MATLAB software took place concurrently with the literature survey. Attention has been given to project topology design principles, switching, control algorithms and the process of analysis for the results obtained through simulation with those derived numerically.

For attaining the aims, the project was then divided into two parts. The first part consists of designing a MIMO step-up DC transformer topology for renewable energy sources for medium to high voltage applications, and derivation of the mathematical expressions which describe the output with the input and duty ratio for an ideal and non-ideal DC transformer. This part of the work is presented in chapter four of the thesis.

The second part of this research project consists of the generation of efficient and robust switching signals for cases when demand changes and sources are fixed, or where sources are fixed and demand changes or both demand and the source change. In addition, a study of the system's closed loop controllers' stability and their performance under normal and faulty cases has been undertaken. This part of the work is presented in chapter five of the thesis.

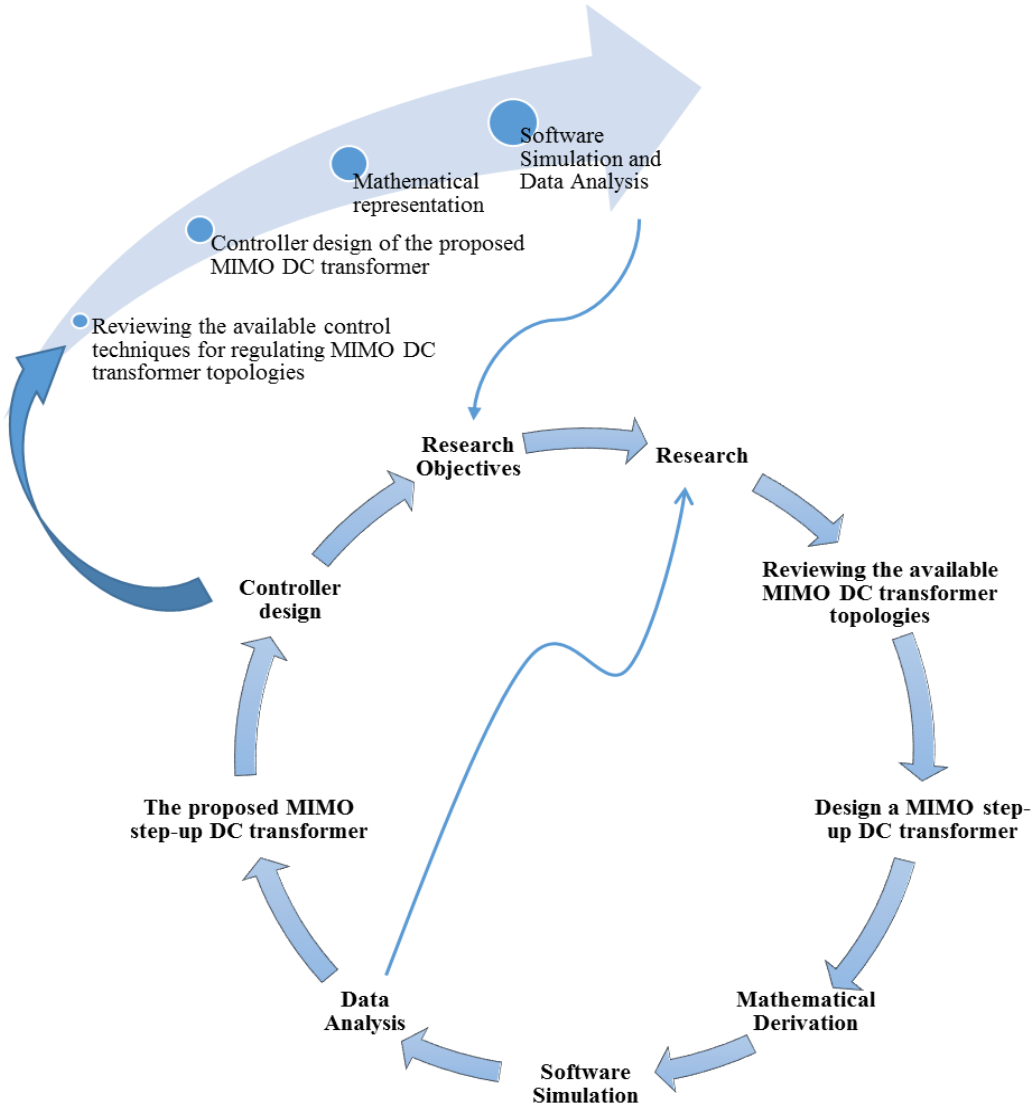


Figure 1.5 the proposed research methodology

1.4. Summary of Contributions

1) A review of the related published papers on DC Transformers and the gathering of the related essential data.
2) The design of a novel Multi-input and Multi-output (MIMO) step-up DC Transformer using insulated gate bipolar transistors in view of an efficient topology in terms of producing a high step-up conversion gain without using an internal AC transformer, reduced switching losses, response of switching speed and minimum use of components.
3) The proposed design is flexible and costly effective. Having a DC hub collection point which is easy to monitor, assemble and effective to distribute the energy.
4) Derive generic expression which consider the Mathematical description of the output with the input, duty ratio of switching rate and other components of circuit topology, considering the operating principle of the proposed DC transformer.

5) Generating mathematically from first principles efficient and robust switching signals for cases when demand changes and sources are fixed, or sources are fixed and demand changes or both demand and the source change. Voltage mode control is used to regulate the output DC voltage.
6) The Construction of the proposed Multi-input and Multi-output step-up DC transformer with its related control algorithm within dedicated software.
7) The Simulation of the constructed MIMO step-up DC transformer in various scenarios for validity of its robustness, efficiency, flexibility and reliability.
8) The evaluation of the proposed MIMO step-up DC transformer whereby comparative analysis has been performed with selected published topologies.

1.5. Thesis Outline

The thesis is structured in seven chapters:

Chapter one presents the motivation of this work and the importance of HVDC technology over HVAC and the role of offshore wind farms in HVDC technology. It also shows the main aims and research objectives with their corresponding methodologies. The research contributions to knowledge have been summarised in this chapter. Finally, it shows the organisation of this thesis.

Chapter two presents a comprehensive literature survey which has been carried out to provide an insight into the design of a novel MIMO step-up DC transformer for high voltage offshore wind farms technology. It also reviews the available control methods and techniques used for regulation of the DC voltage of the DC transformers.

Chapter three discusses the theoretical background of conventional DC transformers which also is known as DC-DC converter topologies. It also presents the operational principles of the basic topologies in continuous and discontinuous conduction modes with their associated mathematical expressions. This chapter shows the reasons for utilising the IGBTs as semiconductor power switches in the proposed design. It also presents the control operation method where Pulse Width Modulation (PWM) has been used in the proposed controller design.

Chapter four presents the proposed MIMO step-up DC transformer design and its operating principle, specifications, theoretical analysis and design criteria. Also provided are the mathematical derivation of inputs and outputs in terms of the passive components and the duty cycle of the power switches. The power losses and efficiency of the proposed MIMO

step-up DC transformer are discussed. Furthermore, for the proposed DC transformer, the optimal operating frequency of utilised power switches is presented. Finally, the main characteristics of the proposed design and the software simulations in steady state condition without a controller are described and presented in this chapter.

Chapter five describes modelling and control algorithms of the proposed MIMO step-up DC transformer. Also shown are the proposed control technique where Proportional Integral Derivative (PID) controllers have been integrated to control the proposed design. The mathematical modelling of the controller design is presented in this chapter and the stability analysis of the proposed MIMO DC transformer is performed through a transfer function approach. Results show the validity of the proposed DC transformer's control performance which is demonstrated through MATLAB-SIMULINK software simulation under different scenarios depending on the utilisation of the input sources. Furthermore, the design of a low pass filter is presented for improvement of the output voltage response curve and also to protect the design from the high voltage spikes which it acquires under specific conditions. Finally, the performance of the proposed MIMO step-up DC transformer under open circuit (across the diodes) and short circuit (across the switches) faults is examined in this chapter and the simulation results are presented.

In chapter six a number of the most recently published MIMO step-up DC transformer topologies with high voltage conversion gain are reviewed. Based on the conversion gain and the boosting techniques used, two different topologies have been selected in order to evaluate the proposed design. Also, the comparative analysis and the performance characteristics of the proposed and the selected topologies under predefined specifications are shown. Finally, the manufacturing cost of the passive components and the semiconductors which used in the proposed and the pre-selected designs are compared and presented in this chapter.

Chapter seven concludes this thesis and summarises the achieved research contributions. Future research directions are presented in this final chapter.

CHAPTER TWO

LITERATURE REVIEW

In this chapter, A comprehensive literature survey will be carried out in order to provide an insight into the design of a novel Multi-Input Multi-output (MIMO) step-up DC transformer for high voltage offshore wind farm technology. Also, a review of the existing DC transformer topologies will be provided and summarised in this chapter to show the novelty of the proposed design.

2.1. MIMO DC Transformers for High Voltage DC Networks

2.1.1. Review of existing DC transformers topologies

DC transformers (or DC-DC converters) have been extensively utilised at low power levels and a number of topologies exist. However, most of these technologies are not suitable for scaling up to megawatt power levels. The limitations are linked to the nature of the switches at the highest power, the operating frequencies, efficiency, switch utilisation, and others. Conventional, unidirectional step-up DC transformers [20] cannot achieve gains larger than $(2-4)$ because of difficulties with the output diode. There have been attempts to develop DC transformers with internal AC transformers [20]-[21] at higher power levels; however, some serious inherent limitations, in terms of stepping ratios and power levels have been demonstrated [22]. Another limitation is with the type of switch, for example, DC transformers utilise Metal–Oxide Semiconductor Field-Effect Transistors (MOSFETs) as switches with around a $10\ kHz$ frequency, which gives low prospects for further increasing to megawatt power levels.

There has been significant research worldwide to develop megawatt sized SISO DC transformers using Insulated Gate Bipolar Transistors (IGBTs), and very promising topologies include a full-bridge converter with a medium frequency AC transformer and resonant topologies [23]. Recent research [24] noted that the Multi-Terminal (MT) DC substation is considerably more complex than two-terminal units and that there is need for more research on design optimisation.

Multiple-Input (MI) and Single Output (SO) DC-DC converters (also known as multi-terminal DC substations) have been shown as useful for combining several energy sources of different power capacity and/or voltage level, to obtain a well-regulated output voltage [25]-[28].

Recently, there has been activity in the design of various topologies with the Multi-Input DC-DC converter with the possibility of Multi-Output (MO) DC transformers for applications such as grid-connected integrated hybrid generation systems, fuel cells, micro-grid-based telecom power systems, uninterruptible power supplies, and electric and hybrid electric vehicles.

The operation modes of a two-input single-output DC-DC step-up converter for small-size wind-photovoltaic generation are analytically studied in terms of voltage ripples for each operation mode in [29]. The converter topology consists of two step-up DC-DC choppers connected in series and tested via computer simulation. A prototype implementation and testing were later presented in [30] by the authors.

In [31] a MISO DC-DC converter for hybrid vehicles is presented and a prototype developed. The converter consists of three step-down /step-up (buck/boost) converters connected in parallel. The inputs of the converter are a fuel cell generator, a battery and an ultra-capacitor. In the same year the construction of a bi-directional DC/DC converter, mainly consisting of an unsymmetrical half-bridge converter, was reported [25]. In this design a transformer provides the galvanic insulation between the low voltage and the high voltage side. The operating principle and the power transfer characteristics are determined analytically and used to design a 1.6 kW prototype.

The MI DC-DC converter topology with minimal parts reported by [27] allows only a unidirectional power flow, which has a negative output voltage.

In [26] two MISO DC-DC transformer topologies are proposed: a buck-boost and a forward type, both with coupled inductors (multi-winding transformer) between the inputs and the output. The buck-boost is studied in detail for a two-input configuration with one input from a solar panel and one from an AC line. The equivalent circuit is constructed for different operation modes and the corresponding transfer function of the converter determined. Theoretical results are confirmed by experiment.

In [32] a step-up/step-down DC-DC converter is presented with a detailed mathematical description of the converter's operation mode. Experimental results are also given. The application of two input DC-DC boost converter topologies that use one less switch for hybrid vehicles is discussed in [34]. Authors also analyse and describe mathematically the operation modes of the converter.

In [35] three new MI DC-DC converter topologies are proposed, and a comparative study conducted between ten different topologies taking into consideration flexibility, reliability and modularity potential for ideal component implementation. As a result of the comparative study it could be found that the multi-input boost buck-boost is the only topology which integrates different inputs, also it could obtain relatively high flexibility.

A bi-directional multi-input one-output DC-DC transformer/converter is presented in [36]. The converter has only one inductor connected to all the inputs. It can operate in boost, buck or buck-boost mode. In boost mode it can have only one input connected. In reverse operation it can charge only one input from the output side. The work focuses on the operation of the MI buck topology. In Discontinuous Conduction Mode (DCM) only one input switch can conduct at a time. Differential equations for the output voltages are determined for different operation scenarios.

The research presented in [33] uses the concept of the zero-volt switching multi-input bidirectional DC-DC converter with a multi-winding transformer as a link between the input and output. When in reversed mode this converter can work with only one input. The concept of the multi-winding transformer is presented in detail with a mathematical description of DC-DC converter operation modes. Simulated current and voltage waveforms are presented for each operating mode, as well as an analysis of the output power from each input source according to the DC-DC converter control variables.

Reference [37] is a short paper explaining the generation of MI converters from their respective SI versions. Based on several assumptions, restrictions, and conditions, the analysis indicates that MI development is feasible. The study uses four rules to identify SI topologies that can be extended into multiple-input circuits. In the same year a duty cycle duration was evaluated for a Single-Ended Primary Inductance Converter (SEPIC) type of MI DC-DC convertor dedicated for Photovoltaic (PV) modules considering the same triggering time. Where a new SEPIC topology is proposed with two coupled inductors (transformer) to obtain the Maximum Power Point (MPP) on each input cell. The duty cycle of one input cell is dependent on the duty cycle of all the other inputs which limits the duty cycle of each input.

A four-port DC-DC converter topology derived from a half-bridge configuration is presented in [39] for a solar-wind combined energy generation system. A transformer links the output of the system to the input sources. The DC-DC converter topology capable of interfacing four DC power ports: two input source ports, a bidirectional storage port, and a galvanically

isolated loading por. The different operation modes of the converter are analysed and presented in detail. The control system of the converter consists of three feedback controllers: a Solar Voltage Regulator (SVR), a Wind Voltage Regulator (WVR) and global Output Voltage Regulator (OVR). For the proper design of SVR, WVR and OVR a dynamic model in the case of a small signal perturbation is developed.

A comprehensive study of two bidirectional DC-DC converter topologies presented in [40] for tapping into HVDC from a medium AC voltage level without AC transformers. The proposed topologies are single-input single-output which can work with line commutated converters or voltage source converters used on the AC/DC side. Basic PI control systems are used for the presented topologies. Possible control limitations are analysed and PSCAD simulations are made for tapping into the $1000\ MW$ HVDC CIGRE benchmark network.

(T. Preti, et al) have designed a high gain DC transformer with a coupling inductor, designed to boost low voltages to voltages into a high range of 30 to 50 times Input voltage with the help of a PI controller [41]. To achieve high voltage output gain, the converter output terminal and boost output terminal are connected in series with the isolated inductor with less voltage stress on the controlled power switch and power diodes.

A proposed MI step-up DC transformer which draws power from several input sources has been simulated in [42]. This Multi-Input Converter (MIC) can deliver power from all the input sources to the load, either individually or simultaneously. The MIC reduces the system size and cost by reducing the number of components. Three different operation modes are discussed, and a PI controller is used for the closed loop performance of the MIC.

A MISO isolated three-level DC transformer presented in [43] with a transformer links the output of the system to the input sources. The architecture eliminates two boost switches which are present in the two-stage counterpart. A low voltage prototype has been designed to serve as a proof of a concept.

Several solutions have been presented for increasing the voltage gain of the step-up DC transformers, such as coupled inductors [47], switched capacitors [48], and multi-stage converters [49]. Utilisation of coupled inductors increases the voltage gain, but the structure becomes complex and bulky. Also, the voltage spikes originating from leakage inductance at higher output powers and large current ripples of low voltage side, are shortcomings of coupled inductor-based topologies [47]. Switched capacitor-based topologies have rather simple structures but usually utilize significant number of capacitors and switches to reach higher voltage gains. However, this increases the switching losses and current stress of

switches and consequently reduces the converter efficiency [48]. In [49] an MI high step-up boost converter has been presented which has been made up of n conventional boost converters which increases the voltage gain by n times.

The study in [50] has achieved a high voltage gain with continuous input current and a simple control circuit. But large switch voltage stress becomes one concern. The study in [51] and [52] proposes an effective topology that can achieve high voltage gains without high duty-cycle by cascading several voltage multiplier cells, whereas the high output voltage is achieved through lifting capacitor voltage step by step. This leads to a high voltage stress of the capacitors which increase the size and cost of the DC transformers.

It is obvious that a step-up DC transformer is one of the most interesting designs for applications of boosting and regulating the low and variable output voltage of renewable energy for the DC link of grid connected systems [44]– [46]. Therefore, in the following sections a review of the existing step-up DC transformer topologies has been summarised and tabulated based on the operating power level, stepping gain and the number of inputs and outputs. In addition, the most recently published high gain non-isolated step-up DC transformer topologies have been reviewed and summarised in chapter six of this thesis.

2.1.1.1.Single-Input Single-Output step-up DC transformers

Table 2.1 sets out the SISO step-up DC transformer topologies. Some of these topologies are designed with a high conversion gain without using an internal AC transformer [54], [55] whereas the models in [57] and [58] used an AC transformer to obtain high step-up conversion gain by changing the transformer's turn ratio. High conversion gain DC transformers are useful for high voltage DC applications thus MI configurations have been provided as a solution to increase the voltage gain by integrating different input sources. In section 2.2.1.2 a number of MISO step-up DC transformer topologies have been presented in [42], [29], [34], [33] and [60] as illustrated in table 2.2.

Table 2.1 review of the existing published SISO Step-up DC transformer topologies

Reference number of Presented Topology	Title	Year	Number of inputs and outputs	Relation between the input and the output voltage	Switching algorithm	Applications
[53]	Design high gain DC-DC boost converter with coupling inductor.	2014	Single-input Single-output	The relation is not included	Only one switch switching with specific duty ratio	Low voltage applications (fuel, solar energy system)
[54]	A high voltage ratio and low stress DC/DC converter with reduced input current ripple for fuel cell source	2014	Single-input Single-output	$V_o = \frac{2}{1-D} V_i$	The switch and the diode switched simultaneously	High voltage transfer gain (renewable energy systems, fuel cell)
[55]	High voltage gain interleaved DC boost converter application for photovoltaic generation system	2012	Single-input Single-output	$V_o = \frac{1+D}{1-D} V_i$	Only one switch operating by controlling the switching period	photovoltaic generation system
[56]	Hybrid switched inductor converters for high step-up conversion	2014	Single-input Single-output	$V_o = \frac{1+2D}{1-D} V_i$	Two switches operated simultaneously	Fuel cell applications

[57]	A novel high step-up DC/DC converter based on integration coupled inductors and switched-capacitors techniques for renewable energy applications	2015	Single-input Single-output	$V_o = \frac{2+n+nD}{1-D} V_i$ Where n is the transformer's turn ratio	Only one switch operating by controlling the switching period for the switch and the diodes	Renewable energy sources
[58]	Experimental evaluation of soft-switching DC/DC converter for fuel cell vehicle applications	2002	Single-input Single-output	$V_o = \frac{n}{1-D} V_i$ Where $n = \frac{N_s}{N_p}$	For one input there are four switches. And every two switches switching simultaneously	Fuel cell powered electric vehicle
[59]	Design of a non-inverting synchronous Buck-Boost DC/DC power convert with moderate power level	2009	Single-input Single-output	$V_o = \frac{D}{1-D} V_i$	Q_1,Q_3 works as a group and Q_2,Q_4 works as another group	Solar system applications

2.1.1.2.Multi-Input Multi-Output step-up DC transformers

MI [42], [29], [34], [33], [65], [66], [36] and [60] and MO [62]-[64], [67], [27] and [68] step-up DC transformer topologies have been presented with different numbers of passive components and semiconductors. And again, some of these topologies used an internal AC transformer in order to have a high conversion gain. For different number of inputs and outputs, the number of power switches have been used to increase the voltage level by adjusting the switches' duty cycle value.

In [60] high conversion gain is obtained which is suitable for high voltage applications. But in this design utilising a high number of power switches will increase the switching losses

as well as the size and the weight of the DC transformer. Also, the internal AC transformer makes the design bulky and costly.

While in [62] a SIMO step-up DC transformer topology has been presented which is suitable for low and high voltage applications, the drawback of this design is that the power switches operate sequentially which means they cannot be active at the same time and thus the power is delivered just one load at a time.

In [63] a MIMO step-up DC transformer for electric vehicle applications has been presented. For m inputs and n outputs there are $(m + n + 2)$ power switches used, and this increases the size, weight and cost as well as the losses of the system. Furthermore, in this design the inputs are connected in parallel, thus the input power switches can operate simultaneously if all input sources are identical. Otherwise only one input at a time could be connected to the system.

Most of the available published step-up DC transformer topologies which provide a high conversion gain utilise an internal AC transformer. Therefore, in the next section a comparison between the MIMO topologies with and without internal AC transformer is examined.

Table 2.2 review of the existing published MIMO Step-up DC transformer topologies

Presented Topology	Title	Year	Number of inputs and outputs	Relation between the input and the output voltage	Switching algorithm	Applications
[60]	A multiple-input DC/DC converter for renewable energy system	2005	Multiple-input Single-output	$V_o = \frac{n}{1-D} V_i$ Where $n = \frac{N_s}{N_p}$	For tow inputs there are four switches operated simultaneously	High voltage applications
[42]	Modelling of multi-input DC/DC converter for renewable energy sources	2014	Double-input Single-output with storage element	$V_o = \frac{1}{1-D}(V_1 + V_2)$	Boosting switches operated simultaneously and sequentially with the storage element switches	Renewable energy sources (wind, solar)
[29]	Testing of a new DC/DC converter topology for integrated wind-photovoltaic generating system	1993	Double-input Single-output	The relation is not included	Two switches operated simultaneously	Photovoltaic-wind generating system
[34]	New DC/DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles	2007	Double-input Single-output	$V_o = \frac{1}{1-D_1} V_1 \quad + \cdots \frac{1}{1-D_2} V_2 \quad + \cdots \frac{1}{(D_1+D_2)-1} V_3$	Three switches cannot be active at the same time	Fuel cell vehicles
[33]	A ZVS bi-directional DC/DC converter for multiple energy storage elements	2005	Double-input Single-output with storage element	The relation is not included	Six switches Switched simultaneously	Hybrid electric vehicles

[62]	Multi-output DC/DC converters based on diode-clamped converters configuration: topology and control strategy	2008	Single-input Multi-output	The relation is not included	The switches operated sequentially then deliver the power to just one load at a time	Low and high-power applications
[63]	A Non-isolated multi-input multi-output DC/DC boost converter for electric vehicle applications	2014	Multi-input Multi-output	The relation is not included	The switches operated simultaneously	Electric vehicle
[64]	Multi-output buck-boost converter with enhanced dynamic response to load and input voltage changes	2010	Single-input Multi-output	The relation is not included	For n outputs $n+1$ switches operated simultaneously	Multi voltage DC networks or multi-level inverters
[65]	Design of multiple-input power converter for hybrid vehicles	2005	Multi-input Single-output	The relation is not included	For n inputs the n switches operated in complementary way, then one input source will be connected at a time	Electric vehicles

[66]	Characteristics of the multiple-input DC/DC converter	1993	Multi-input Single-output	$V_o = (\frac{V_1 t_{ON1}}{N_1 t_{OFF}} + \frac{V_2 t_{ON2}}{N_2 t_{OFF}}) / (1 + \frac{r{T_s}^2}{R t_{OFF}})$	For n inputs the n switches operated in complementary way, then one input source will be connected at a time	Renewable energy sources
[67]	A single-inductor multiple output switcher with simultaneous buck, boost and inverted output	2011	Single-input Triple-output and can be extended to generate $n-$outputs	The relation is not included	For n outputs there are $(n+1)$ switches operated individually. When the input switch is ON all the other switches are OFF once the input switch OFF then the output switches will be ON sequentially	LED back light LCD monitor
[68]	A new DC/DC converter with multi output topology and control strategies	2008	Single-input Multi-output	$V_o=(DR\sum_{j=K}^{n} Dj) / (\sum_{K=1}^{n}\left[R\left(\sum_{j=K}^{n} Dj\right)^2\right])$	The switches operated simultaneously with limitations on some switching states	To supply multi-level inverters
[27]	A multiple-input DC/DC converter topology	2003	Multiple - input Single - output and Multiple - input Multiple - output could be constructed)	For Two inputs If $D_1 > D_2$ $V_o = \frac{D_1}{1-D_1} V_1$ If $D_2 > D_1$ $V_o = \frac{D_1 V_1 + (D_2 - D_1)}{1-D_2} V_1$	The switches operated simultaneously	Hybrid energy system

[36]	A multiple-input DC/DC converter topology	2008	Multi-input Single-output	$V_o = \frac{1}{1-D_1} V_1$	For Boost: possible only with one input voltage at a time	Hybrid electric vehicles

2.1.2. Isolated and non-isolated step-up DC transformer topologies

DC transformer topologies, as illustrated before, can be categorized as MISO [60], [33], [34], [36], [69]– [71], SIMO [72]– [76], or MIMO [63], [77]– [88] configurations. Under each category, two general configurations can be found in the literature: isolated (inputs and outputs are coupling magnetically) and non-isolated (inputs and outputs are coupling electrically) topologies. In fully isolated configurations, all ports of the DC transformer are isolated through a multi-winding transformer as noted in such MISO [58], SIMO [63], and MIMO topologies [77]– [79]. For applications that do not require isolation, non-isolated configurations can be both less costly and complex by providing a transformer-less solution as noted in such MISO [36], [71], SIMO [73]– [75], and MIMO [77], [81]– [86] topologies.

The MIMO topologies proposed in [77], [82]– [84], and [85] utilize one inductive element to transfer energy between sources and loads. While the use of one inductor results in lower magnetic volume and weight, it comes at a cost of pulsating input and output currents as source and load multiplexing are required (i.e., time sharing of the single inductor) [89]. This results in lower component utilization and increased source and load filtering requirements. In addition, due to their unidirectional structure, these topologies are not suitable for energy storage applications.

In isolated MI DC transformers, a high-frequency transformer is used to make electric isolation [90]. A high frequency AC transformer provides electric isolation and impedance matching between two sides of a DC transformer. In general, isolated DC transformers use leakage inductance as energy storage for transferring power between the input and output. Usually isolated DC transformers, in addition to high frequency AC transformer, have a high frequency inverter and rectifier. The power flow between input and output sides is controlled by adjusting the phase shift angle between primary and secondary voltages of transformer [91], [92]. Due to using an internal AC transformer, isolated DC transformers are heavy and massive. These DC transformers require inverters in input sides of an AC transformer for conversion of input DC voltage to AC and also need rectifiers in outputs of an AC transformer for conversion of AC voltage to DC. Therefore, in all input and output terminals

of these DC transformers, several switches are applied which leads to an increase of cost and losses. In addition, extending the isolated topologies to MIMO configuration by adding additional windings or internal AC transformers in an isolated SISO DC transformer such as in [93]-[96] will increase size and weight of the design, also the regulation is poor such that load variation of one output affects other output voltages.

In [97], an isolated multi-port bidirectional DC transformer has been presented. Using an AC transformer in this structure results in the limited switching for high frequencies, high losses, complicated structures, high size, and high costs. The two-input full bridge boost DC-DC converter presented in [98] benefits from a multi-winding transformer with different type of windings in primary and secondary sides. Other features of this structure are low input current ripple, separate controllers for each one of the inputs, and the possibility of expanding it to n inputs. Nevertheless, by increasing the inputs, the number of the AC transformer windings, the complexity of these winding arrays, the number of switches and input inductors also increase [99]. Therefore, non-isolated high step-up DC transformers are employed to achieve high efficiency and low cost.

Figure 2.1 depicts the advantages and disadvantages of DC transformer topologies as mentioned in [100].

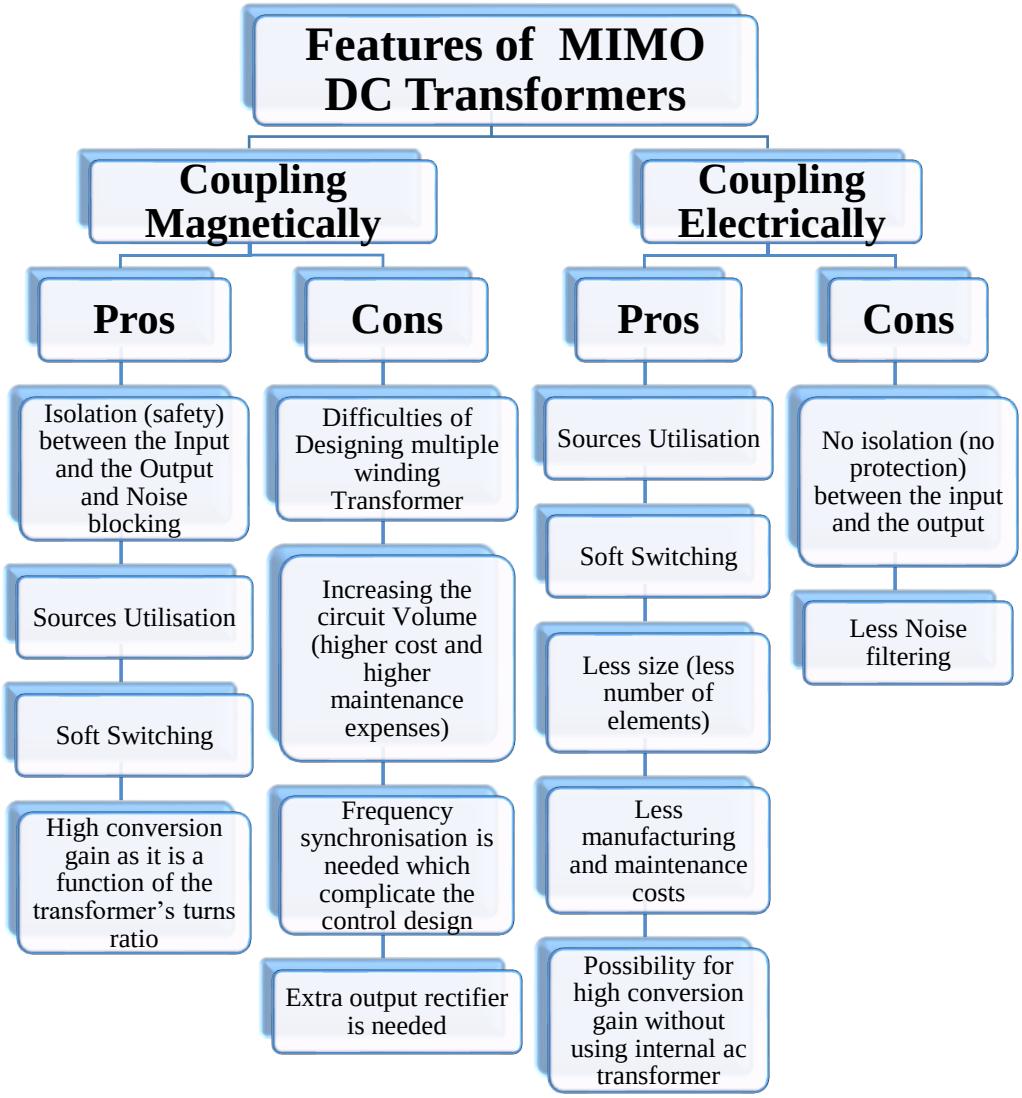


Figure 2.1 comparison between the isolated and non-isolated MIMO DC transformer designs as reported in [100]

Because of the drawbacks of isolated MIMO DC transformers as shown in figure 2.1, usage of non-isolated MIMO DC transformers seems to be more useful [90]. In [81], a MI DC transformer with just one inductor is proposed which can distribute load power between input sources. Also, transferring power between sources is possible.

A non-isolated step-up DC transformer topology with high step-up voltage gain is modelled in [101], so the voltage stress and current stress on the power switches can be reduced; however, the voltage conversion ratio is usually lower than 5. In [102], a triple input structure for hybridization of battery, photovoltaic cells, and fuel cell is introduced by the author. By proper switching of the converter the charge and discharge of the battery by means of other sources and load is possible, respectively. In [62] and [103], a single inductor MI DC transformer is proposed which can generate several different voltage levels in its outputs. The design is controlled to regulate the output voltages at their desired values

despite the load power variation or input voltage variation. But by this design only one output can be provided. For the applications which require more than one output from several input sources there is one way to solve this problem which is by using MIMO DC transformers. In [104] and [105], a non-isolated MIMO DC transformer is introduced which has just one inductor. Using of large number of switches is a drawback of this design which caused low efficiency. Also, the impossibility of energy transferring between input sources is another disadvantage of the proposed design. In [86], a non-isolated MIMO topology capable of DC–DC and DC–AC conversion is proposed, although this topology is limited to only one load port and one energy storage port.

In [62] a MO step-up DC transformer has been presented, where its outputs are connected in series, and are used in high power and low power applications. In this structure for n outputs, $n + 1$ switches are needed, and also the controller system is complicated where a voltage control with hysteresis current control loop is used. In [76], a SIMO DC transformer with high efficiency and bidirectional power flow capability is presented. This structure has the ability of performing in both step-down and step-up modes. Complexity and big size are the main drawbacks of this design. In [84] a single stage MIMO DC transformer has been presented. This structure uses many switches, in which for n input and m output topology, $n + m$ switches are utilised, which makes the structure very complex. In this structure by increasing the number of the input energy sources and output loads, the share of each energy source for supplying the output loads decreases. In [106] a MIMO DC transformer has been presented which is suitable for micro grid applications. In this structure by increasing the output loads, the input voltage sources also increase as well as inductors and switches. In addition, for n input m output mode, there are m^2 of switches, m inductors and m DC voltage sources. According to this a high count of parts, high losses, big size, heavy weight, and more complicated structure have been obtained by this design.

From the DC transformer topologies which are available in the literature it can be summarised that in order to design a step-up DC transformer for medium to high voltage applications utilising renewable energy sources such as wind turbines, a MIMO configuration with high step-up conversion gain without using internal AC transformer is needed. This can be used to obtain different output voltage levels from several power sources. MIMO DC transformers provide flexibility in terms of the choice and the availability of the power source, reduction in the number of power lines to transfer power to pre-specified locations as well as enhancement in system reliability.

2.2. DC Transformers Control Methods

DC transformers convert electrical energy from one level of voltage and current to another using power switching components. The input of the DC transformer is an unregulated DC voltage which produces a regulated output voltage having a magnitude that differs from the DC input voltage by changing the duty cycle of the power switches. Thus, due to the nature of power switches, the DC transformers are nonlinear systems which represent a big challenge for control design [29]. Fixed frequency Pulse Width Modulation (PWM) is the most used closed loop method to control switching power supplies and is used to design a controller with a high degree of dynamic response which is required in nonlinear systems [30].

A DC transformer is a voltage regulator so; in such applications, it must provide a fixed DC output voltage under input and load variations. There is much previous research which focuses on DC transformers and its associated control design. Due to the nonlinearity of the DC transformers; when designing a closed loop with classical (linear) control methods, a linearization of the plant is required. The mathematical representation of the plant to be controlled could be represented in a dynamic model of the switching DC transformer in order to obtain a Small Signal Model (SSM) [55].

When a DC transformer is employed in open loop mode, it exhibits poor voltage regulation and unsatisfactory dynamic response, and hence, this DC transformer is provided with closed loop control for output voltage regulation. Various closed loop control systems have been proposed such as a Proportional Integral Derivative (PID) controller as a linear control method, fuzzy logic and sliding mode control and other methods, as well as many other researchers presenting a new designs to be controlled with appropriate control technique such as [31] using soft switching technique, and [96] a method for high frequency power switches design using a fixed frequency switching strategy.

The investigation of different analogue and digital control methods for DC transformers is not new and several works are available up to now. As in [39] various types of digital control methods are studied, and the advantages/ disadvantages of each method have been stated. In general, digital control methods are gaining popularity in the automotive industry applications due to their accuracy, flexibility and robustness. In contrast, digital controllers are more expensive than analogue controllers and additional components are needed such as Analogue/Digital (A/D) and Digital/ Analogue (D/A) converters.

In controlling the DC transformers, a Voltage Mode Control (VMC) or Current Mode Control (CMC) are the most popular principles for regulating the output voltage. VMC and CMC could be applied simply by closing the feedback loop between the required output voltages and switching device duty ratio signal [27]. The VMC and CMC will be analysed in sections 2.2.1 and 2.2.2 respectively.

2.2.1. Voltage Mode Control Method

In the voltage regulation method there is only a single voltage feedback loop as shown in figure 2.2. In this method the output of the DC transformer is measured and compared with a reference voltage and then the differential compared value is used to produce a PWM signal to control the DC transformer's power switch duty cycle d . The duty cycle value will control the average voltage across the inductor in the DC transformer thus the output voltage will remain constant without any variation. In addition, this method is used to control the DC transformer topology in two modes Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). As in [40] the voltage feedback control method has been used to produce a constant output voltage. And a microcontroller is used to produce a set of PWM signals. The controller adapts as the input voltage varies whilst it requires additional effort to take variations of the load into consideration.

The VMC method is used in research as well as in industry due to its easy implementation [107]. Another advantage of using the VMC method is the large sawtooth waveform which provides a good noise margin for a stable modulation process, as well as by using accurate voltage sensors such as a Complementary Metal Oxide Semiconductor (CMOS) sensor which is easy to design and nearly lossless this will improve the efficiency of the DC transformer [108].

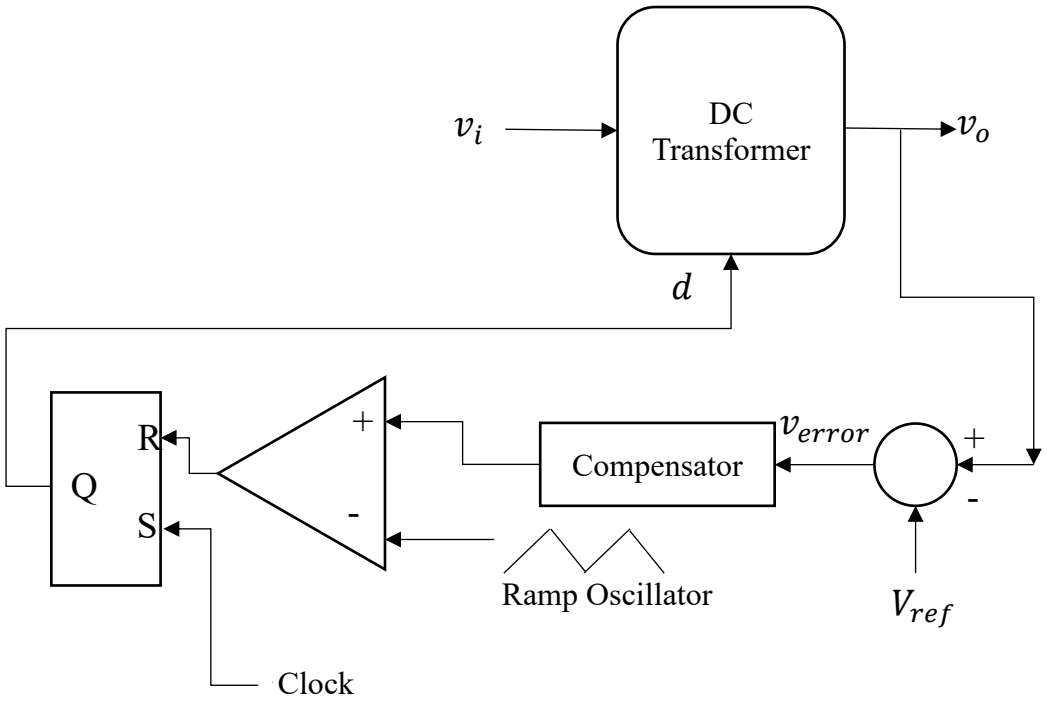


Figure 2.2 voltage mode control of DC transformer [107]

The disadvantage of using the VMC method in regulating DC transformers is that it provides a slower transient response [108]. When any changes occur in the input voltage or on the load side, this will be denoted as output voltage changes which will be sensed and then corrected by the feedback loop. In such applications it exhibits poor reliability and stability of the power switch [107].

2.2.2. Current Mode Control Method

In this method as shown in figure 2.3 there are two control loops: voltage and current control loops, so the CMC method is more complex than the VMC method as the additional loop in the CMC method is used to control the inductor's current and then regulate the output voltage indirectly [32]. After sensing the inductor's current, it will be compared to the control signal which is the difference between the output and reference voltage. By comparing the inductor's current with the control signal the duty cycle d of a particular frequency will be generated to derive the switch of the DC transformer.

There are several current mode control strategies which have been proposed in the literature [42]. Since instantaneous changes in the input voltage are immediately reflected in the inductor current, there are various current sensing techniques available in literature as CMC provides an excellent line transient response and the sensed current is used to determine when to switch between CCM and DCM thus, improving the efficiency of the power DC transformers in specific applications [41]. In the same paper [41] the author reviewed six

current sensing techniques used in current mode control and all those techniques need extra components for sensing the inductor current, for example adding sensing resistance in series with the inductor. This incurs power losses in the DC transformer and therefore reduces the DC transformer's efficiency.

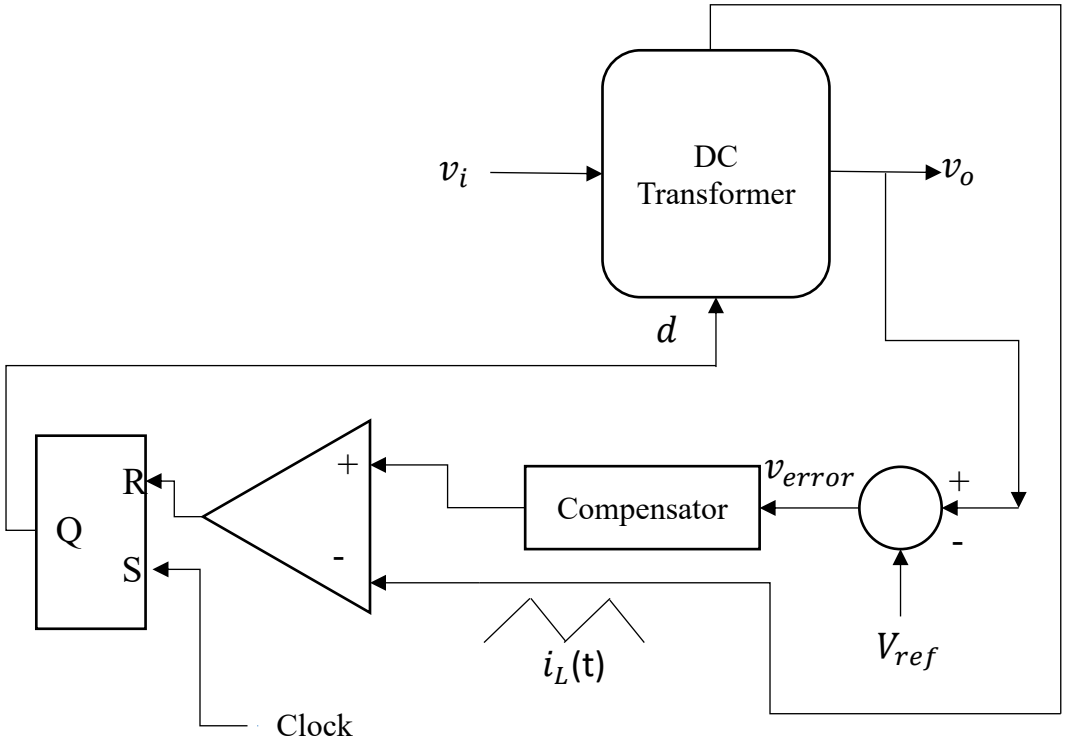


Figure 2.3 current mode control of DC transformer [107]

The advantage of using the CMC method is that the transient response will be improved with a good performance in line regulation. And the main switch gains more protection by limiting the inductor's current [107]. While it is a very unstable control loop when the duty cycle value exceeded 50% therefore it is not appropriate for control of the step-up DC transformers where the duty cycle value should be more than 50%. Also having two control loops will make the circuit more complicated and more difficult to analyse. Since the control modulation is based on a signal derived from the output current, oscillations in the power stage can insert noise into the control loop [108] which will be another drawback of CMC method. Furthermore, due to the nonlinearity of the CMC dynamics the SSM is difficult to achieve, also the additional inner feedback loop and the extra components and sensors which are needed in the CMC method will make the CMC method more complex to implement than the VMC method as well as costlier.

Therefore, research has been done where the DC transformers have been controlled by linear VMC methods and these controllers offer advantages such as fixed switching frequencies, zero steady state error and give a better small signal performance [38]. Consequently, the

linear classical controller will be discussed in detail in this thesis as this technique has already been successfully used to control the proposed MIMO step-up DC transformer.

2.2.3. Linear (Classical) Control Technique

PID control is one of the oldest and most popular control techniques used for DC transformers [109], [110]. As shown in figure 2.4 the schematic diagram of the PID controller, there are different families P, PI, PD and PID could be used in controlling the DC transformers. These different combinations will give various ways to regulate the DC power supply in DC transformers.

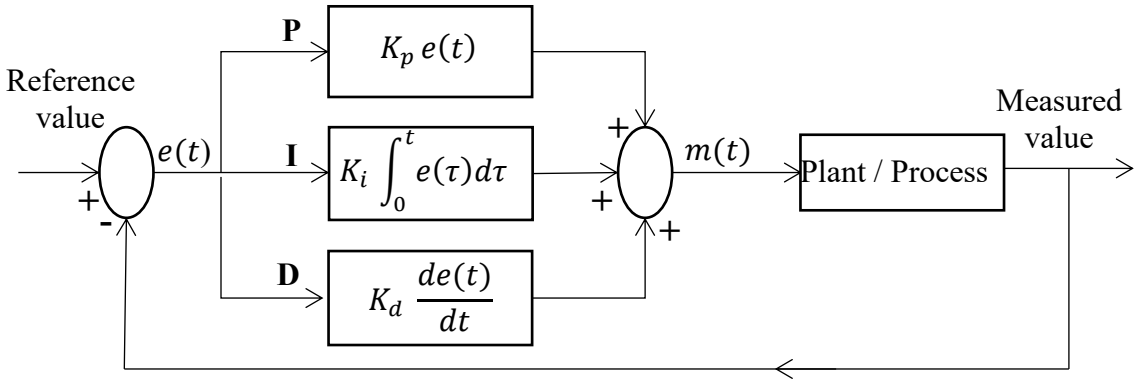


Figure 2.4 block diagram of a PID controller in a feedback loop

The PID control signal is formulated as follows:

$$m(t) = K_p\, e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \qquad (2.1)$$

Where $m(t)$ is the control variable and $e(t)$ is the error signal over time.

A PID controller calculates an error value as the difference between the measured and the desired reference value [24], [34]. So, the PID controller must adjust three parameters K_p, K_i and K_d of the system which would affect the transient response, rise time, settling time, steady state error, overshoot and stability. Thus, it is not necessary for the system to adjust the three actions P, I and D and it may use only one or two actions to improve the system dynamic response. Here, K_p is a gain adjustment acting on error signal and the integral gain K_i adjusts the accuracy of the plant, while K_d adjusts the damping of the plant [21]. Thus, before using a PID controller, the mathematical modelling of the plant to be controlled must be created, in contrast to intelligent (non-linear) control systems which do not need this mathematical model.

A PID controller design procedure should include the mathematical modelling of the plant as well as the way of finding the PID parameters (K_p,K_i, K_d) which is called as PID tuning. PID parameters tuning is a core part of the controller design [47]. Many PID tuning methods had been derived to determine the value of the three parameters to obtain a controller with good performance and robustness [47] such as manual tuning method and Ziegler-Nichols (Z-N) method and these methods require retuning the parameters by trial and error to improve the controller performance. There are more advanced tuning methods to improve the performance and these need more computational processing and more information of the plant dynamics [115].

The choice of the tuning method should be based on the characteristics of the plant and performance requirement [47]. As a result, a method which is easy to use with simple formulae is always in demand if the desired performance is obtained [48]. The methods of trial and error, and Z-N have had a strong impact on the practice of control due to the simplicity in tuning the PID for designers as well as for the users with good performance and robustness [49], [107].

The PID controller is a popular control feedback used in industry due to its flexibility and easy implementation in real applications [23]. Furthermore, if the system is complex, the PID can be designed to track an error and assume the system as a black box. PID controller design requires a mathematical modelling of the plant which means that the output voltage derivative is replaced with information about the capacitor current thus reducing noise injection [35]. In [36] the performance comparison of the controller designed for DC transformer is made in terms of peak overshoot, rise time and robustness to load /input variations and it can be concluded that the PID controller obtained 0.009% overshoot peak while, 13.78% was obtained with a fuzzy logic controller, and the response of Z-N PID controller for input/load variation has a good performance proving that PID adapts through this research.

In [42] a Proportional Integral (PI) controller has been designed and implemented for a step-up DC transformer using a real time interface and the results show that fast transient response and stability of the system can be achieved using a PI controller by adjusting the values of K_p and K_i. Also, in [111] the proposed PID closed loop implementation of the step-up DC transformer maintains constant output voltage despite changes in input voltage and significantly reduces overshoot thereby improving the efficiency of the conventional step-up DC transformer. Furthermore, [112] analysed two different methods of tuning a PI

controller with step-up DC transformer, Z-N method and loop shaping method. And from the comparison results a conclusion can be made that the loop shaping method gives a better response than the Z-N method for the proposed model.

Although several MI DC transformer topologies have been presented for renewable energy system applications, only a few papers have mentioned the control techniques to control those DC transformers in different operating conditions [113]. Furthermore, the control strategy of the MI step-up DC transformer is presented to regulate the output voltage at the desired level. The PI controllers for the voltage and current loops have been designed for this case. PID controllers are useful for MI configurations such as in [33] where the concept of the Zero Voltage Switching (ZVS) MI bidirectional DC transformer with a multi-winding transformer is used as a link between the input and output. The firing pulse generation logic and PI control of the DC transformer are also presented.

2.2.4. Non-linear (Intelligent) Control Technique

In an intelligent control approach, it is not necessary to extract the internal dynamics of the plant to be controlled as the intelligent control system models the plant. An intelligent control system approach is enough in cases where the plant is too complex to be modelled [21].

The distinction between classical and intelligent control techniques is that an intelligent control method is used for a system that does not have to be mathematically modelled. Thus, different methods such as sliding mode control, fuzzy logic control [25], artificial neural networks [26], genetic programming [27] and others have been proposed in intelligent control as solutions to different control problems due to the complexity of the plant to be controlled.

In general, the intelligent control methods depend on learning the input-output behaviour of the plant to be controlled, for example fuzzy logic control is based on the idea that the human reasoning is approximate, non-quantitative, and non-binary [21]. Fuzzy logic control and sliding mode control as non-linear control techniques have been used in research to control the DC transformers. These two techniques will be discussed in sections 2.2.4.1 and 2.2.4.2 respectively.

2.2.4.1.Fuzzy Logic Control Technique

A fuzzy logic controller is a digital approach which is non-linear and adaptive, and it is a practical alternative for a variety of control applications [107]. To apply fuzzy logic control to the plant as mentioned in [21] firstly the designer should define the inputs of the system

and its outputs as variables. Secondly, for each variable, there is a subset interval. For example, the velocity has three subset intervals: low, medium and high. Third, choose the shape of the membership functions between the various subsets as to whether they are changing linearly or not. After that the rules determine how the combinations of the inputs obtain the outputs. Since, the rules are non-exact some adjustments are needed for optimal control performance.

In general, the process to apply fuzzy logic control to the plant would be summarised in the following five steps:

1. Define the input and output variables in the system to be controlled.
2. Define the subsets' intervals.
3. Choose the membership functions.
4. Set the IF-THEN rules.
5. Perform calculations and adjusts rules.

Fuzzy logic controllers have become increasingly popular in designing converter control models because they have an advantage over the traditional controller by reducing the dependence on the mathematical model [114]. In addition, their low cost implementations are based on cheap sensors, and the possibility of upgrading the system easily by adding new rules to improve performance or add new features will make it more useful in control systems [107]. The performance of a fuzzy logic controller depends on the rule basis, number of rules and membership functions. These variables are determined by a trial and error procedure, which is time consuming [114]. To solve this problem, different optimization methods have been suggested in literature.

Each control method has advantages and drawbacks in controlling the parameters of DC transformers as there are large number of proposed topologies for DC transformers in literature and in some applications using one of the available control methods may not be sufficient to reach the desired level of the controller's robustness, so a mix of at least two different methods to improve the control performance could be used as presented in [28] and [37]. As the fuzzy control can be used for the improvement of traditional controller systems then in recent research a combination of PID controller families with fuzzy logic have been presented [107] which provide a robust performance under parameter variation and load disturbances, as well as increasing the range of operating conditions which can be operated

with noise and disturbance natures. In [37] is presented implementation and simulation with MATLAB/SIMULINK of a fuzzy logic controller for a three-input bi-directional DC transformer with PI controllers which are connected to the fuzzy logic control output values which are used to regulate the duty ratios that govern the DC transformer.

2.2.4.2.Sliding Mode Control Technique

A sliding mode controller is a type of non-linear controller with a unique feature where the ideal sliding mode control technique operates at infinite switching frequency. Whilst in practice, sliding mode controllers are operated at finite switching frequencies [107]. The technique is employed and adapted for controlling variable structured systems [107]. Sliding mode control methods are well suited to DC transformers as they are inherently variable structure systems. These controllers are robust concerning DC transformer parameter and load variations. However, sliding mode controlled DC transformers generally suffer from switching frequency variation when the input voltage and output load are varied. Therefore, sliding mode controllers are troublesome in the design of the input and output filters [38].

Using the sliding mode controllers with DC transformers show a good stability for large line and load variation and fast dynamic response. In contrast, as mentioned before the controlled DC transformers suffer from the switching frequency variation. Also, these controllers are not available in Integrated Circuit (IC) forms for their power electronic applications, and there is no systematic procedure available for the design of sliding mode controllers [107].

Many control techniques are used where the simple and low cost controller structure is always in demand for most industrial and high performance applications [20], thus classical control systems are preferred by many designers. Hence when classical control can be used in controlling a system to a high performance, then it is preferable to use such as control approach. Intelligent control systems are used particularly for highly non-linear systems; where a system model is difficult or impossible to obtain; and when classical control methods fail to control the system [21]. Even some intelligent control techniques are incapable of handling non-linear systems and system uncertainties whereas classical techniques have evolved substantially over the past decades [51].

2.3. Summary

A comprehensive literature survey has been carried out in order to provide an insight into the design of a novel Multi-Input Multi-output (MIMO) step-up DC transformer for high voltage offshore wind farm technology. A review of the existing DC transformer topologies including Single-Input Single-Output (SISO) and MIMO topologies have been provided and

summarised. Isolated and non-isolated DC transformer topologies have been studied and the advantages as well as the drawbacks of each configuration have been provided.

Furthermore, a review of the available control methods and techniques for regulating SISO DC transformers have been provided. On the contrary there are only a few papers which have mentioned the control techniques to regulate the MIMO DC transformers in different operating conditions.

From the conducted literature review it can be found that there is a great demand in designing MIMO step-up DC transformers for high voltage renewable energy sources. As there are many challenges facing the researches in order to design high step-up conversion gain DC transformers without using an internal AC transformers. As well as to design an efficient, financially viable DC transformer with a smaller size and weight. In addition to ensure the system flexibility and reliability the control strategies to control MIMO DC transformer is found as another research challenge. Therefore, in this work the author propose a new design which course with these research challenges.

CHAPTER THREE

DC TRANSFORMER THEORY

In this chapter, the theoretical background of conventional DC transformers, or DC-DC converter topologies, will be presented and discussed. The operation principles of the basic topologies in continuous and discontinuous conduction operation modes will be explained and expressed mathematically. As well as the reasons for using IGBTs as a power switching device in the proposed design will be mentioned.

3.1.Conventional DC Transformer topologies

Power electronics DC transformers (or DC-DC converters) are a family of electrical circuits, which convert electrical energy from one level of voltage and current to another using power switching components. In all power converter families, energy conversion is a function of different switching states, regarding different applications. Various families of power converters with optimum technique should be used to deliver the desired electrical energy to the load with maximum efficiency and minimum cost.

DC-DC power converters are employed in a variety of applications, including power supplies for personal computers, office equipment, and DC motor drives. The input to the DC-DC converter is an unregulated DC voltage. The converter produces a regulated output voltage having a magnitude and (possibly polarity) that differs from the DC input voltage. High efficiency is invariably required, the ideal DC-DC converter exhibits 100% efficiency; in practice, efficiencies of 70% to 95% are typically obtained [116].

The basic circuits used to design advanced DC-DC converters consist of three main topologies, which are the step-down topologies, the step-up topologies, and the topologies able to perform both step-up and step-down conversion. Some circuits are also able to perform polarity inverting at output. The step-down topologies are only able to provide an output voltage lower than the input voltage, while the step-up topologies are only able to provide an output voltage higher than the input voltage. The combination of a step-up and a step-down topology enables both voltage reduction and voltage increase with a single switching converter. Thus, the step-down and step-up topologies are the basic converter topologies. And the other topologies are the combination of these two topologies.

The converters are analysed in steady-state, with a constant input voltage V_{in} and a constant output voltage V_o . Further, the components used in the power paths are taken as ideal and no parasitic resistances losses are considered.

3.1.1. Boost Converter

A boost converter is a switch mode DC to DC converter in which the output voltage is greater than the input voltage. It is also called a step-up converter, so the boost converters are used in applications where the output DC voltage needs to be higher than the input DC voltage. By the law of conservation of energy, the input power has to be equal to output power (assuming no losses in the circuit illustrated in figure 3.1), since $V_{in} < V_o$ in boost converters, it follows then that the output current is less than the input current.

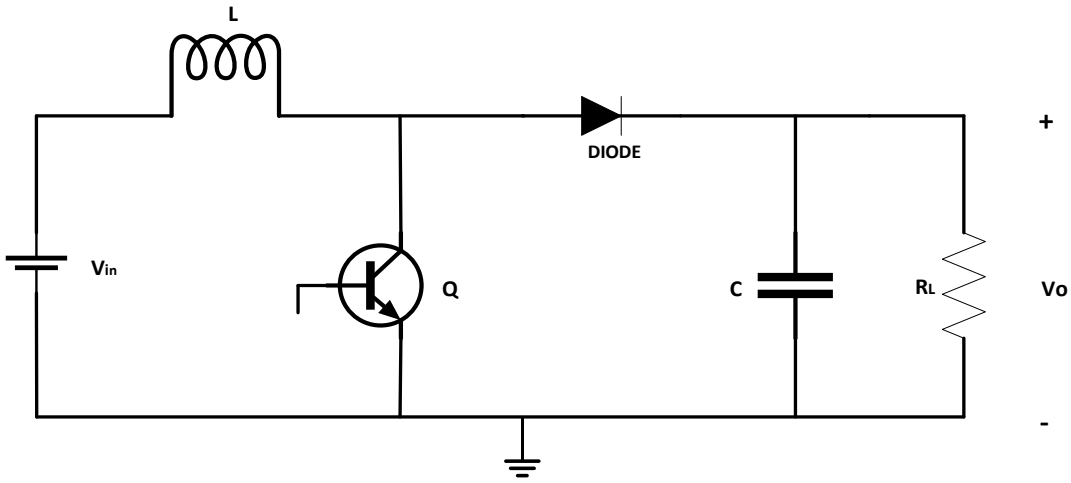


Figure 3.1 boost converter circuit diagram

When the switch is closed, current flow through the inductor in clockwise direction and the inductor stores some energy by generating a magnetic field. When the switch is opened, current will be reduced. The magnetic field previously created will be collapsed to maintain the current towards the load. Thus, the polarity will be reversed (means left side of inductor will be negative). As a result, two sources will be in series causing a higher voltage to charge the capacitor through the diode. If the switch is cycled fast enough, the inductor will not discharge fully in between charging stages, and the load will always see a voltage greater than that of the input source alone when the switch is opened. Also, while the switch is opened, the capacitor in parallel with the load is charged to this combined voltage.

When the switch is then closed and the right-hand side is shorted out from the left hand side, the capacitor is therefore able to provide the voltage and energy to the load. During this time, the diode prevents the capacitor from discharging through the switch. The switch must of

course be opened again fast enough to prevent the capacitor from discharging too much [117].

3.1.1.1.Continuous Conduction Operation Mode

It is assumed for the following analysis that the boost converter operated in Continues Conduction Mode (CCM) in which the current through inductor never goes to zero as shown in figure 3.2. To find the relation between the input voltageV_{in} and the output voltage V_o , two states must be distinguished:

- State 1: the power switch is ON and the diode is reverse biased ($0 < t < t_{ON}$). Here t represents the time variable.

$$V_L = V_{in} \tag{3.1}$$

- State 2: the power switch is OFF, and the diode is forward biased ($t_{ON} < t < T_s$). Here T_s represents the switching period.

$$V_L = V_{in} - V_o \tag{3.2}$$

The inductor's current is continuous and periodic, then integrating the inductor current over one complete switching period (T_s) yields:

$$\frac{1}{L}\int_0^{T_s} V_L(t)\,dt = I_L(T_s) - I_L(0) \tag{3.3}$$

In a steady-state the initial value $I_L(at\ t = 0)$ and the final value $I_L(at\ t = T_s)$ of the inductor current are equal. Therefore, the integral of the inductor voltage over one period must be equal to zero. And this is called the inductor volt second balance approach [20]. It is used over this thesis to determine the conversion ratio of the proposed MIMO step-up DC transformer topology.

By neglecting the ripple voltage of V_{in} and V_o then the inductor voltage within each state will be constant as follows:

$$\int_0^{t_{ON}} V_{in}\,dt + \int_{t_{ON}}^{T_S} (V_{in} - V_o)dt = 0 \tag{3.4}$$

Since V_{in} and V_o are considered to be constant, the output capacitor must be designed to be large enough to provide an output voltage ripple that could be neglected. Thus, the integration of the inductor voltage gives

$$V_{in}t_{ON} + (V_{in} - V_o)(T_S - t_{ON}) = 0 \tag{3.5}$$

$$V_{in}t_{ON} + V_{in}(T_S - t_{ON}) = V_o(T_S - t_{ON}) \tag{3.6}$$

After simplification the output voltage will be

$$V_o = \frac{V_{in}t_{ON}}{T_S - t_{ON}} + V_{in} = V_{in}\left(1 + \frac{t_{ON}}{T_S - t_{ON}}\right) \tag{3.7}$$

$$\frac{V_o}{V_{in}} = \frac{T_S - t_{ON} + t_{ON}}{T_S - t_{ON}} \tag{3.8}$$

$$\frac{V_o}{V_{in}} = \frac{T_S}{T_S - t_{ON}} = \frac{1}{1 - \frac{t_{ON}}{T_S}} = \frac{1}{1 - D} \tag{3.9}$$

$$V_o = \frac{1}{1 - D}V_{in} \tag{3.10}$$

For boost converter the conversion ratio (M_{Boost}) is given by:

$$M_{Boost} = \frac{1}{1 - D} \tag{3.11}$$

Thus, the output DC voltage is greater than the input DC voltage by the ratio $\frac{1}{1-D}$ where D is the power switch duty cycle.

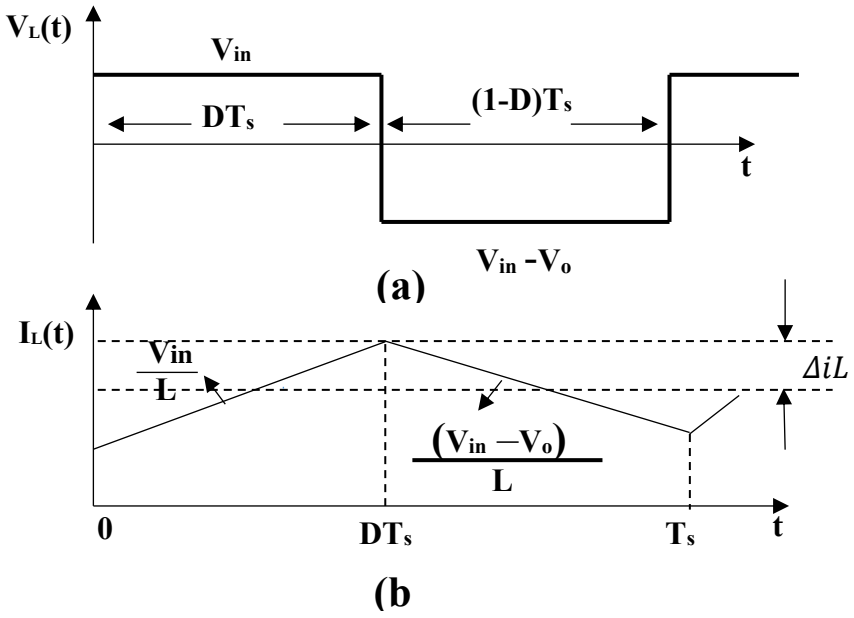


Figure 3.2 boost converter waveforms where ($t_{ON} = t_{OFF}$)[20]

(a) Inductor's voltage waveform

(b) Inductor's current waveform

3.1.1.2. Discontinuous Conduction Operation Mode

As mentioned before for the boost converter to operate in CCM there are two different states, one of which is the ON time state and the other is the OFF time state. Whereas in the Discontinuous Conduction Operation Mode (DCM) an additional state will be added to the normal states, in which the power switch and the diode of the boost converter turn OFF simultaneously for a short period. In this case the inductor current and its voltage will be zero. Therefore, the output voltage decreases by the following ratio:

$$\frac{dv_o}{dt} = \frac{I_{Load}}{C_o} \tag{3.12}$$

Figure 3.3 depicts the inductor current waveform of the boost converter operating in DCM.

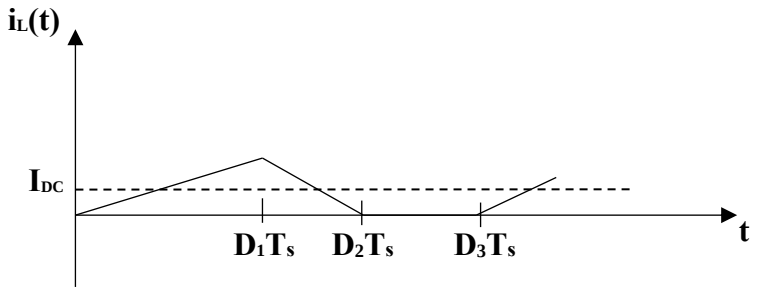


Figure 3.3 boost converter inductor current waveform in DCM [20]

The operation mode of DC-DC converter depends directly on its design parameters such as the load resistance, inductance, capacitance and the duty cycle D. The average DC current will control whether the converter is operating in CCM or DCM. Whereas if the DC current I_L is greater than the ripple currents ΔI_L the DC transformer operates in CCM, but if the $I_L < \Delta I_L$ then the converter is forced into DCM [3]. Once the DC-DC boost converter is forced into DCM the conversion ratio M_{DCM} will change; where the off time interval will not be the same as in CCM as shown in figure 3.3 where $D_1\,T_s,\ D_2\,T_s\ and\ \ D_3\,T_s$represent the durations of the ON time, the OFF time and the dead time respectively. By applying the volt second balance approach the inductor voltage over one switching period will be zero.

$$\int_0^{D_1} V_L\,dt \ + \int_{D_1}^{D_2} V_L dt + \int_{D_2}^{D_3} V_L\,dt = 0 \tag{3.13}$$

As the inductor voltage in the period between $(D_2 - D_3)$ equals to zero then the result of the integration will be:

$$D_1\,V_{in} \ + \ D_2\,(V_{in} \ - \ V_o) \ + \ D_3\,(0) \ = \ 0 \tag{3.14}$$

Then the conversion ratio equals:

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{D_1 + D_2}{D_2} \tag{3.15}$$

To find the D_2 the capacitor charge balance approach is used in which in periodic steady-state the net change in capacitor voltage is zero [20]. Hence the total charge under the capacitor current waveform is zero then the average capacitor current I_C is zero as follows:

$$\frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = 0 \tag{3.16}$$

Then the average diode's current will be:

$$I_{Diode} = I_C + \frac{V_o}{R_L} \tag{3.17}$$

$$I_C = 0$$

Hence,

$$I_{Diode} = \frac{V_o}{R_L} \tag{3.18}$$

Then to find D_2 integrate the diode current over one period as follows:

$$I_{Diode} = \frac{1}{T_s}\int_0^{T_s} i_{Diode}(t)\, dt \tag{3.19}$$

$$I_{Diode} = 0.5\, i_{L-peak} D_2 T_s \tag{3.20}$$

For boost converter the inductor current peak value acquires during the ON time thus by substitution i_{L-peak}

$$i_{L-peak} = \frac{V_{in} D_1 T_s}{L} \tag{3.21}$$

$$I_{Diode} = \frac{V_{in} D_1\, D_2 T_s}{2L} \tag{3.22}$$

Therefore, there are two equations for the average diode current. By equating them the following relation is obtained:

$$\frac{V_o}{R_L} = \frac{V_{in} D_1\, D_2 T_s}{2L} \tag{3.23}$$

From the M_{DCM} equation D_2 could be expressed as follows:

$$D_2 = \frac{D_1 V_{in}}{V_o - V_{in}} \tag{3.24}$$

After substituting (3.24) in (3.23) then the conversion ratio of boost converter operating in DCM will be:

$$V_o{}^2 - V_o V_{in} - \frac{\left(V_{in}{}^2 D_1{}^2\right)}{k} = 0 \tag{3.25}$$

Where

$$k = \frac{2L}{R_L T_s} \tag{3.26}$$

Factorise the second order equation,

$$\frac{V_o}{V_{in}} = \frac{1 \pm \sqrt{1 + 4{D_1}^2/k}}{2} \tag{3.27}$$

As V_o is positive then only one root will be considered so that the conversion ratio M_{DCM} is equal to:

$$M_{DCM} = \frac{1 + \sqrt{1 + 4{D_1}^2/k}}{2} \tag{3.28}$$

The output voltage is a function of the duty cycle of the power switch when the converter operates in CCM while, in DCM, the output voltage will be a function of the duty cycle and k which is represented by L and R_L.

To ensure that the designed boost converter is operating in CCM the following relation must occur:

$$I_L > \Delta I_L \tag{3.29}$$

$$\frac{V_{in}}{(1 - {D_1}^2)R_L} > \frac{V_{in} D_1 T_s}{2L} \tag{3.30}$$

Rearranging both sides:

$$\frac{2L}{R_L T_s} > (1 - {D_1}^2)D_1 \tag{3.31}$$

Assume $k_{critical} = (1 - {D_1}^2)D_1$

$$\begin{Bmatrix} In\ CCM, k > k_{critical} \\ In\ DCM, k < k_{critical} \end{Bmatrix} \tag{3.32}$$

In general, the conversion ratio of DC-DC boost converter is:

$$M = \begin{cases} \dfrac{1}{1 - D_1}, & k > k_{critical} \\ \dfrac{1 + \sqrt{1 + 4{D_1}^2/k}}{2}, & k < k_{critical} \end{cases} \tag{3.33}$$

As $\frac{4{D_1}^2}{k} \gg 1$, then the approximation of M_{DCM}in DCM will be:

$$M_{DCM} = \frac{1}{2} + \frac{D_1}{\sqrt{k}} \tag{3.34}$$

If the converter is designed to operate in DCM, then the automatic reset of inductor current to zero each switch cycle ensures no core saturation of the inductor. Furthermore, the inductor size in DCM is much smaller than in CCM which means less cost. In contrast, the ripple current is high in DCM which complicates the filter designs and also leads to an increase in the losses of the DC-DC converter and decreasing efficiency [20]. Thus, in this work the proposed MIMO step-up DC transformer is designed to operate in CCM to ensure a more efficient and reliable design.

3.1.2. Buck Converter

The buck converter shown in Figure 3.4 is the simplest step-down switching topology. It is made of a power switch acting as the energizing switch for the inductor L, a power diode assuring the continuity of the current in L, and a filtering capacitor C reducing the output voltage ripple on V_o. The power input is represented by the DC voltage source delivering V_{in}.

As the buck converter is a voltage step down and current step up converter, thus the buck converters are used in applications where the output DC voltage needs to be lower than the input DC voltage. The basic operation of the buck converter is that the current in an inductor is controlled by two switches; namely a controlled switch (transistor) and an uncontrolled switch (diode). In the ideal case, all the components are considered to be ideal. Specifically, the switch and the diode have zero voltage drop in the ON state, and zero current flow when OFF. Also, in that case the inductor has zero series resistance.

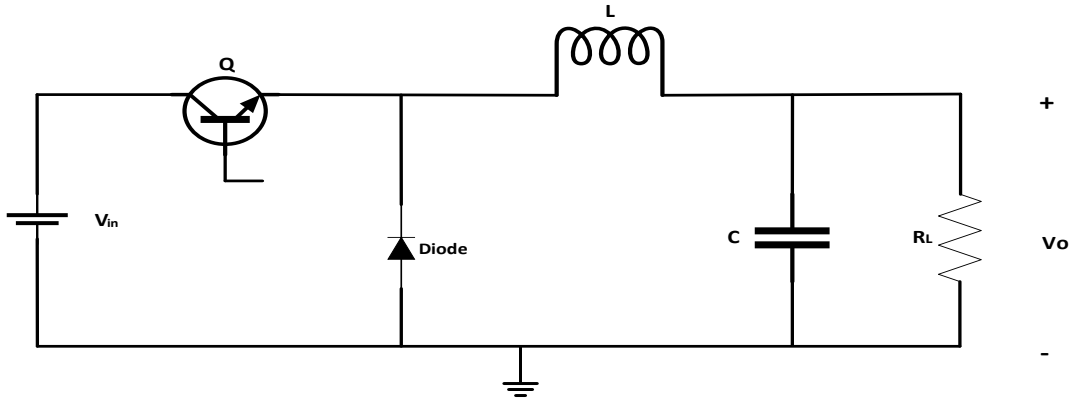


Figure 3.4 buck converter circuit diagram

V_o is equal to V_{in} when the power switch (MOSFETs, IGBTs, BJTs or Thyristors) is ON, and is equal to zero when the switch is OFF. The switch changes the ON-OFF states periodically, such that the switch voltage waveform is a rectangular waveform having period

T_s and duty cycle D. The duty cycle is equal to the fraction of time that the switch is connected, and hence $0 < D < 1$. The switching frequency f_s is equal to $1/T_s$. Typical switching frequencies lie in the range $1\,kHz$ to $1\,MHz$ depending on the speed of the semiconductor devices [116]. The conceptual model of the buck converter is best understood in terms of the relation between current and voltage of the inductor. Beginning with the switch open (OFF-state), the current in the circuit is zero. When the switch is closed (ON-state), the current will begin to increase, and the inductor will produce an opposing voltage across its terminals in response to the changing current. The inductor equation states that the voltage V_L at the inductor's terminals is proportional to the rate of change in current through the inductor L.

The constant of proportionality is the inductance L.

$$V_L(t) = L\frac{d}{dt}I_L(t) \tag{3.35}$$

This voltage drop counteracts the voltage of the source and therefore reduces the net voltage across the load. Over time, the rate of change of current decreases, and the voltage across the inductor also then decreases, increasing the voltage at the load. During this time, the inductor stores energy in the form of a magnetic field. If the switch is opened while the current is still changing, then there will always be a voltage drop across the inductor, so the net voltage at the load will always be less than the input voltage source. When the switch is opened again (OFF-state), the voltage source will be removed from the circuit, and the current will decrease. The changing current will produce a change in voltage across the inductor. The stored energy in the inductor supports current flow through the load. During this time, the inductor is discharging its stored energy into the rest of the circuit. If the switch is closed again before the inductor is fully discharged, the voltage at the load will always be greater than zero. The capacitor equation states that the current I_C flowing through the capacitor C is proportional to the rate of change in voltage V_C at the capacitor's terminals. The constant of proportionality is the capacitance C.

$$I_C(t) = C\frac{d}{dt}V_C(t) \tag{3.36}$$

3.1.2.1.Continuous Conduction Operation Mode

Figure 3.5 shows the waveforms for the CCM of operation where the inductor's current flows continuously $i_L(t) > 0$. By using the same methodology as the boost converter in section 3.1.1 then the inductor voltage over one period must equal to zero.

$$\int_0^{T_S} V_L dt = 0 \tag{3.37}$$

When the switch is ON for a time duration of t_{ON}, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $V_L = V_{in} - V_o$ across the inductor. This voltage causes a linear increase in the inductor current I_L. When the switch is turned OFF the current flows through the diode and $V_L = -V_o$.

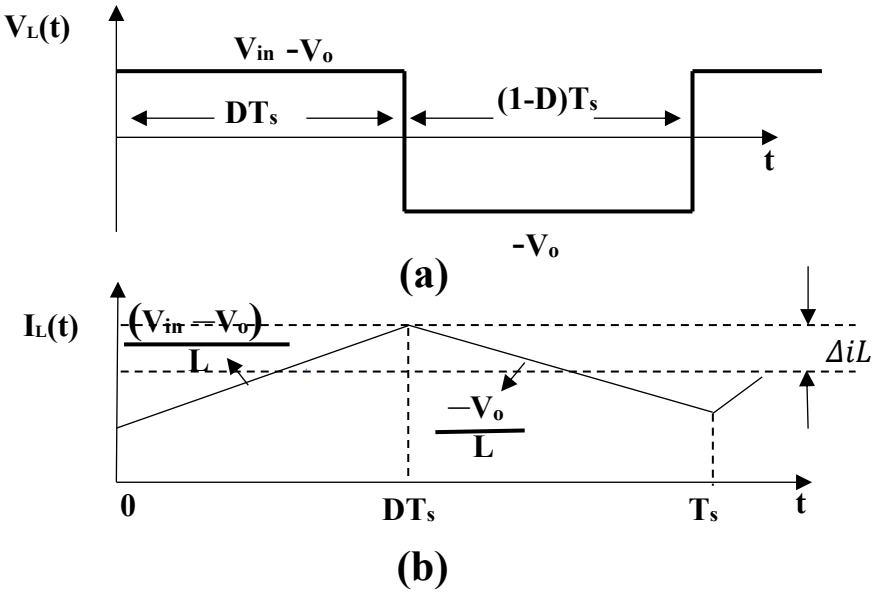


Figure 3.5 buck converter waveforms where ($t_{ON} = t_{OFF}$)[20]

(a) Inductor's voltage waveform

(b) Inductor's current waveform

In steady-state operation and by principle of inductor volt second balance [20], the average inductor voltage over one period must be zero. Then the output voltage as a function of the switch duty cycle could be found as follows

$$\int_0^{T_S} V_L \, dt = 0 \tag{3.38}$$

$$\int_0^{t_{ON}} V_L \, dt + \int_{t_{ON}}^{T_S} V_L \, dt = 0 \tag{3.39}$$

$$\int_0^{t_{ON}} (V_{in} - V_o)\, dt - \int_{t_{ON}}^{T_S} V_o \; dt = 0 \tag{3.40}$$

$$(V_{in} - V_o)t_{ON} = V_o(T_S - t_{ON}) \tag{3.41}$$

$$V_{in}t_{ON} = V_oT_S \tag{3.42}$$

$$V_o = (t_{ON}/T_S)\, V_{in} \tag{3.43}$$

As the duty cycle D,

$$D = \frac{t_{ON}}{T_S} \tag{3.44}$$

Then the buck converter's output voltage

$$V_o = D\, V_{in} \tag{3.45}$$

Therefore, the output voltage varies linearly with the duty cycle of the switch for a given input voltage.

For ideal components

$$V_{in}I_{in} = V_oI_o \tag{3.46}$$

$$I_o = \frac{1}{D} I_{in} \tag{3.47}$$

In CCM the output voltage could be controlled by changing the switch's duty ratio from 0 to 1.

The output voltage ripple could be calculated as follows

During the ON time $(0 < t < t_{ON})$

$$V_L(t) = V_{in} - V_o \tag{3.48}$$

$$L\frac{di_{L(t)}}{dt} = V_{in} - V_o \tag{3.49}$$

$$\frac{di_{L(t)}}{dt} = \frac{V_{in} - V_o}{L} \tag{3.50}$$

During the OFF time $(t_{ON} < t < T_s)$

$$V_L(t) = -V_o \tag{3.51}$$

$$V_L(t) = L\frac{di_{L(t)}}{dt} \tag{3.52}$$

$$\frac{di_{L(t)}}{dt} = \frac{-V_o}{L} \tag{3.53}$$

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{C}\frac{\Delta I_L T_S}{4} \tag{3.54}$$

$$\Delta I_{L_{OFF}} = \frac{V_o}{L}(1-D)T_S \tag{3.55}$$

Then average ripple voltage

$$\Delta V_o = \frac{T_S}{8C}\frac{V_o}{L}(1-D)T_S \tag{3.56}$$

Where:

V_o is the output DC voltage.

ΔV_o is the output voltage ripple.

D is the switch duty cycle.

The conversion ratio is defined as the ratio of the output DC voltage V_o to the input DC voltage V_{in} under steady state conditions. For buck converters the conversion ratio M_{Buck} is given by:

$$M_{Buck} = \text{D} \tag{3.57}$$

3.1.3. Buck-Boost Converter

3.1.3.1.Continuous Conduction Operation Mode

The buck–boost converter is a type of DC-DC converter where a buck (step-down) converter combined with a boost (step-up) converter, so the output DC voltage magnitude is either greater or less than the input DC voltage magnitude, in contrast the output DC voltage which has the opposite polarity of the input voltage.

Figure 3.6 shows the circuit diagram of a buck-boost converter. The basic principle of the buck–boost converter is simple: when the switch turns ON the input voltage source is directly connected to the inductor L. This results in accumulating energy in L. In this stage,

the capacitor supplies energy to the output load. While in the OFF state, the inductor is connected to the output load and capacitor, so energy is transferred from L to C and R_L.

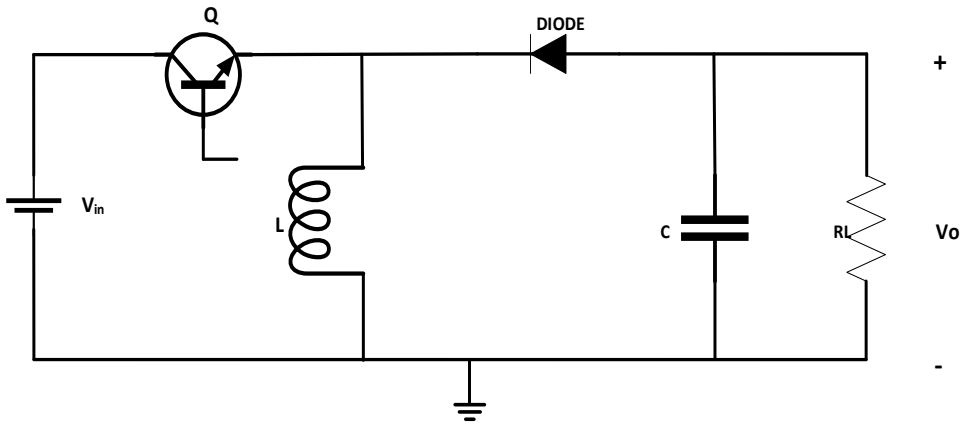


Figure 3.6 buck- boost converter circuit diagram

Compared to the buck and boost converters, the characteristics of the buck–boost converter are mainly:

- Polarity of the output voltage is opposite to that of the input.
- The output voltage can vary continuously from 0 to ∞ (for an ideal converter), while, the output voltage ranges for buck and boost converter are respectively V_{in} to 0 and V_{in} to ∞ [117].

The buck-boost converter circuit is used when a higher or lower output voltage than the input voltage is required. When the switch is active the current flowing through the inductor L increases and the diode is reversed biased. When the switch turns OFF the inductor L drains the current through the diode which becomes forward biased. This generates a negative voltage at the output side. For this analysis, the same hypothesis as for the previous case is considered where the converter operates in CCM and has reached steady-state.

By using the same methodology as for the boost converter in section 3.1.1, the voltage conversion ratio $M_{Buck-Boost}$ of the buck-boost converter could be calculated as shown in figure 3.7 as follows

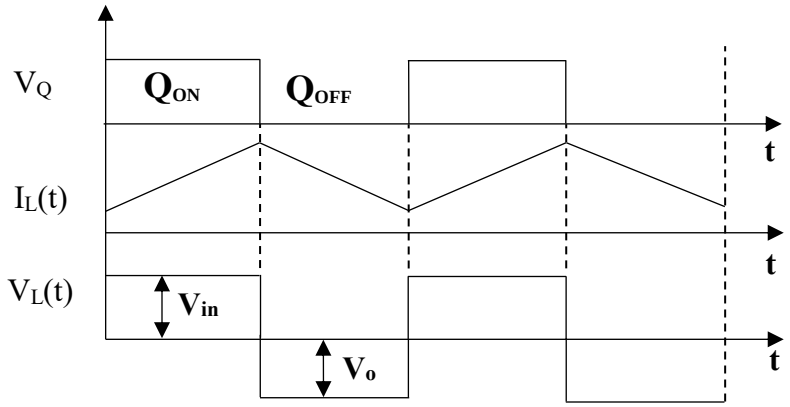


Figure 3.7 inductor's voltage and current waveforms of a buck-boost converter where ($t_{ON} = t_{OFF}$)[20]

$$\int_0^{t_{ON}} V_L \, dt + \int_{t_{ON}}^{T_S} V_L \, dt = 0 \tag{3.58}$$

$$\int_0^{t_{ON}} V_{in} \, dt - \int_{t_{ON}}^{T_S} V_o \, dt = 0 \tag{3.59}$$

$$V_{in} t_{ON} + V_o \, (T_S - t_{ON}) = 0 \tag{3.60}$$

For buck-boost converter in CCM the conversion ratio is given by:

$$M_{Buck-Boost} = \frac{-t_{ON}}{T_S - t_{ON}} = \frac{-\mathrm{D}}{1 - \mathrm{D}} \tag{3.61}$$

To calculate the output voltage ripple, the same methodology from section 3.1.2.1 will be used as shown in equation (3.62):

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{I_o D \, T_S}{C} \tag{3.62}$$

$$\frac{\Delta V_o}{V_o} = \frac{D}{\tau} T_S \tag{3.63}$$

Where the time constant τ is:

$$\tau = R * C \tag{3.64}$$

3.2.Semiconductor Switching Devices

Power electronics is the application of the solid-state electronics to the control and conversion of electrical power. In modern systems the conversion is performed with semiconductor switching devices such as diodes, thyristors and transistors. The capabilities

and economy of power electronics are determined by the active devices that are available. Their characteristics and limitations are a key element in the design of power electronics systems.

Devices such as diodes conduct when a forward voltage is applied and have no external control of the start of conduction. Power devices such as Silicon Controlled Rectifiers (SCR) and thyristors allow control of the start of conduction but rely on periodic reversal of current flow to turn them OFF. Devices such as Gate Turn OFF thyristors (GTO), Bipolar Junction Transistors (BJT) and Metal Oxide Semiconductor Field Effect Transistors (MOSFET) provide full switching control and can be turned ON or OFF without regard to the current flow through them which are known as voltage-controlled switching devices [118].

Before the development of the Insulated Gate Bipolar Transistors (IGBT), power MOSFETs were used in medium or low voltage applications which require fast switching. Whilst BJTs, thyristors and GTOs were used in medium to high voltage applications which require high current conduction. A power MOSFET allows for simple gate control circuit design and has excellent fast switching capability. On the other hand, the internal resistance between drain and source during ON state, limits the power handling capability of a MOSFET, thus incurring high losses due to $R_{DS_{ON}}$ while the BJT has excellent ON state characteristics due to the low forward voltage drop, but its base control circuit is complex.

The IGBT developed in the early 1980s has the combined advantages of BJT and MOSFET making it a voltage controlled bipolar device [118]. Figure 3.8 depicts the equivalent circuit of IGBT and its electrical symbol. Its gate behaviour is similar to MOSFET so a simple gate control circuit design is required to turn it ON and OFF, also it has low losses like BJT due to its low ON state collector- emitter voltage $V_{CE_{saturation}} = (2-3)\,V$. Because of that IGBTs are very popular for high voltage applications $< 3.3\,kV$ with good switching capability up to$100\ kHz$.

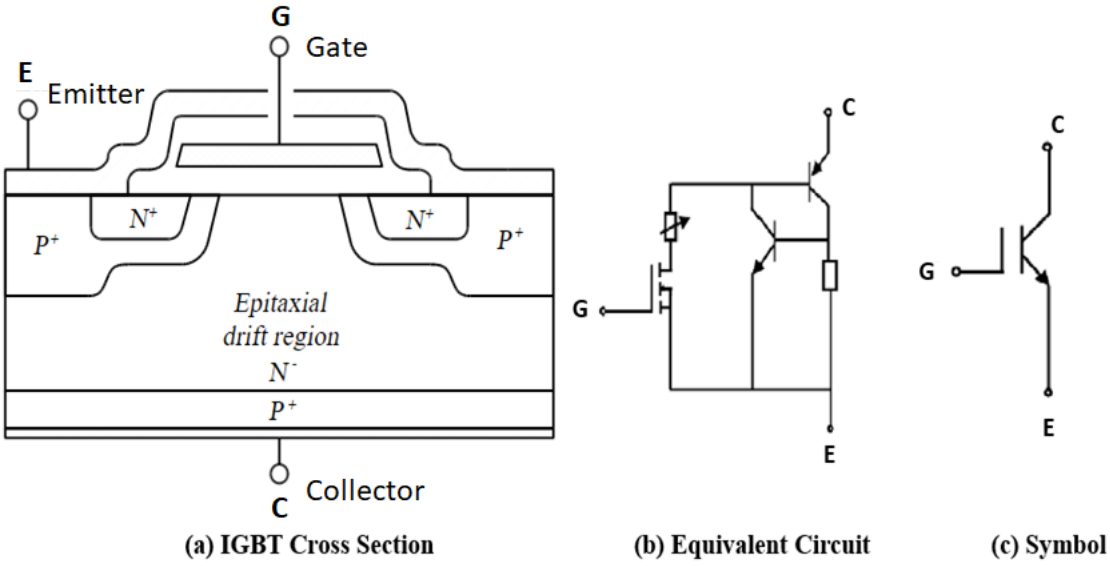


Figure 3.8 IGBT symbol and its equivalent circuit- Image credit: Cyril, B. (2006) -Wikipedia "This file is licensed under the Creative Commons Attribution-Share Alike 3.0" [119]

Figure 3.9 illustrates the voltage, current and frequency ratings for the aforementioned semiconductor switches.

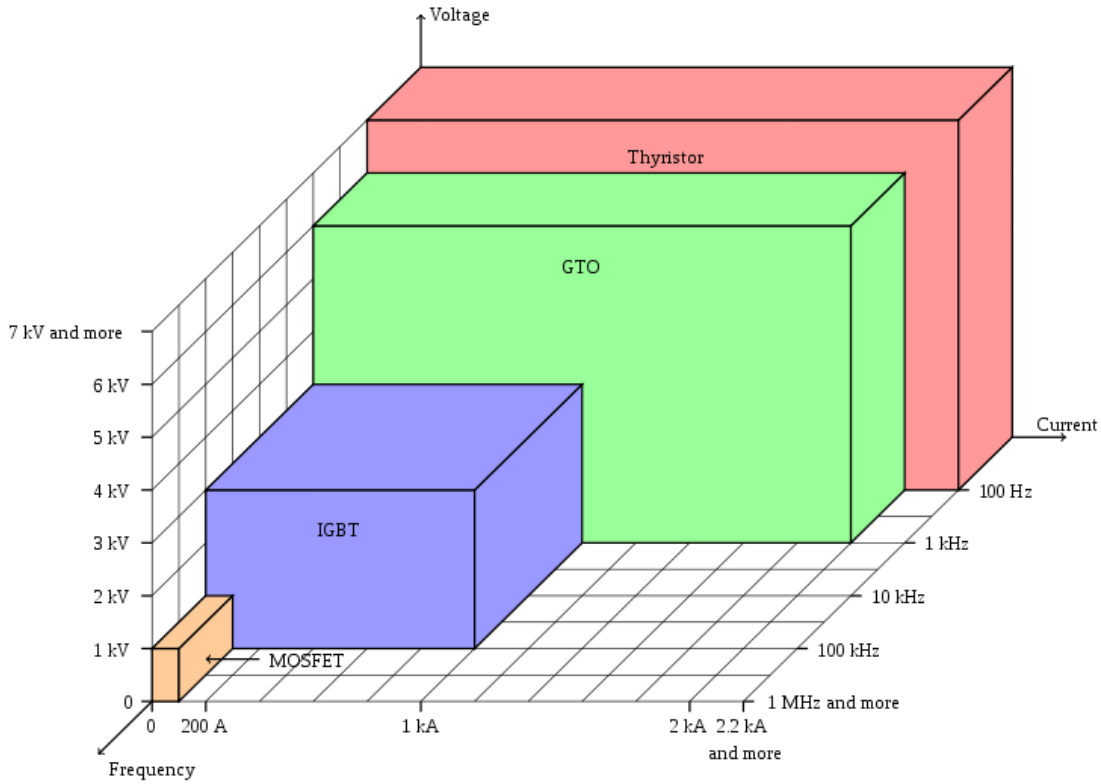


Figure 3.9 ratings of semiconductor switches- Image credit: Cyril, B. (2006) -Wikipedia "This file is licensed under the Creative Commons Attribution-Share Alike 3.0" [119]

From figure 3.9 the IGBT ratings could be concluded as follows:

$$V_{CE} < 3.3\ kV$$

$$I_C < 1.2\ kA$$

$$f_s < 100\ kHz$$

IGBT is used in this project as a semiconductor switching device due to its fast switching capability resulting in the reduction of passive component size and cost. Furthermore, it easily controls the ON and OFF state, where it only requires a small voltage on the gate to maintain conduction through the device. Making the gate signal zero or slightly negative will cause it to turn OFF. Whereas in thyristors for example, once the device turns ON, the gate loses its control to turn OFF the device. The turn OFF is achieved by applying a reverse voltage across the anode and cathode which complicates the control design. Also, the switching frequency of the device will be limited by the ON state power losses which are determined by the forward voltage at any given current. The switching power loss becomes a dominating factor affecting the device junction temperature at high operating frequencies [120].

In contrast the IGBT is a unidirectional device, meaning it can only pass current in the forward direction from collector to emitter whereas the MOSFET has a bidirectional current switching capability which is controlled in the forward direction. Using two IGBTs in antiparallel could also provide the device with a bidirectional power flow capability.

In the proposed design the utilised IGBTs are combined with antiparallel diodes to obtain a continuous path of the inductor's current when the switch is OFF. This also prevents the current from circulating through the input source, therefore reducing its heatsink design.

Table 3.1 illustrates the main features of the IGBTs over the mentioned switching devices which make it popular and preferable to use for high voltage applications.

Table 3.1. Comparison between the switching devices' characteristics [121]

Device characteristic	*Power Bipolar*	*Power MOSFET*	*IGBT*
Voltage Rating	*High* $< 1\ kV$	*High* $< 1\ kV$	*Very High* $> 1\ kV$
Current Rating	*High* $< 500\ A$	*Low* $< 200\ A$	*High* $> 500\ A$
Input Drive	*Current* $(20 - 200)\ A$	*Voltage* $V_{GS} = (3 - 10)\ V$	*Voltage* $V_{GE} = (4 - 8)\ V$
Input Impedance	*Low*	*High*	*High*
Output Impedance	*Low*	*Medium*	*Low*
Switching Speed	*Slow*(μ *Sec*)	*Fast*(*n Sec*)	*Medium*
Cost	*Low*	*Medium*	*High*

3.3.Small Signal Analysis

DC transformers (or DC-DC converters) are switching converters with nonlinear characteristics. During a switching cycle the topology of the equivalent linear circuit changes every time the switch opens or closes, resulting in nonlinear and time variant systems [122]. The nonlinearity of the system invalidates the direct application of the control theory including the mathematical representation of the system and its properties to behave and adapt in a desired way [122]. Thus, to design a closed loop with classical (linear) control methods, a mathematical representation of the plant must be obtained. In order to do this, it must be understood how variations in the power input voltage, the load current, or the duty cycle ($D = \frac{T_{ON}}{T_s}$) affect the output voltage. All these could be represented in a dynamic model of the switching transformer to obtain a Small Signal Model (SSM) [43]. Using small signal modelling is important so as to achieve a complete transfer function of the transformer. The analysis also helps in identifying the deviation around a steady state operating point achieving a more stable and regulated output voltage [5].

To obtain a linear model that is easier to analyse, the construction of an SSM that has been linearised about a quiescent operating point is required, in which the harmonics of the modulation or excitation frequency are neglected [43]. Figure 3.10 illustrates linearization of the familiar diode $(i - v)$ characteristic. Suppose that the diode current $i(t)$ has a quiescent DC value I and a signal component $\hat{\imath}(t)$. As a result, the voltage $v(t)$ across the diode has a quiescent value (steady state value) V and a signal component $\hat{v}(t)$. If the signal components are small compared to the quiescent values, then the relation between $\hat{\imath}(t)$ and $\hat{v}(t)$ is approximately linear $\hat{v}(t) = r_D\,\hat{\imath}(t)$, where $(1/r_D)$ is the diode conductance.

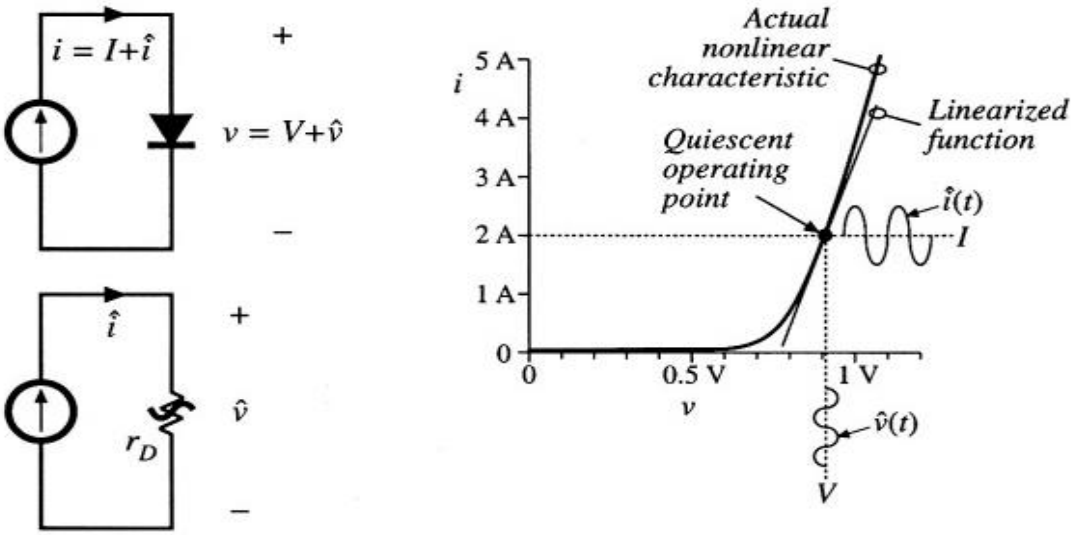


Figure 3.10 Small signal equivalent circuit modelling of the diode -Image credit: © 2016, IEEE [43]

3.3.1. State Space Averaging Approach

The state space averaging method is a state space description of dynamical systems in order to derive the small signal equations of the switching transformers. The SSM with state space averaging technique is the most popular and widely adopted approach in the linearization of DC transformers [124] due to the generality of the state space averaging results. This is because the SSM could be obtained by providing the state equations of the designed DC transformer [43]. The derived capacitor's voltage and inductor's current equations of the DC transformer over one period during the ON and OFF switching time, constitute a system of nonlinear differential equations (DC terms, first order AC terms and second order AC terms) which are known as averaged equations, hence these equations must be linearised by perturbing variables. Employing a Laplace transform and omitting additional AC and DC terms then only first order AC terms (linear) are provided, thus the system transfer functions are achieved [116].

As the proposed MIMO DC transformer as mentioned in chapter two of this thesis is a step-up type then the state space representation will be discussed for the conventional ideal boost converter in continuous operation mode. Figure 3.11 depicts the basic DC-DC boost (step-up) converter circuit which consists of the inductor L, the capacitor C, diode and the power switch. The procedure to extract the averaged equations to obtain the SSM starts with deriving the capacitor voltage and inductor current equations as follows:

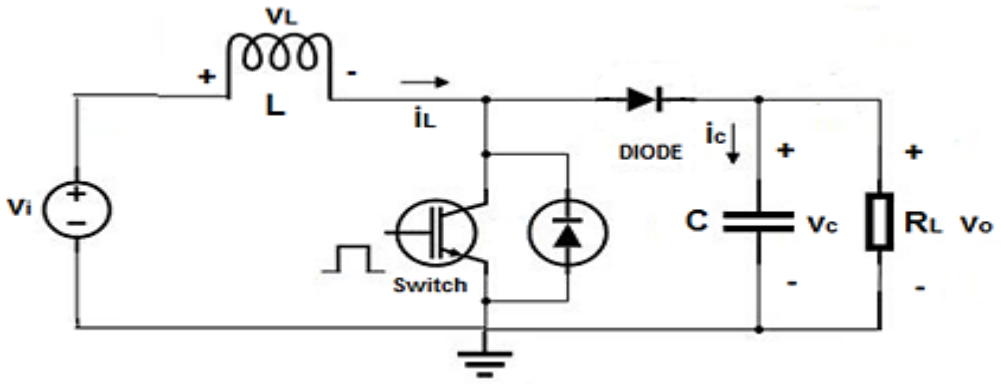


Figure 3.11 Basic DC-DC boost converter circuit structure.

Applying Kirchhoff's voltage law and Kirchhoff's current law during the ON switching interval, the inductor's current $i_L\,(t)$ and the capacitor's voltage $v_c\,(t)$ equations are:

$$v_L(\mathrm{t}) = \mathrm{L}\frac{di_L(t)}{dt} =< v_i(t) >_{T_s} \tag{3.65}$$

$$i_c(\mathrm{t}) = \mathrm{C}\frac{dv_c(t)}{dt} = -< \frac{v_c(t)}{R} >_{T_s} \tag{3.66}$$

When the switch is OFF:

$$v_L(\mathrm{t}) = \mathrm{L}\frac{di_L(t)}{dt} =< v_c(t) >_{T_s} \tag{3.67}$$

$$i_c(\mathrm{t}) = \mathrm{C}\frac{dv_c(t)}{dt} = -< i_L(t) >_{T_s} -< \frac{v_c(t)}{R} >_{T_s} \tag{3.68}$$

It is clear that in each cycle (ON, OFF) T_s there are two equations for the inductor's current and the capacitor's voltage, so the inductor voltage averaged value over one cycle $< v_L(t) >_{T_s}$ is:

$$< v_L(t) >_{T_s} = \frac{1}{T_s}\int_0^{T_s} v_L(\tau)d\tau = d(t) < v_i(t) >_{T_s} + \acute{d}(t) < v_c(t) >_{T_s} \tag{3.69}$$

Where $d(t)$ is the duty cycle of the switch and $\acute{d}(t)$= $\big(1 - d(t)\big)$.

After substituting (3.65) in (3.69)

$$L\frac{d < i_L(t) >_{T_s}}{dt} = d(t) < v_i(t) >_{T_s} + \acute{d}(t) < v_c(t) >_{T_s} \tag{3.70}$$

So (3.71) is the result of averaging the inductor waveform:

$$i_L(T_s) = i_L(0) + \frac{T_s}{L}\{d(t) < v_i(t) >_{T_s} + \acute{d}(t) < v_c(t) >_{T_s}\} \quad (3.71)$$

Figure 3.12 shows the actual inductor current waveform and the averaged waveform $< i_L(t) >_{T_s}$.

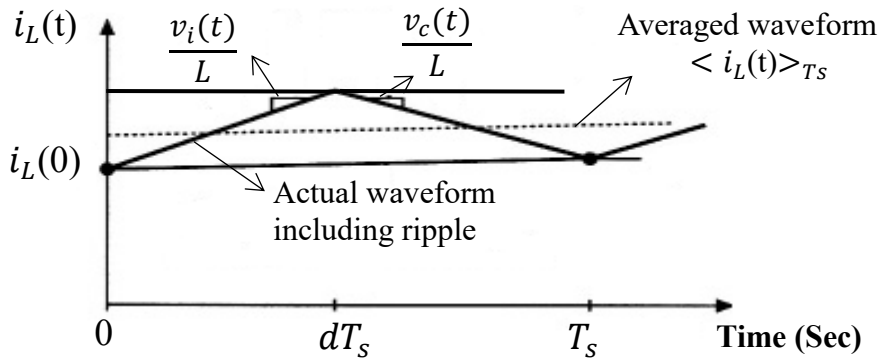


Figure 3.12 the inductors current waveform where $i_L(0) = i_L(T_s)$

The capacitor averaged waveforms could be obtained by the same procedure, so the result will be in (3.72) and (3.73)

$$i_c(T_s) = \left\{d(t)(< -\frac{v_c(t)}{R} >_{T_s}) + \acute{d}(t)(-< i_L(t) >_{T_s} - < \frac{v_c(t)}{R} >_{T_s})\right\} \quad (3.72)$$

$$C\frac{d < v_c(t) >_{T_s}}{dt} = \left\{d(t)(< -\frac{v_c(t)}{R} >_{T_s}) + \acute{d}(t)(-< i_L(t) >_{T_s} - < \frac{v_c(t)}{R} >_{T_s})\right\} \quad (3.73)$$

To construct the SSM assuming that the averaged inductor current and the averaged capacitor voltage during a cycle will be equal to the quiescent value (steady state value) I_L and V_c, plus some small AC variation $\hat{\imath}_L(t)$, $\hat{v}_c(t)$ and the same for the duty cycle $d(t)$ and the input voltage $v_i(t)$.

$$< i_L(t) >_{T_s} = I_L + \hat{\imath}_L(t) \quad (3.74)$$

$$< v_c(t) >_{T_s} = V_c + \hat{v}_c(t) \quad (3.75)$$

With the assumption that the AC value is much smaller in magnitude than the DC value then the nonlinear equations (3.70), (3.73) could be linearised by substituting (3.74) and (3.75)

$$L\frac{d(I_L + \hat{\imath}_L(t))}{dt} = (D + \hat{d}(t))(V_i + \hat{v}_i(t)) + (\acute{D} - \hat{d}(t))(V_c + \hat{v}_c(t)) \quad (3.76)$$

After collecting terms in (3.76) the equation will be

$$L\left(\frac{dI_L}{dt}+\frac{d\hat{\imath}_L(t)}{dt}\right)=\underbrace{\left(\mathrm{D}\,V_i+\acute{D}\,V_c\right)}_{\text{DC terms}}+\underbrace{\left(\mathrm{D}\hat{v}_i(t)+\acute{D}\hat{v}_c(t)+\left(V_i-V_c\right)\hat{d}(t)\right)}_{\text{First order AC terms (linear)}}+ \tag{3.77}$$

$$\cdots\underbrace{\hat{d}(\mathrm{t})(\hat{v}_i(t)-\hat{v}_c(t))}_{\text{Second order AC terms (nonlinear)}}$$

From (3.77) any product of two AC terms is considered negligible and removed. Thus, the nonlinear terms are no longer available in the equation and the averaged inductor current will be equal to the DC terms plus first order AC terms (linear) in that case the linearization is obtained.

In section 5.3.1 of this thesis the SSM of the proposed MIMO step-up DC transformer has been derived and the linearization of the plant are acquired using the same methodology.

3.3.1.1.Ideal DC-DC Boost Converter Transfer Function

The previous equations could be written in a matrix from as follows

For the ON state:

$$\begin{bmatrix} L\dfrac{di_L(t)}{dt} \\ C\dfrac{dv_c(t)}{dt} \end{bmatrix}=\begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix}+\begin{bmatrix} 1 \\ 0 \end{bmatrix}\begin{bmatrix} v_i(t) \\ 0 \end{bmatrix} \tag{3.78}$$

$$y(t)=\begin{bmatrix} 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{3.79}$$

For the OFF state:

$$\begin{bmatrix} L\dfrac{di_L(t)}{dt} \\ C\dfrac{dv_c(t)}{dt} \end{bmatrix}=\begin{bmatrix} 0 & -1 \\ 1 & -\dfrac{1}{R} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix}+\begin{bmatrix} 1 \\ 0 \end{bmatrix}\begin{bmatrix} v_i(t) \\ 0 \end{bmatrix} \tag{3.80}$$

$$y(t)=\begin{bmatrix} 1 & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{3.81}$$

The ON and OFF equations could be averaged using the state space averaging technique [125]. Then the general state space representation of state variables takes the following form where in most of the analysis the matrix D is assumed to be zero [125].

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{3.82}$$

$$y(t) = Cx(t) + Du(t) \tag{3.83}$$

A, B, C and D are the system matrices $S\ (A, B, C, D)$ where:

Dynamic matrix A: describes the dynamics of the system and controls the trajectory of the state vector $x(t)$.

Input matrix B: shows how each control input affects the state variables of the systems.

Output matrix C: transforms the state vector $x(t)$ into the output vector $y(t)$.

Transmission matrix D: indicates the direct (feedforward) effect of control inputs to output vector $y(t)$. Here the D matrix is represented as a null matrix as there is no direct effect of control inputs to output.

The DC transformer's waveforms are expressed as a steady state value plus perturbation as follows:

$$x(t) = X + \hat{x}(t) \tag{3.84}$$

$$u(t) = U + \hat{u}(t) \tag{3.85}$$

$$y(t) = Y + \hat{y}(t) \tag{3.86}$$

These are A_1, B_1 and C_1 matrices from the ON state dynamic equations. And A_2, B_2 and C_2 matrices are from the OFF state dynamic equations. Then the averaged matrices will take the following form:

$$A = A_1 D + A_2 \acute{D} \tag{3.87}$$

$$B = B_1 D + B_2 \acute{D} \tag{3.88}$$

$$C = C_1 D + C_2 \acute{D} \tag{3.89}$$

After performing and substituting the averaged matrices with their corresponding equations, the A, B and C matrices could be obtained as follows:

$$A = \begin{bmatrix} 0 & -\acute{D} \\ \acute{D} & -\frac{1}{R} \end{bmatrix}, B = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, C = [1 \quad 0] \tag{3.90}$$

$$\begin{bmatrix} L\frac{di_L(t)}{dt} \\ C\frac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\acute{D} \\ \acute{D} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} v_i(t) \\ 0 \end{bmatrix} \tag{3.91}$$

$$y(t) = [1 \quad 0] \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} \tag{3.92}$$

In the steady state condition $\dot{X} = 0$ and using the relation $X = A^{-1} * B * U$ as stated in [125], A^{-1} is the inverse of matrix A. This is found as follows:

$$A^{-1} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}^{-1} = \frac{1}{a_{11}a_{22} - a_{21}a_{12}} \begin{bmatrix} a_{22} & -a_{12} \\ -a_{21} & a_{11} \end{bmatrix} \tag{3.93}$$

Then from equation (3.92) the relation between the output voltage and the input voltage in the steady state will be:

$$V_o = \frac{V_i}{(1 - D)} \tag{3.94}$$

To obtain the transfer function of the ideal boost converter the linearised equation (3.77) will be used in a steady state condition as follows

$$\begin{bmatrix} L\frac{d\hat{i}_L(t)}{dt} \\ C\frac{d\hat{v}_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\acute{D} \\ \acute{D} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_o(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} \hat{v}_i(t) \\ 0 \end{bmatrix} \begin{bmatrix} V_o \\ -I \end{bmatrix} \hat{d} \tag{3.95}$$

Using the Laplace transform the transfer function between the duty cycle as a control input and the output voltage is given in equation (3.96) assuming

$\hat{v}_i(s) = 0$:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{\frac{-1}{C[S - \frac{\acute{D} * V_o}{L * I_o}]}}{[S^2 + \frac{S}{C * R} + \frac{\acute{D}^2}{L * C}]} \tag{3.96}$$

3.3.1.2.Non-Ideal DC-DC Boost Converter Transfer Function

In the non-ideal case the same assumption will be considered as in the ideal converter adding the effect of the inductance resistance R_{ind} and the switch ON resistance $R_{CE_{ON}}$ plus the forward diode drop voltage $V_{DIODE_{ON}}$. Figure 3.13 depicts the equivalent circuit diagram of the non-ideal boost converter including the ON and OFF states.

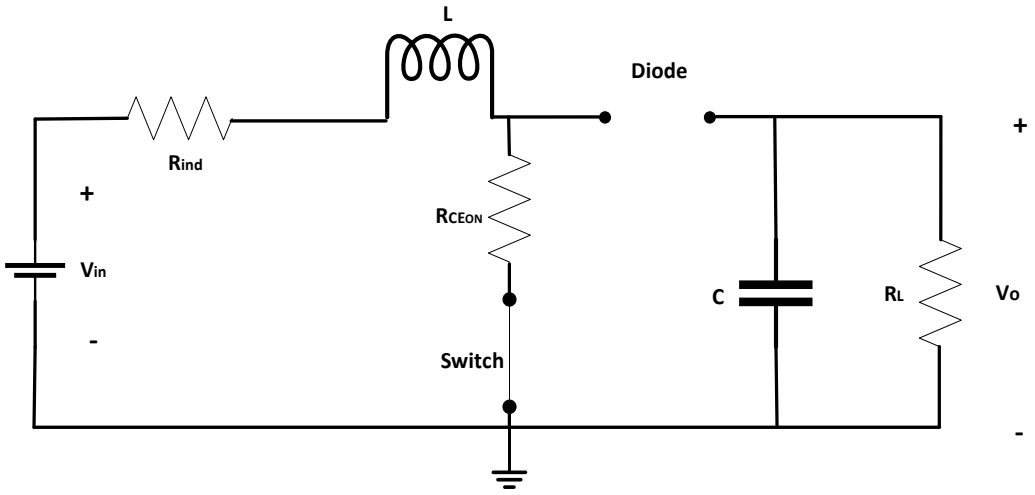


Figure 3.13.a Non-ideal boost converter ON state equivalent circuit

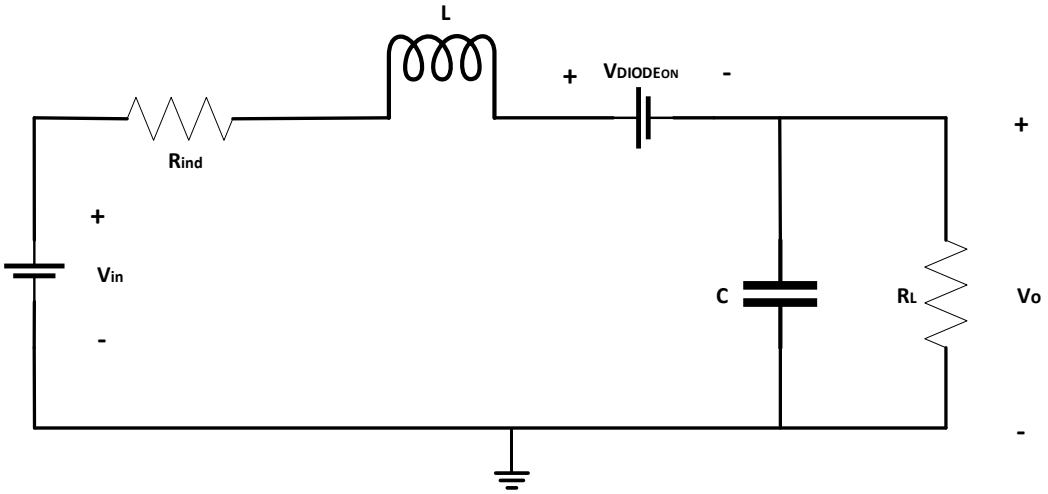


Figure 3.13.b Non-ideal boost converter OFF state equivalent circuit

Figure 3.13 Non-ideal boost converter equivalent circuit

As the switching period is T_s then the switch will be ON for DT_s and OFF for $(1-D)T_s$. So the dynamic equations for the ON state will be:

$$\begin{bmatrix} L\dfrac{di_L(t)}{dt} \\ C\dfrac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{ind}+R_{CE_{ON}}) & 0 \\ 0 & -\dfrac{1}{R} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_i(t) \\ 0 \end{bmatrix} \qquad (3.97)$$

$$y(t) = [1 \quad 0]\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} \tag{3.98}$$

And the OFF state equations:

$$\begin{bmatrix} L\dfrac{di_L(t)}{dt} \\ C\dfrac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} -R_{ind} & -1 \\ 1 & -\dfrac{1}{R} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_i(t) \\ V_{DIODE_{ON}} \end{bmatrix} \tag{3.99}$$

$$y(t) = [1 \quad 0]\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} \tag{3.100}$$

There are A_1, B_1 and C_1 matrices from the ON state dynamic equations. And A_2, B_2 and C_2 matrices from the OFF state dynamic equations. Then the averaged matrices will take the following form:

$$A = A_1 D + A_2 \acute{D} \tag{3.101}$$

$$B = B_1 D + B_2 \acute{D} \tag{3.102}$$

$$C = C_1 D + C_2 \acute{D} \tag{3.103}$$

The complete dynamic equations in state space representation obtained as follows:

$$A = \begin{bmatrix} -(R_{ind} + R_{CE_{ON}})D & -\acute{D} \\ \acute{D} & -\dfrac{1}{R} \end{bmatrix}, B = \begin{bmatrix} 1 & -\acute{D} \\ 0 & 0 \end{bmatrix}, C = [1 \quad 0] \tag{3.104}$$

$$\begin{bmatrix} L\dfrac{di_L(t)}{dt} \\ C\dfrac{dv_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{ind} + R_{CE_{ON}})D & -\acute{D} \\ \acute{D} & -\dfrac{1}{R} \end{bmatrix}\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} 1 & -\acute{D} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_i(t) \\ V_{DIODE_{ON}} \end{bmatrix} \tag{3.105}$$

$$y(t) = [1 \quad 0]\begin{bmatrix} i_L(t) \\ v_o(t) \end{bmatrix} \tag{3.106}$$

The steady state solution of the non-ideal converter will be found by assuming that $\dot{X} = 0$ and using the relation $X = A^{-1} * B * U$ as follows

$$V_o = \frac{R_{ind} * \left[-\acute{D} * \left(V_i - \acute{D} * V_{DIODE_{ON}}\right)\right]}{R_{ind} + R_{CE_{ON}} * D + \acute{D}^2} \tag{3.107}$$

To obtain the transfer function of the non-ideal converter linearisation is required in order to simplify the analysis. Linearisation is done using the following expression:

$$\frac{d\hat{x}(t)}{d(t)} = A\hat{x}(t) + B\hat{u}(t) + \big((A_1 - A_2)X + (B_1 - B_2)U\big)\hat{d}(t) \tag{3.108}$$

$$\hat{y}(t) = (-CA^{-1}B + D)U \tag{3.109}$$

After substitution the matrices A, B are as stated in (3.104) then $\frac{d\hat{x}(t)}{d(t)}$ will be:

$$\begin{bmatrix} L\dfrac{d\hat{\imath}_L(t)}{dt} \\ C\dfrac{d\hat{v}_o(t)}{dt} \end{bmatrix} = \begin{bmatrix} -(R_{ind} + R_{CE_{ON}})D & -\acute{D} \\ \acute{D} & \dfrac{1}{R} \end{bmatrix} \begin{bmatrix} \hat{\imath}_L(t) \\ \hat{v}_o(t) \end{bmatrix} \ldots$$

$$+ \begin{bmatrix} 1 & -\acute{D} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_i(t) \\ \hat{v}_{DIODE_{ON}}(t) \end{bmatrix} \begin{bmatrix} -R_{CE_{ON}} * I + V_{DIODE_{ON}} + V_o \\ -I \end{bmatrix} \hat{d}(t) \tag{3.110}$$

Using the Laplace transform the transfer function between the duty cycle as a control input and the output voltage is given in equation (3.111) assuming

$\hat{v}_i(s) = 0$:

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{\big(V_o + V_{DIODE_{ON}} - R_{CE_{ON}} * I\big) * \acute{D} - I * (LS + R_{ind} + R_{CE_{ON}} * D)}{C(LS^2 + \big(R_{ind} + R_{CE_{ON}} * D\big)S + \acute{D}^2 + \dfrac{R_{CE_{ON}} * D + R_{ind} + LS}{R}} \tag{3.111}$$

3.4.Switching Controllers Considerations

In DC transformers the controller regulates the output voltage to a requested voltage value. The controller could be designed to use different control operation methods, each of them adapted to a specific case. Mainly two different modulations have been used to derive the DC transformer's power switches. The first is the Pulse Width Modulation (PWM) operation control method. And the second is the Pulse Frequency Modulation (PFM) operation control method. Each is optimized for a specific output power range, where the PWM is well suited for high power conversion whilst the PFM is better suited for low power conversions [108].

A PWM DC transformer is a power converter which uses a fixed frequency oscillator to derive the power switches and transfer energy for input to output. The drive signal used is constant in frequency but varies in its duty cycle (ratio of power switch ON time to the total switching period). The clock frequency is fixed, and the pulse width of each clock cycle is adjusted based on the operating conditions. Whereas the PFM uses a variable frequency

clock to drive the power switches and transfer energy from the input to the output. Because the drive signal's frequency is directly controlled to regulate the output voltage, then it could be designed with constant ON time or constant OFF time [127].

With the PWM control as illustrated in figure 3.14, the regulation of the output voltage is obtained by changing the power switch's duty cycle D keeping the frequency of operation constant. The operation control with PWM is preferable by most designers, since constant frequency operation simplifies the design of the regulation feedback loop and the output filter, thus avoiding stability issues [108]. While PFM DC transformers inherently have a variable operating frequency, and therefore many system designers have concerns about using this type of architecture [127].

In contrast the PWM becomes inefficient when a light load (meaning low power) is supplied. Thus, a combination of the PWM and the FPM is needed in some applications where a high load variation is applied [108].

Generally, PWM is the most used closed loop method to control switching power supplies and is used to design a controller with a high degree of dynamic response which is required in nonlinear systems [134].

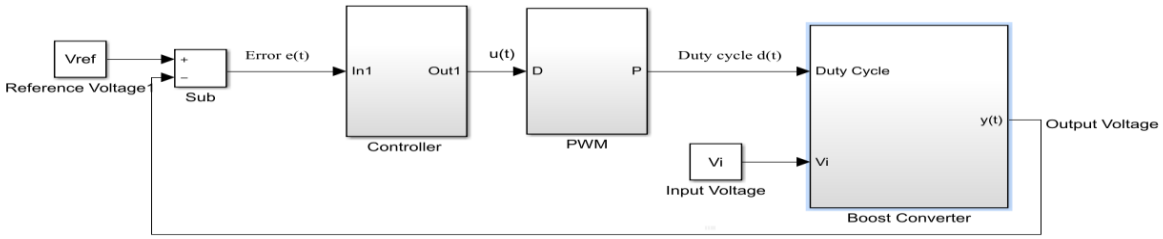


Figure 3.14 typical voltage mode PWM control of the DC-DC boost converter with feedback loop

Figure 3.15 shows the block diagram of the PWM generator. The PWM signal is generated by comparing the triangular waveform (sawtooth generator) with the DC voltage level, which is adjusted to control the ratio of ON to OFF time that is required. When the triangle is above the demand voltage, the output goes high and when the triangle is below the demand voltage, the output goes low.

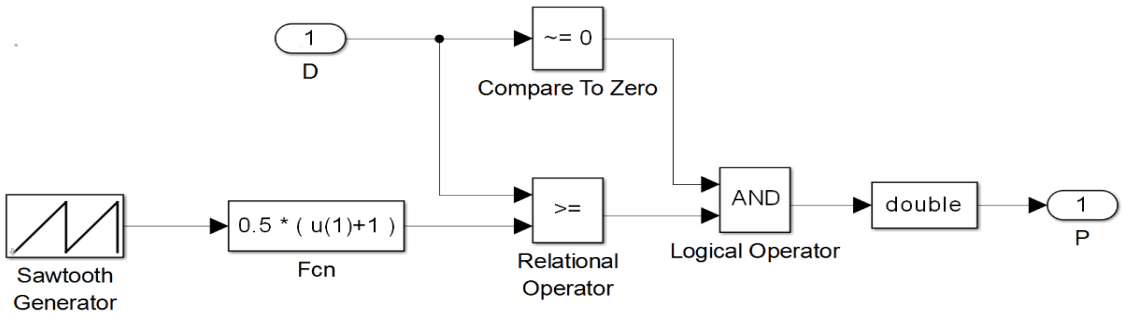


Figure 3.15 Simulink block diagram of the PWM generator

As a result, the proposed MIMO step-up DC transformer in this thesis has been designed for high voltage applications. And the PWM has been used with a voltage mode control to obtain a fixed output voltage with a more efficient power conversion.

3.5.Summary

In this chapter the theoretical background of conventional DC transformers, or DC-DC converter topologies, have been presented and discussed. The operation principles of the basic topologies in continuous and discontinuous conduction operation modes have been explained and expressed mathematically. The mathematical description of the output voltage with the input voltage; the switch's duty cycle; and other components of the circuit have been presented for the ideal and non-ideal converter. The emphasis is on the step-up DC transformer (boost DC-DC converter) topology as the proposed MIMO DC transformer is a stepping-up type. This has been designed for medium to high voltage applications utilising renewable energy sources, particularly offshore wind farms, therefore stepping-up the DC voltage to higher levels is needed in order to transfer power for long distances with less losses in the transmission lines [126].

Different types of semiconductor switching devices have been discussed considering the advantages and drawbacks of using each power switch. Therefore, the main features of the IGBTs over the mentioned switching devices make it popular and preferable to use for high voltage applications which have been utilised in the proposed MIMO step-up DC transformer.

As the conventional switching converters are nonlinear plants then small signal modelling and linearisation of the plant is required to obtain a linear model which is easier to analyse. Then in order to obtain the small signal model the mathematical modelling and the state space representation in a matrix form of the conventional boost DC-DC converter have been

derived, and as a result the transfer functions of the ideal and non-ideal boost converters have been presented.

The controller could be designed to use different control operation methods, each of them adapted to a specific case. Two different modulations have been defined: the PWM and PFM to derive the DC transformer's power switches. Each is optimized for a specific output power range.

CHAPTER FOUR

THE PROPOSED MIMO STEP-UP DC TRANSFORMER DESIGN

4.1. A Multi-String Series Connected Step-up DC Transformer Topology

In this chapter, a novel MIMO step-up DC transformer for medium to high voltage applications is proposed. A wide range of DC transformer topologies have been developed for low voltage applications, however DC transformers for high voltage DC grid applications are not as mature as for low voltage applications.

Recently, the combination of various renewable energy sources such as wind turbines, fuel cells and Photo Voltaic (PV) panels, have attracted extensive research interest because of the environmental considerations and increased reliability requirement. In such a system, Multi- Input transformers play a very important role to integrate these energy sources to supply the loads.

In general, the DC transformers can be classified as Multi-Input Single-Output (MISO), Single-Input Multi-Output (SIMO) and Multi-Input Multi-Output (MIMO) transformers. These classes will be presented in this chapter as a method that assists the researcher to design a MIMO step-up DC transformer.

In this section, a multi-string series connected step-up DC transformer topology as a MISO step-up DC transformer is proposed as a first phase in designing a MIMO step-up DC transformer topology.

As shown in Figure 4.1 m number of input DC voltage sources can be integrated to feed the load. Thus, the conversion gain of the DC transformer will be increased as well as the system will be more reliable in terms of the availability and choice of the input sources.

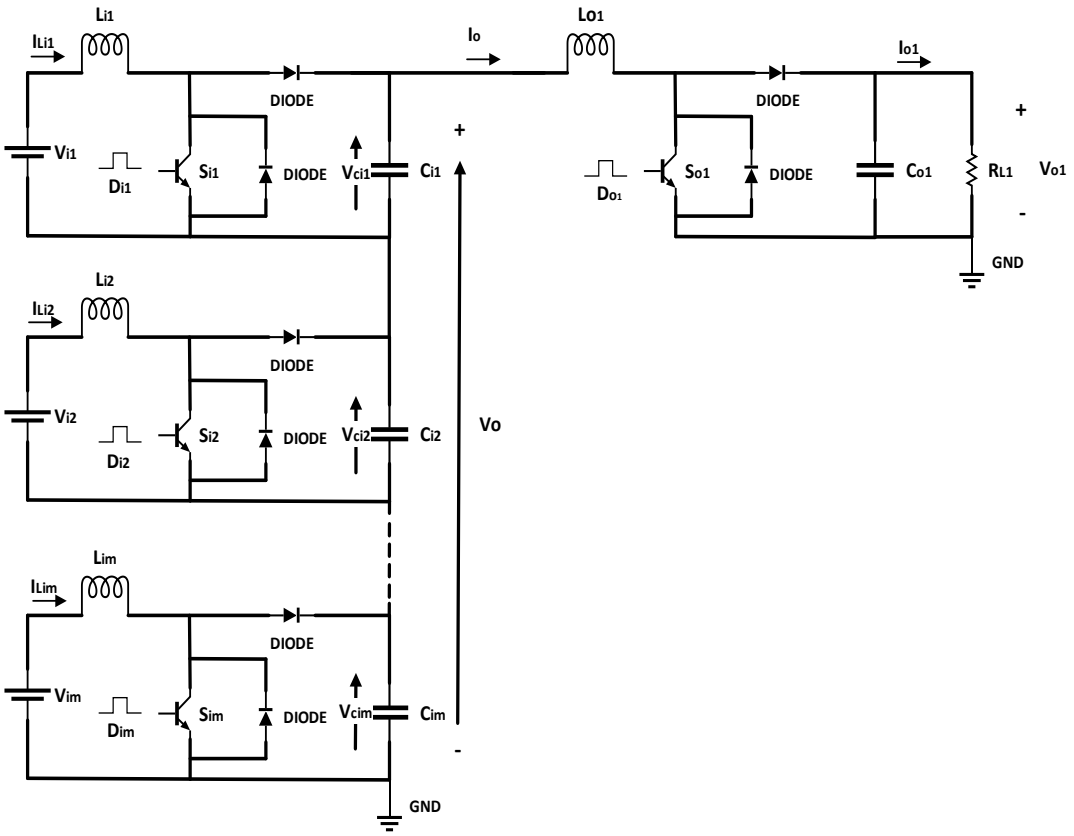


Figure 4.1 Multi-string series connected step-up DC transformer [61]

The step-up conversion gain of the proposed DC transformer depends on the power switches duty ratios D and on the number and values of the DC input voltage sources, in order to understand the relationship between the inputs and the output voltage; the mathematical equations have been derived in the next section of this chapter by assuming that the capacitors are large enough and thus in one switching cycle, their voltages are constant. Then using the inductor volt second balance approach, the average inductor voltage over one period (0-T_s) must be zero.

$$\frac{1}{T_S}\int V_L(t)dt = zero \tag{4.1}$$

$$T_S = T_{ON} + T_{OFF} \tag{4.2}$$

Where

T_S is the switching period and V_L is the inductor's voltage.

When the input switches (S_{im})conduct, the input inductors(L_{im}) will store the energy from their respective input sources(V_{im}) until the inductors' voltage will equal to the input source value. At the same time the input diodes $(Diode_{im})$ are reversed biased and no current passes through the second phase of the design which constitutes the Multi-Output (MO) stage.

While during the OFF time the input capacitors $(C_{i1}, C_{i2}, \dots, C_{im})$ will charge through the input inductor current. Consequently, as shown in figure 4.2, in the second phase of design, the output inductors$(L_{o1}, L_{o2}, \dots, L_{on})$ will store energy depending on the summation charge of the input capacitors. And the loads are supplied from the output capacitors during the OFF time of the output power switches (S_{on}). Hence, figure 4.2 shows diagrammatically the proposed MIMO step-up DC transformer topology of m inputs and n outputs where in the 1st phase of design the input stages are connected in series for adding up the input voltage thus increasing the step-up conversion gain, while in the second phase of design the output stages are connected in parallel in order to maximise the voltage level on each output.

It has been reported that the Continues Conduction Mode (CCM) is more suitable for efficient high power conversion applications especially for renewable energy system applications [42] while, Discontinues Conduction Mode (DCM) fits well for low power applications or stand-by operation [133] as well as for large load variation applications. Here for high power applications, the operation of the proposed DC transformer design is based on CCM throughout the full range of the duty cycle variation with resistive loads.

In this design the step-up voltage occurs in two phases; where the output voltage of the first phase (V_o) acts as the input voltage for the next phase. Hence, this proposed topology will provide a higher conversion ratio of the voltage, which this feature is important in high DC voltage applications.

In the proposed DC transformer topology m input sources are responsible for supplying the loads $(R_{L1}, R_{L2}, \dots, R_{Ln})$. As mentioned before the transformer is designed to operate in CCM where the current through the inductors $(I_{Li1}, I_{Li2}, \dots, I_{Lim})$ will never go to zero. In this mode the input switches$(S_{i1}, \dots, S_{im})$ are active. For each switch, a specific duty ratio is considered. This is based on the availability of the input source, the required magnitude of first phase output voltage as well as the output voltage of the second phase. For example the inductors currents $(I_{Li1}, I_{Li2}, I_{Li3}, \dots \text{ and } I_{Lim})$ can be controlled to provide the desired value by regulating $(V_{i1}, V_{i2}, V_{i3}, \dots \text{and } V_{im})$ respectively when $(S_{i1}, S_{i2}, S_{i3}, \dots \text{and } S_{im})$ are active. Therefore, the DC bus voltage $V_o = (V_{ci1} + V_{ci2} + V_{ci3+\dots.} V_{cim})$ can be regulated to any desired value solely by adjusting the duty ratios of the m input switches $(S_{i1}, S_{i2}, S_{i3}, \dots \text{and } S_{im})$. The aforementioned concept is also applicable to the second phase of design. For example, the output voltage V_{o1} is controlled by the output power switch S_{o1}, similarly S_{o2} regulates the second output voltage V_{o2}. Furthermore, each

output voltage (V_{o1}, V_{o2}, ... and V_{on}) will be regulated by all input power switches(S_{i1}, S_{i2}, ... and S_{im}).

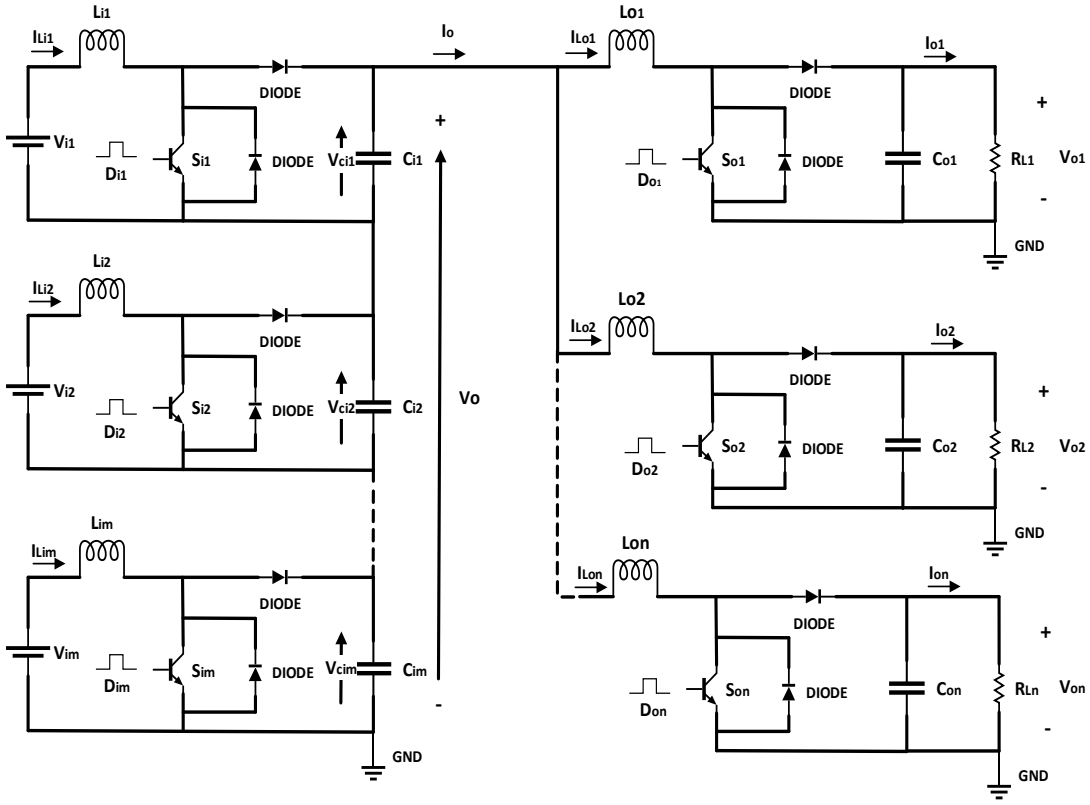


Figure 4.2 The proposed MIMO step-up DC transformer topology [123]

4.2.Operation of MIMO DC Transformer in Continues Conduction Mode

In order to derive the mathematical equations of the proposed MIMO DC transformer a comprehensive understanding of the transformer's structure and its operation principle is needed.

The main reason of having a MIMO structure is to integrate the available input sources for supplying the loads. That means the percentage of the absorbed energy from each source will be reduced compared with single input systems. To achieve the functionality of the designed MIMO topology the input power switches S_{i1} to S_{im} should operate simultaneously (active at the same time), whereas the output power switches S_{o1} to S_{on} can be operated simultaneously or sequentially. In order to minimize the switching losses in the system the appropriate switching algorithm has been chosen where the output switches will be active at the same time. When the power switches in the system operate (simultaneously) at the same time then no extra losses could be obtained [42].

According to the switches' states, there are four different switching states in one switching period as shown in figure 4.3. Figure 4.3 represents a three-input double-output

configuration which is taken here as an example for the proposed MIMO DC transformer. For each state, the steady state analysis of the inductors' and capacitors' equations have been investigated as follows:

a) Switching state 1: In this state, the input power switches (S_{i1}, S_{i2} and S_{i3}) are turned ON and the input stage diodes are reversely biased while the output switches (S_{o1} and S_{o2}) are turned OFF. Assuming that the output capacitors (C_{o1}, C_{o2}) are fully charged and the power is delivered to the loads (R_{L1}, R_{L2}). The equivalent circuit of the proposed transformer in this state is shown in figure 4.3(a). In this state, (V_{i1}, V_{i2} and V_{i3}) sources will respectively charge their corresponding inductors (L_{i1}, L_{i2} and L_{i3}) by increasing their currents and at the same time the capacitors (C_{i1}, C_{i2} and C_{i3}) will discharge.

The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= V_{i1} \\ L_{i2}\frac{di}{dt} &= V_{i2} \\ L_{i3}\frac{di}{dt} &= V_{i3} \\ C_{i1}\frac{dv_{ci1}}{dt} &= -I_o \\ C_{i2}\frac{dv_{ci2}}{dt} &= -I_o \\ C_{i3}\frac{dv_{ci3}}{dt} &= -I_o \\ L_{o1}\frac{di}{dt} &= V_o - V_{co1} \\ L_{o2}\frac{di}{dt} &= V_o - V_{co2} \\ C_{o1}\frac{dv_{co1}}{dt} &= I_{Lo1} - \frac{V_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= I_{Lo2} - \frac{V_{o2}}{R_{L2}} \end{aligned}\right\} \quad (4.3)$$

b) Switching state 2: In this state, the input power switches (S_{i1}, S_{i2} and S_{i3}) are still ON, and the output switches (S_{o1} and S_{o2}) are turned ON. When the input switches are ON the input stage diodes are reversed biased. Assuming that the input capacitors (C_{i1}, C_{i2} and C_{i3}) are fully charged, thus the power will deliver to the loads (R_{L1}, R_{L2}). Equivalent circuit of proposed transformer in this state is shown in figure 4.3(b). In this state, (V_{i1}, V_{i2} and V_{i3}) sources will charge the inductors (L_{i1}, L_{i2} and L_{i3}) also the output inductors ($L_{o1}$and L_{o2}) are charged from the input capacitors

(C_{i1}, C_{i2} and C_{i3}). Consequently, the inductors' current ($I_{Lo1}$and I_{Lo2}) will increases and at the same time capacitors ($C_{o1}$and C_{o2}) will discharge. The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= V_{i1} \\ L_{i2}\frac{di}{dt} &= V_{i2} \\ L_{i3}\frac{di}{dt} &= V_{i3} \\ L_{o1}\frac{di}{dt} &= V_o \\ L_{o2}\frac{di}{dt} &= V_o \\ C_{i1}\frac{dv_{ci1}}{dt} &= -(I_{Lo1} + I_{Lo2}) \\ C_{i2}\frac{dv_{ci2}}{dt} &= -(I_{Lo1} + I_{Lo2}) \\ C_{i3}\frac{dv_{ci3}}{dt} &= -(I_{Lo1} + I_{Lo2}) \\ C_{o1}\frac{dv_{co1}}{dt} &= \frac{-V_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= \frac{-V_{o2}}{R_{L2}} \end{aligned}\right\} \quad (4.4)$$

c) Switching state 3: In this state, the input power switches (S_{i1}, S_{i2} and S_{i3}) are turned OFF, and the output switches (S_{o1} and S_{o2}) are turned OFF. When the input switches are OFF the input stage diodes are forward biased. In this state, the stored energy in the input inductors will deliver to charge the input capacitors (C_{i1}, C_{i2} and C_{i3}). In addition, the stored energy in the output inductors will deliver to charge the output capacitors ($C_{o1}$and C_{o2}), as well as to deliver the stored energy in($C_{o1}$and C_{o2}) to the loads (R_{L1}, R_{L2}). The equivalent circuit of the proposed transformer in this state is shown in figure 4.3(c). In this state, the inductors' current (I_{Li1}, I_{Li2} and I_{Li3}) will decrease and the capacitors (C_{i1}, C_{i2} and C_{i3}) will charge. The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= V_{i1} - V_{ci1} \\ L_{i2}\frac{di}{dt} &= V_{i2} - V_{ci2} \\ L_{i3}\frac{di}{dt} &= V_{i3} - V_{ci3} \\ L_{o1}\frac{di}{dt} &= V_{o} - V_{co1} \\ L_{o2}\frac{di}{dt} &= V_{o} - V_{co2} \\ C_{i1}\frac{dv_{ci1}}{dt} &= I_{Li1} - I_{o} \\ C_{i2}\frac{dv_{ci2}}{dt} &= I_{Li2} - I_{o} \\ C_{i3}\frac{dv_{ci3}}{dt} &= I_{Li3} - I_{o} \\ C_{o1}\frac{dv_{co1}}{dt} &= I_{Lo1} - \frac{V_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= I_{Lo2} - \frac{V_{o2}}{R_{L2}} \end{aligned}\right\} \quad (4.5)$$

d) Switching state 4: In this state, the input power switches (S_{i1}, S_{i2} and S_{i3}) are still OFF, and the output switches (S_{o1} and S_{o2}) are turned ON. When the input switches are OFF the input stage diodes are forward biased. In this state, the stored energy in the input inductors(L_{i1}, L_{i2} and L_{i3}) keep charging the capacitors (C_{i1}, C_{i2} and C_{i3}). In addition, the stored energy in the output inductors ($L_{o1}$and L_{o2}) will charge ($C_{o1}$and C_{o2}) when their respective corresponding switches (S_{o1} and S_{o2}) are in OFF mode position. Then the stored energy in($C_{o1}$and C_{o2}) are discharged through (R_{L1}, R_{L2}). The equivalent circuit of the proposed DC transformer in this state is shown in figure 4.3(d). In this state, the capacitors (C_{i1}, C_{i2} and C_{i3}) are charged and the equations representing voltage and current for inductors and capacitors are expressed as follows:

$$
\left.
\begin{aligned}
L_{i1}\frac{di}{dt} &= V_{i1} - V_{ci1} \\
L_{i2}\frac{di}{dt} &= V_{i2} - V_{ci2} \\
L_{i3}\frac{di}{dt} &= V_{i3} - V_{ic3} \\
L_{o1}\frac{di}{dt} &= V_o \\
L_{o2}\frac{di}{dt} &= V_o \\
C_{i1}\frac{dv_o}{dt} &= I_{Li1} - I_o \\
C_{i2}\frac{dv_o}{dt} &= I_{Li2} - I_o \\
C_{i3}\frac{dv_o}{dt} &= I_{Li3} - I_o \\
C_{o1}\frac{dv_{co1}}{dt} &= \frac{-V_{o1}}{R_{L1}} \\
C_{o2}\frac{dv_{co2}}{dt} &= \frac{-V_{o2}}{R_{L2}}
\end{aligned}
\right\} \qquad (4.6)
$$

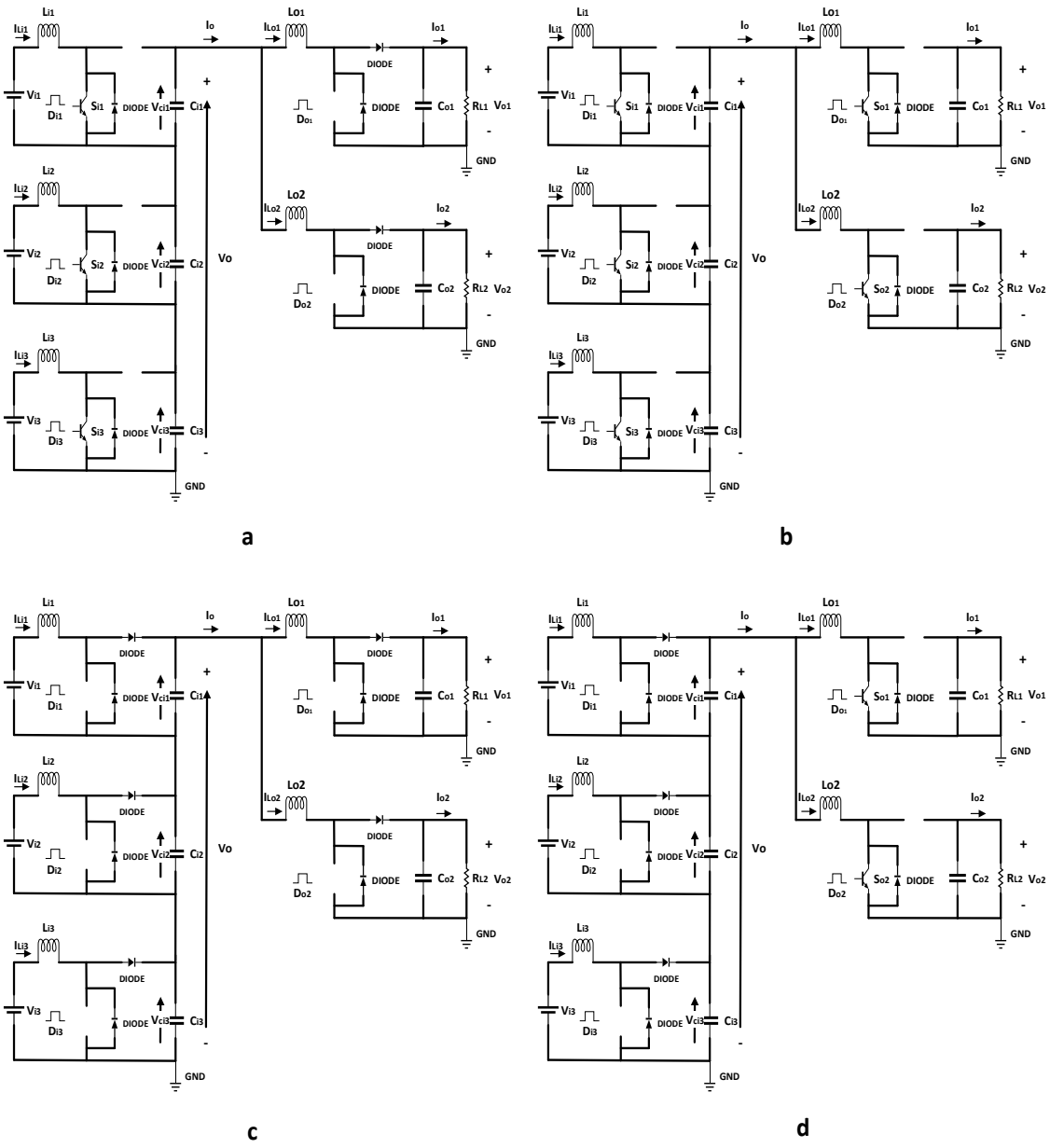


Figure 4.3 Equivalent circuit of step-up DC transformer operation mode, (a) switching state 1, (b) switching state 2, (c) switching state 3, (d) switching state 4.

Assuming that the capacitors are large enough and their voltages are constant in one switching cycle. From the inductor volt second balance approach which means that the average inductor voltage over one period must be zero.

$$\frac{1}{T_S}\int V_L(t)dt = zero \tag{4.7}$$

By applying KVL on each input module during the ON and OFF time, the voltage across the inductor is given by:

$$V_{L_{ON}} = V_{i1}$$

$$V_{L_{OFF}} = V_{i1} - V_{ci1}$$

$$D_{i1}TV_{i1} + (1 - D_{i1})T(V_{i1} - V_{ci1}) = 0 \quad (4.8)$$

$$D_{i1}V_{i1} + V_{i1}(1 - D_{i1}) = V_{ci1}(1 - D_{i1}) \quad (4.9)$$

$$\therefore V_{ci1} = \frac{V_{i1}}{1 - D_{i1}} \quad (4.10)$$

$$D_{i2}TV_{i2} + (1 - D_{i2})T(V_{i2} - V_{ci2}) = 0 \quad (4.11)$$

$$D_{i2}V_{i2} + V_{i2}(1 - D_{i2}) = V_{ci2}(1 - D_{i2}) \quad (4.12)$$

$$\therefore V_{ci2} = \frac{V_{i2}}{1 - D_{i2}} \quad (4.13)$$

And for the third input as previous

$$\therefore V_{ci3} = \frac{V_{i3}}{1 - D_{i3}} \quad (4.14)$$

The DC voltage of the string series connected will be

$$\therefore V_o = \frac{V_{i1}}{1 - D_{i1}} + \frac{V_{i2}}{1 - D_{i2}} + \frac{V_{i3}}{1 - D_{i3}} + \cdots + \frac{V_{im}}{1 - D_{im}} \quad (4.15)$$

The general equation for (m) input of the MISO DC transformer will be

$$\therefore V_{o1} = [\sum_{k=1}^{k=m} V_{ik} \frac{1}{1 - D_{ik}}](\frac{1}{1 - D_{o1}}) \quad (4.16)$$

Where

V_o is the DC output voltage.

V_{ik} is the DC input voltage.

$D_{ik}$is the Duty cycle of the input power switches.

m is the number of DC transformer input sources.

D_{o1} is the duty cycle of the output power switch.

4.2.1 Mathematical Derivation of the Proposed MIMO DC Transformer in Continues Conduction Mode

4.2.1.1 Ideal MIMO step-up DC transformer

Based on the expressions derived in the previous section, the general mathematical equations of the proposed MIMO step-up DC transformer have been derived by assuming that the system is lossless (ideal components). The DC bus voltage V_o will be:

$$V_o = \frac{V_{i1}}{1 - D_{i1}} + \frac{V_{i2}}{1 - D_{i2}} + \frac{V_{i3}}{1 - D_{i3}} + \cdots + \frac{V_{im}}{1 - D_{im}} \tag{4.17}$$

$$V_o = \left[\sum_{k=1}^{k=m} V_{ik} \frac{1}{1 - D_{ik}}\right] \tag{4.18}$$

V_{o1} = the output voltage of the first stage * the conversion ratio of the next stage

$$V_{o1} = \left[\frac{V_{i1}}{1 - D_{i1}} + \frac{V_{i2}}{1 - D_{i2}} + \frac{V_{i3}}{1 - D_{i3}} + \cdots + \frac{V_{im}}{1 - D_{im}}\right]\left[\frac{1}{1 - D_{o1}}\right] \tag{4.19}$$

Then the DC output voltage for n outputs (V_{on}) will be:

$$\therefore V_{on} = \left[\sum_{k=1}^{k=m} V_{ik} \frac{1}{1 - D_{ik}}\right]\left[\frac{1}{1 - D_{on}}\right] \tag{4.20}$$

Where

V_{on} is the DC output voltage.

V_{im} is the DC input voltage.

D_{im} is the Duty cycle of the input power switches.

D_{on} is the Duty cycle of the output power switches.

n is the number of DC transformer outputs.

Equation (4.20) suggests that each output of the proposed topology could have its own voltage level as is regulated by the duty cycle of all input power switches as well as the duty cycle of that output. Thus, this design can provide different output voltage levels for grids connection.

The step-up conversion gain of the proposed ideal MIMO DC transformer expressed in equation (4.21) shows a high conversion gain could be obtained.

$$M(D) = \left[\sum_{k=1}^{k=m} \frac{1}{1-D_{ik}}\right]\left[\frac{1}{1-D_{on}}\right] \quad (4.21)$$

Figure 4.4 depicts the theoretical and measured (simulated via MATLAB) characteristics of the output voltage as a function of the input voltage with good correlation.

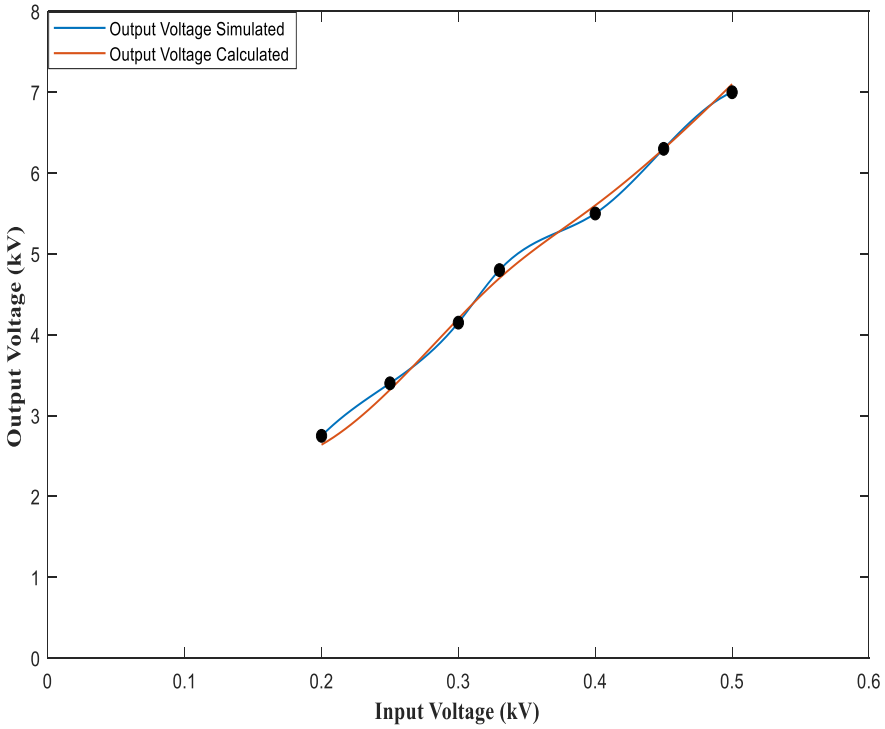


Figure 4.4 the relation between the output DC voltages V_{o1} and the input DC voltage V_{i1} with $D_{i1} = 67\%$ and $D_{o1} = 80\%$

4.2.1.2 Non-Ideal MIMO step-up DC transformer

In reality there is no ideal system without losses; electronic switches, diodes and the parasitic elements in the circuit will contribute to losses in the system. For demonstration purposes a SISO step-up DC transformer as shown in figure 4.5 is taken as a template to find out how these components effect on the output DC voltage.

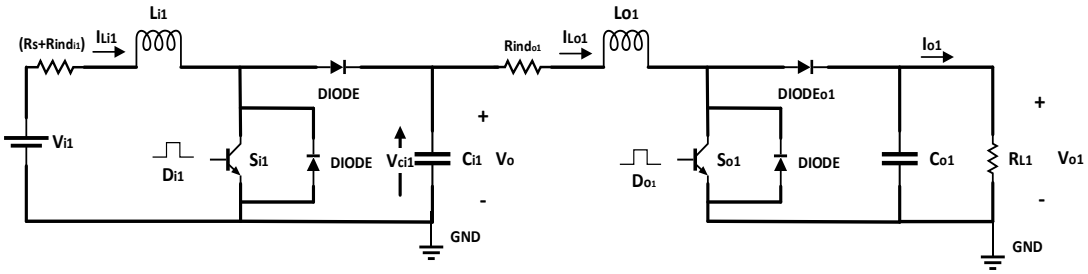


Figure 4.5 A SISO step-up DC transformer topology

According to the circuit in figure 4.5 the mathematical equation of V_{o1} has been derived as follow taking into consideration the conduction and switching losses in the system:

Mode 1: S_{i1}: ON and S_{o1}: OFF

$$V_{L_{i1}-ON} = V_{i1} - V_{S_{i1}-ON} - I_{L_{i1}}(R_s + R_{ind_{i1}}) \tag{4.22}$$

Mode 2: S_{i1}: OFF and S_{o1}: OFF

$$V_{L_{i1}-OFF} = V_{i1} - V_{DIODE-ON} - V_o \tag{4.23}$$

From the inductor volt second balance approach

$$\frac{1}{T_S}\int V_{Li1}(t)dt = zero \tag{4.24}$$

$$V_o(1 - D_{i1}) = V_{i1}D_{i1} - V_{S_{i1}-ON}D_{i1} - I_{L_{i1}}(R_S - R_{ind_{i1}})D_{i1} + V_{i1}(1 - \cdots D_{i1}) - V_{DIODE-ON}(1 - D_{i1}) \tag{4.25}$$

Then

$$V_o = \frac{1}{1 - D_{i1}}V_{i1} - \frac{D_{i1}}{1 - D_{i1}}V_{S_{i1}-ON} - \frac{D_{i1}}{1 - D_{i1}}I_{L_{i1}}(R_S - R_{ind_{i1}}) - V_{DIODE-ON} \tag{4.26}$$

To compute V_{o1} the following criteria needs to be met which are defined as:

Mode 3: S_{i1}: ON and S_{o1}: ON, assuming that C_{i1} is fully charged

$$V_{L_{o1}-ON} = V_o - V_{S_{o1}-ON} - I_{L_{o1}}R_{ind_{o1}} \tag{4.27}$$

And when S_{o1}: OFF

$$V_{L_{o1}-OFF} = V_o - V_{DIODEo1-ON} - V_{o_1} \tag{4.28}$$

$$V_{o_1}(1 - D_{o1}) = V_o - V_{S_{o1}-ON}D_{o1} - I_{L_{o1}}R_{ind_{o1}}D_{o1} - V_{DIODEo1-ON} \tag{4.29}$$

$$V_{o_1} = \frac{1}{(1 - D_{o1})}V_o - \frac{1}{(1 - D_{o1})}V_{S_{o1}-ON} \cdots - \frac{1}{(1 - D_{o1})}I_{L_{o1}}R_{ind_{o1}} - V_{DIODEo1-ON} \tag{4.30}$$

After substitution:

$$V_{o_1} = \frac{1}{(1-D_{o1})}\frac{1}{(1-D_{i1})}V_{i1} - \frac{1}{(1-D_{o1})}\frac{D_{i1}}{(1-D_{i1})}V_{S_{i1}-ON} - \frac{D_{i1}}{(1-D_{i1})}\frac{1}{(1-D_{o1})}I_{L_{i1}}(R_S + R_{ind_{i1}}) - \cdots V_{DIODE-ON} - \frac{D_{o1}}{1-D_{o1}}V_{S_{o1}-ON} - \cdots \frac{D_{o1}}{1-D_{o1}}I_{L_{o1}}R_{ind_{o1}} - V_{DIODEo1-ON} \quad (4.31)$$

Thus, the general equation of the proposed non-ideal MIMO DC transformer output voltage will be:

$$V_{on(non-ideal)} = \left[\frac{1}{1-D_{on}}\right]\left[\sum_{k=1}^{k=m} V_{ik}\frac{1}{1-D_{ik}}\right] - \cdots$$

$$\left[\sum_{\mathrm{k=1}}^{\mathrm{k=m}} \mathrm{V}_{S_{ik-ON}}\frac{1}{(1-\mathrm{D_{ik}})(1-D_{on})} - \frac{1}{(1-\mathrm{D_{ik}})(1-D_{on})}I_{L_k}(R_{S_{ik}} - R_{ind_{ik}}) - \mathrm{V}_{DIODE_{ik-ON}}\right] - \cdots \quad (4.32)$$

$$\left[\sum_{j=1}^{j=n} \mathrm{V}_{S_{oj-ON}}\left(\frac{D_{oj}}{1-D_{oj}}\right) - I_{L_{oj}}R_{ind_{oj}}\left(\frac{D_{oj}}{1-D_{oj}}\right) - \mathrm{V}_{DIODE_{oj-ON}}\right]$$

Where

$\mathrm{V}_{S_{ik-ON}}$ is the input IGBT-ON state voltage drop which is between two to three volts.

$\mathrm{V}_{S_{oj-ON}}$ is the output IGBT-ON state voltage drop which is between two to three volts.

$\mathrm{V}_{DIODE_{k,oj-ON}}$ is the diode forward voltage.

$R_{S_{ik}}$ and R_{ind_k} are the series resistances of the voltage source and the inductor respectively.

$I_{L_{ik,oj}}$ is the input and output inductor current.

Further details about the power losses in the system will be discussed in the next section of this chapter.

4.3.The Proposed MIMO DC Transformer Specifications

In this section the specifications of the designed MIMO step-up DC transformer will be presented and discussed in detail. There are the inductors and capacitors size, optimal operating frequency of the switches for $0.188\,MW$, $(350/11000)\,V$ step-up DC transformer. Also, discussed is the effect of the switches' operating frequency on the performance of the proposed transformer.

4.3.1. Passive Components Sizing

In the proposed m inputs n outputs DC transformer $(m+n)$ inductors and capacitors are utilised in the design. Each inductor and capacitor need to be sized to a certain value based on the requirements. For three-input double-output step-up DC transformer configuration shown in figure 4.6, the set predefined requirements have been set as follows:

The input voltage sources of the 1st phase: $V_{i1} = 350\,V\,, V_{i2} = 700\,V, V_{i3} = 500\,V$

The output voltage of the1st phase (stage) known as the DC bus voltage or as an input for the 2nd phase: $V_o = V_{ci1} + V_{ci2} + V_{ci3} = 4\,kV$

The output voltage of the 2nd phase: $V_{o1} = 8\,kV, V_{o2} = 11\,kV$

A fixed operating frequency is considered for all the switches: $f_s = 1\,kHz$

A fixed value is assumed for all the resistive loads: $R_L = 1\,k\Omega$

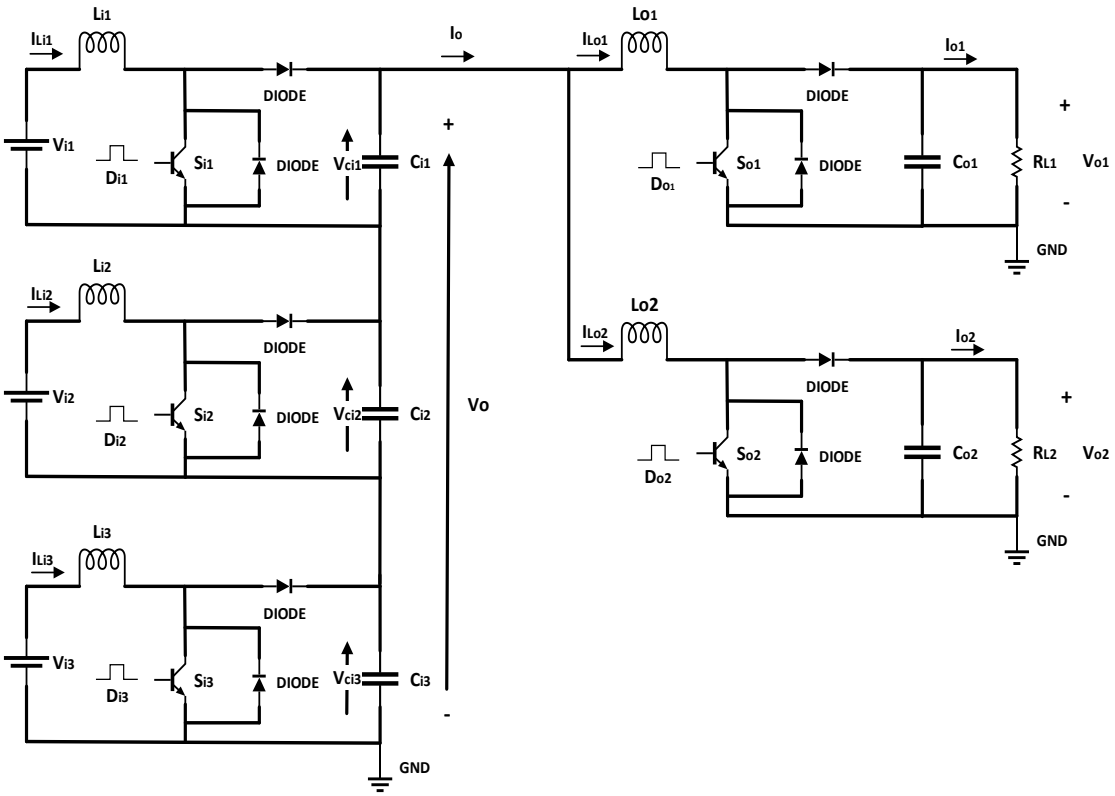


Figure 4.6 Three-input double-output step-up DC transformer topology

The DC bus voltage (V_o) value has been used here to determine the ratio between the input sources(V_{im}) and the required output voltage level (V_{on}). This enables the percentage of each input source for the formation of (V_o) for cases where the input sources are made of different types of renewable sources. Also, for cases where the price or availability may dictates the composition of the DC bus voltage (V_o) and subsequently the output voltage (V_{on}). In another word, this ratio determines the duty cycle of individual power switches for such cases.

For example, if percentage composition of each input source for formation of the DC bus voltage (V_o) be as:

$$V_{ci1} = 25\%, V_{ci2} = 44\% \text{ and } V_{ci3} = 31\%$$

Then

$$V_{ci1} = V_o * 0.25 = 1000\ volts$$

$$V_{ci2} = V_o * 0.44 = 1750\ volts$$

$$V_{ci3} = V_o * 0.31 = 1250\ volts$$

Thereafter, the duty cycle (D_{im})of each power switch on the input side could be found as:

$$D_{im} = 1 - \frac{V_{im}}{V_{cim}} \tag{4.33}$$

With the aid of data obtained earlier and equation (4.33), the switches' duty cycle are:

$$D_{i1} = 0.65$$

$$D_{i2} = D_{i3} = 0.6$$

Similarly, the duty cycle or duty ratio of the output power switches is expressed as:

$$D_{on} = 1 - \frac{V_o}{V_{on}} \quad (4.33A)$$

Substituting for V_o and V_{on} in equation (4.33A), the corresponding duty cycles will be:

$$D_{o1} = 0.5\,, D_{o2} = 0.63$$

According to this the inductors L and the capacitors C of three-input double-output step-up DC transformer could be found.

- Inductors selection

The inductance could be calculated using the following expression:

$$V_{Li} = L_i \frac{di}{dt} \tag{4.34}$$

$$L_i = V_{Li} \frac{dt}{di} \tag{4.35}$$

Where

V_{Li} is the voltage across the inductor.

dt is the time duration in second.

di is the ripple inductor current.

Integrating equation (4.35) between 0 and T_s yields:

$$\int_0^{T_s} V_{Li}\, dt = \int_0^{T_s} L_i\, di \tag{4.36}$$

Where T_s is the switching period in second.

Or

$$\int_0^{T_s} V_{Li}\, dt = L_i \int_0^{T_s} di \tag{4.37}$$

Or

$$\int_0^{T_s} V_{Li}\, dt = L_i \Delta I_{Li} \tag{4.38}$$

The inductor's voltage over one switching period is $V_{Li} = V_i D_i$, then the equation (4.38) becomes:

$$V_i D_i T_S = L_i\, \Delta I_{Li} \tag{4.39}$$

All the inputs of the proposed design are connected in such a way where each input is individually grounded thus, the input inductors current will be regulated by its corresponding power switch duty cycle which expressed in equation (4.39). Therefore, the equation (4.40) expresses the general form representation of each input inductance after substituting equation (4.33) into equation (4.39).

$$L_{im} \geq \frac{V_{im}\,(V_{cim} - V_{im})}{V_{cim}\, f_s\, \Delta I_{Lim}} \tag{4.40}$$

Where

ΔI_{Lim} is the Inductor ripple current and it is reported that practically $\Delta I_{Li} < 20\%$ of maximum output current [128].

$m = 1,2,3, \ldots$ represents the integer number of inputs of the proposed DC transformer.

It is clear from equation (4.40) that the higher the inductance value, the smaller the ripple current.

To find the inductance value the ripple current must be calculated.

$$\Delta I_{Lim} = 20\% * \left(\frac{V_{cim}}{V_{im}} * I_{cim}\right) \tag{4.41}$$

The relation between the input and output current of each input of the proposed design is:

$$I_{cim} = (1 - D_{im}) I_{im} \tag{4.42}$$

In order to calculate the input inductors' current, it is necessary to compute the output current of the second phase of design which are:

$$I_{o1} = \frac{V_{o1}}{R_{L1}} = 8\ A \tag{4.43}$$

$$I_{o2} = \frac{V_{o2}}{R_{L2}} = 11\ A \tag{4.44}$$

It is now possible to express and calculate the output current I_o of the first phase design (series or string connected converters) from the following relations:

$$I_o = I_{Lo1} + I_{Lo2} \tag{4.45}$$

$$I_o = \frac{I_{o1}}{(1 - D_{o1})} + \frac{I_{o2}}{(1 - D_{o2})} = 46.25\ A \tag{4.46}$$

With the knowledge of the input inductors' current as:

$$I_{Lim} = \frac{I_o}{(1 - D_{im})} \tag{4.47}$$

The input inductors' current for each module is calculated as:

$$I_{Li1} = 134.2\ A$$

$$I_{Li2} = I_{Li3} = 117.5\ A$$

The above computed input inductors' currents are different. This is related to different voltage sources and different duty cycle values of converters. However, due to the connection of the modules (converters) output in the 1st phase of the proposed DC transformer, the value of the input inductors' current will eventually become equal to each other after approximately 1.0 second from the start of the simulation. Based on this finding and also assuming that $R_L = R_{L1} = R_{L2}$ the input inductors' current could be expressed from the power balanced relationship.

$$Input\ Power_{total} = Output\ Power_{total}$$

$$I_{Li1}\mathrm{V_{i1}} + I_{Li2}\mathrm{V_{i2}} + I_{Li3}\mathrm{V_{i3}} = I_{o1}\mathrm{V_{o1}} + I_{o2}\mathrm{V_{o2}} \tag{4.48}$$

For the reason of simplicity, here it is assumed that the three-input modules are identical. Hence, the inductor current is expressed as:

$$I_{Li} = \frac{{V_o}^2(\frac{1}{(1-D_{o1})^2} + \frac{1}{(1-D_{o2})^2})}{(3V_i)R_L} \quad (4.49)$$

After finding value of inductors' currents and arbitrary prescribing the inductance ripple current, the inductance of each input module for operation in CCM the following criteria must satisfy:

$$L_{im} \geq \frac{V_{im}\,(V_{cim} - V_{im}\,)}{V_{cim}\,f_s\,\Delta I_{Lim}} \quad (4.50)$$

The value of three input inductances are found to be:

$$L_{i1} \geq 677.1\ \mu H$$

$$L_{i2} \geq 2.4\ mH$$

$$L_{i3} \geq 1.3\ mH$$

Similarly, the output inductor and the output ripple current are expressed as:

$$L_{on} \geq \frac{V_{on}\,(V_{con} - V_{on}\,)}{V_{con}\,f_s\,\Delta I_{Lon}} \quad (4.51)$$

$$\Delta I_{Lon} = 20\% * \left(\frac{V_{on}}{V_o} * I_{on}\right) \quad (4.52)$$

Where $n = 1,2,3,$ ... is the integer number of outputs of the proposed DC transformer.

Then through substitution of relevant data in equation (4.51) the output inductors' values will be:

$$L_{o1} \geq 91\ mH$$

$$L_{o2} \geq 421\ mH$$

It is clear that for three-input double-output DC transformer of the proposed type, there are five inductors which now have been sized or calculated.

Theoretically the proposed DC transformer could have m and n number of inputs and outputs respectively. However, in practice, this may not be possible due to constraints that may exist in the available number of input sources and output terminals. During this study,

tentative observation during simulations has revealed that, the latter could be without constraints if the following conditions are considered:

$$D_{o1} = D_{o2} = D_{o-min}$$

And

$$(I_{Lo1} + I_{Lo2}) * (1 - D_{o-min}) \leq I_{o-min} \tag{4.53}$$

In general, for n outputs

$$I_o \geq \sum_{k=1}^{k=n} \frac{I_{ok}}{(1 - D_{ok})} \tag{4.54}$$

- Capacitors selection

The function of the capacitor is to filter the inductor current ripple and deliver a stable output voltage. The following equations have been used to define the value of the output capacitors.

$$I_{ci} = C_i \frac{dv_{ci}}{dt} \tag{4.55}$$

Integrating both sides of (4.55) yields:

$$\int_0^{T_s} I_{ci}\, dt = \int_0^{T_s} C_i\, dv_{ci} \tag{4.56}$$

Or

$$I_{ci} D_i T_S = C_i\, \Delta V_{ci} \tag{4.57}$$

Each input module could be designed as an individual converter, where each capacitor voltage will be regulated by its switch's duty cycle as expressed in equation (4.57).

This will lead to the general representation of the input capacitors expression in equation (4.58)

$$C_{im} \geq \frac{I_o D_{im}}{\Delta V_{cim} f_s} \tag{4.58}$$

Where

($I_o = I_{ci}$) and ΔV_{cim} is the input capacitors' peak-to-peak ripple voltage which is reported that it is practically $\Delta V_{cim} < 5\%$ of the output voltage [129].

Based on this the three input capacitors' peak-to-peak ripple voltage will be:

$$\Delta V_{ci1} = 0.05 * 1\ kV = 50\ V$$

$$\Delta V_{ci2} = 0.05 * 1.75\ kV = 87.5\ V$$

$$\Delta V_{ci3} = 0.05 * 1.25\ kV = 62.5\ V$$

Then through substitution of relevant data in equation (4.58) the input capacitors' values will be:

$$C_{i1} \geq 19.1\ mF$$

$$C_{i2} \geq 5.8\ mF$$

$$C_{i3} \geq 11.3\ mF$$

Similarly, the output capacitors can be calculated from the following expression:

$$C_{on} \geq \frac{I_{on} D_{on}}{\Delta V_{on}\ f_s} \tag{4.59}$$

Then for $\Delta V_{o1} < 400\ V$ and $\Delta V_{o2} < 550\ V$ as a peak-to-peak ripple voltage for the two outputs, the output capacitors values will be:

$$C_{o1} \geq 25.1\ \mu F$$

$$C_{o2} \geq 31.5\ \mu F$$

The proposed DC transformer design has been validated through MATLAB/SIMULINK software and the simulations have been performed of a three-input double-output DC transformer. The simulation results are shown in figures 4.7 – 4.9.

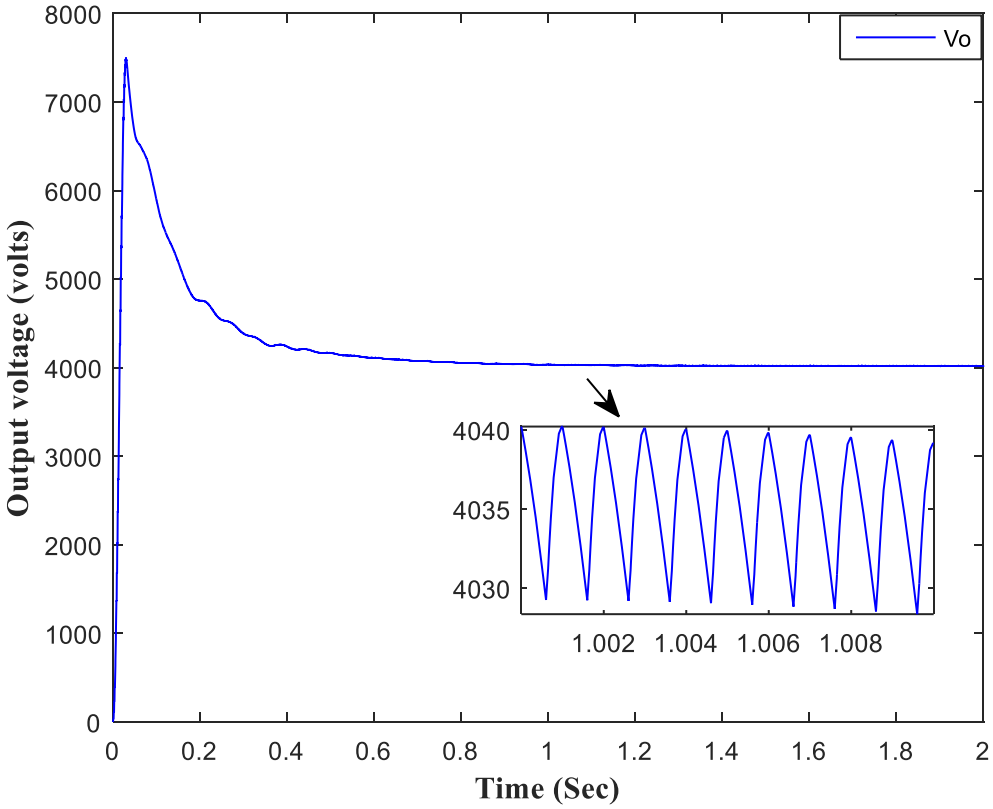


Figure 4.7 The DC bus voltage response curve V_o of the proposed three-input double-output DC transformer

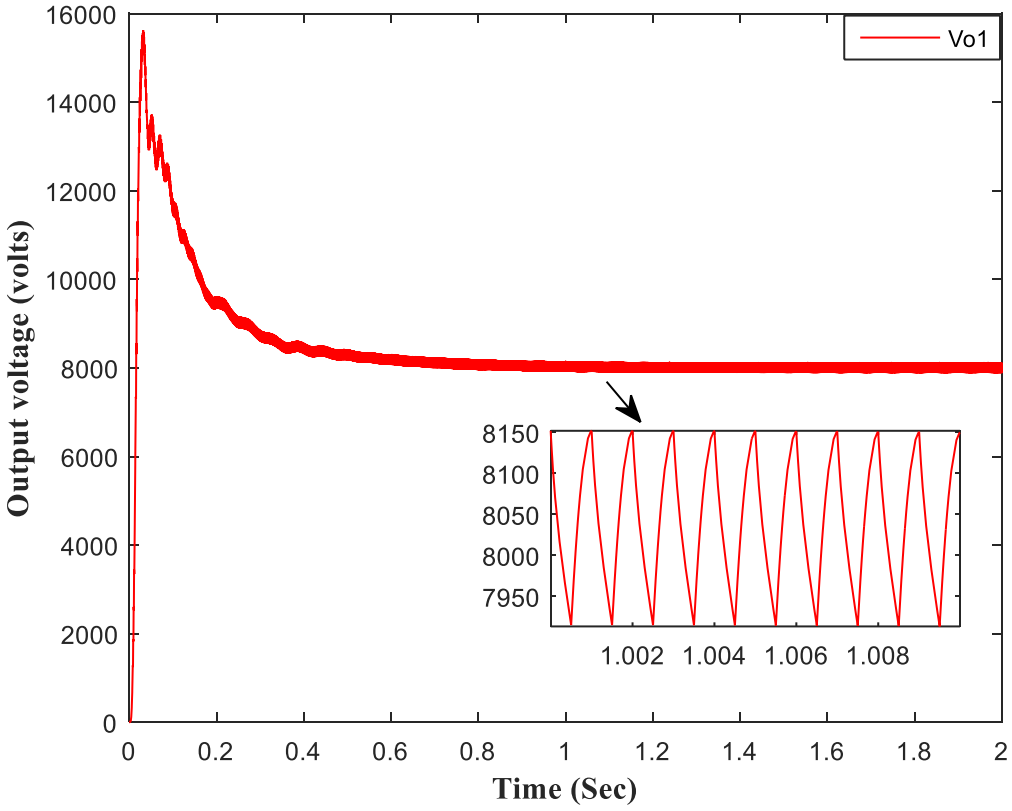


Figure 4.8 The output voltage response curve V_{o1} of the proposed three-input double-output DC transformer

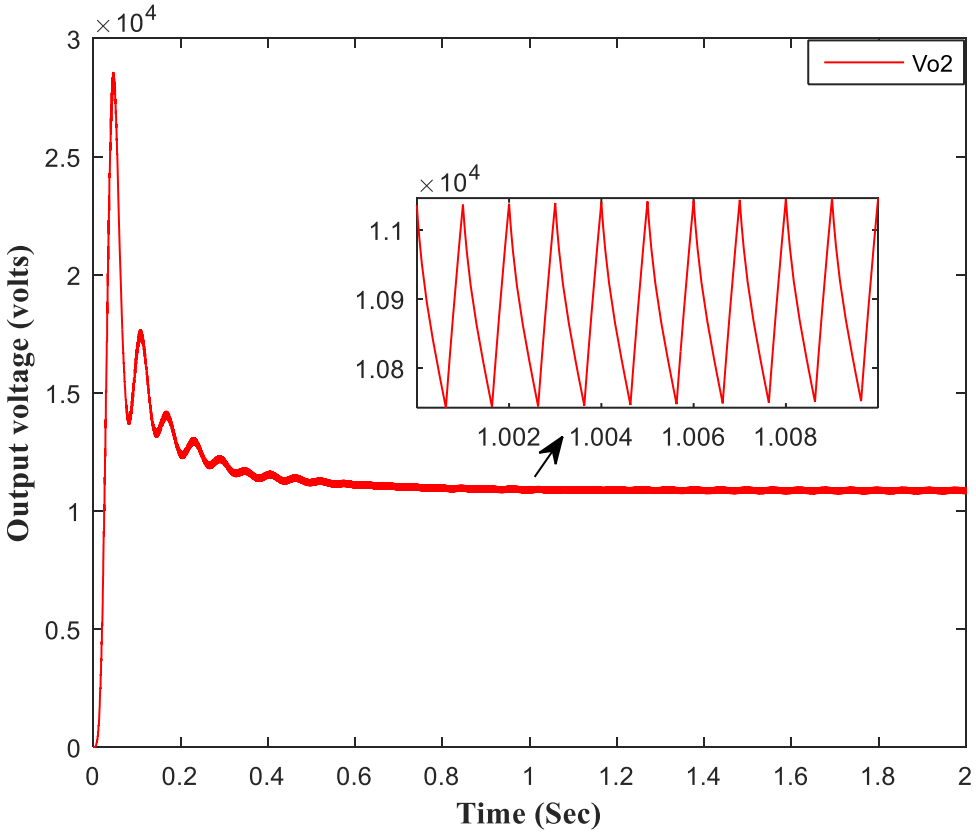


Figure 4.9 The output voltage response curve V_{o2} of the proposed three-input double-output DC transformer

From the simulated results it is clear that the predefined output voltage values are obtained where $V_{o1} = 8\ kV$ and $V_{o2} = 11\ kV$. With low peak-to-peak ripple voltage for the DC bus voltage V_o to be $12\ V$ and for V_{o1}, V_{o2} will be $250\ V, 400\ V$ respectively. In addition, the peak-to-peak ripple current of I_o will be $20\ A$ as shown in figure 4.10.

For cases where components are considered ideal, the efficiency could reach to 98 % as shown below.

$$Efficiency = \frac{Total\ output\ power\ (P_{oTotal})}{Total\ input\ power\ (P_{iTotal})} * 100\% \qquad (4.60)$$

The total input and output power could be calculated using equation (4.48), and after substitution the relevant data in equation (4.60) the efficiency will be:

$$Efficiency = \frac{187.9\ kW}{185\ kW} * 100\%$$

$$Efficiency = 98.4\ \%$$

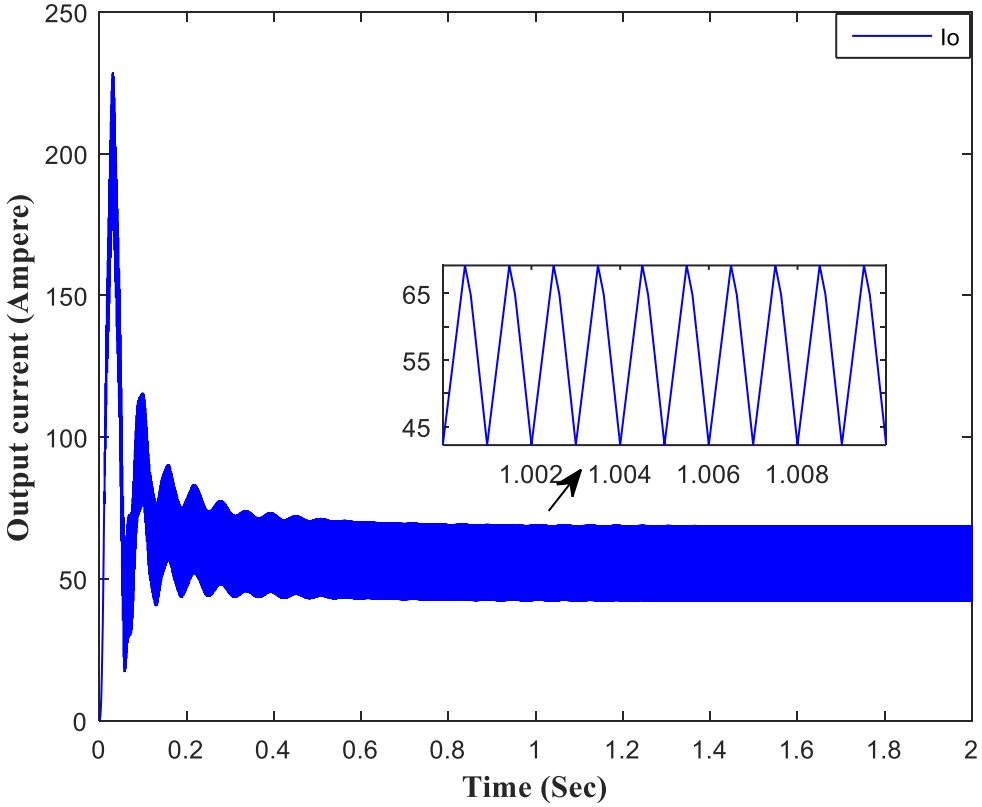


Figure 4.10 The output current response curve I_o of the proposed three-input double-output DC transformer

4.3.2. Power Losses and Efficiency of the Proposed MIMO DC Transformer

It is known that non-ideal components cause losses in the system. In order to find the total loss in a non-ideal DC transformer, the current flow through each component during the conduction period has to be calculated and then multiplied with the ON state voltage of that component such as the switches or the diodes.

Figure 4.11 shows the switching module power losses hierarchy.

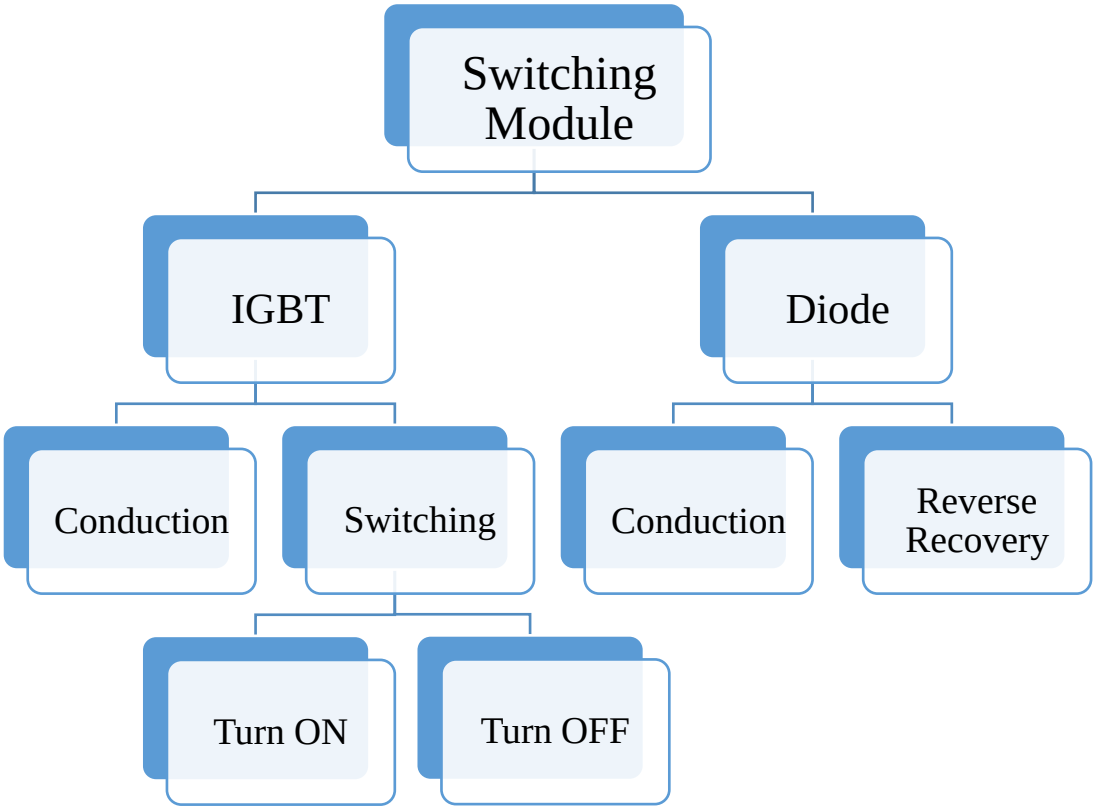


Figure 4.11 the IGBT module power losses hierarchy [130]

Assuming the switches are of IGBT types, then the total power loss of the IGBT is the sum of the conduction loss, turn ON and turn OFF losses.

$$P_{loss_{IGBT}} = P_{conduction} + P_{ON} + P_{OFF} \tag{4.61}$$

And

$$P_{switching} = P_{ON} + P_{OFF} \tag{4.62}$$

The switching loss occurs when the IGBT turns ON and OFF, thus it depends on the switching frequency. When the IGBT turns ON the collector current (I_C) increases rapidly and the collector-emitter voltage (V_{CE}) decreases. During this switching it takes time for the current to increases from zero to its rated value and for the voltage to drop to its saturation level, this transition of voltage and current produces losses called turn ON power loss (P_{ON}). The reverse behaviour of the switch's current and voltage occurs when the switch turns OFF (P_{OFF}).

And the switching loss of the switch will be

$$P_{S_{switching}} = P_{ON} + P_{OFF} \tag{4.63}$$

$$P_{S_{switching}} = 0.5 f_s V_{CE} I_C\ (t_{ON}) + 0.5 f_s V_{CE} I_C (t_{OFF}) \quad (4.64)$$

Where

$$t_{ON} = \frac{D}{f_s} \text{ and } t_{OFF} = \frac{(1-D)}{f_s} \quad (4.65)$$

Or it could be calculated from its data sheet using the energy loss concept(E_{ON} and E_{OFF}) as expressed below:

$$P_{S_{switching}} = (\ E_{ON} + E_{OFF}) * f_s \quad (4.66)$$

The conduction power loss ($P_{conduction}$)occurs when the switch or diode is ON and conducting current in the steady state mode. Its amount depends on the duration of steady state. When the switch is ON, then the power dissipated during the conduction mode $\left(P_{S_{conduction}}\right)$is found by multiplying the ON state voltage and the ON state current as follows

$$P_{S_{conduction}} = \frac{1}{T}\int_0^T [V_{CE}(t)\, I_C(t)]\, dt \quad (4.67)$$

$$P_{S_{conduction}} = I_{Switch_{ON}} * V_{CE_{ON}} \quad (4.68)$$

Or

$$P_{S_{conduction}} = {I_{Switch_{ON}}}^2 * R_{CE_{ON}} \quad (4.69)$$

The value of the ON state resistance for the IGBT switch or the diode normally can be found from their respective datasheets. Here for the IGBT, theoretically is expressed as:

$$R_{CE_{ON}} = \frac{\Delta V_{CE}}{\Delta I_C} \quad (4.70)$$

The diode conduction loss on the input side of the proposed design could be expressed as:

$$P_{Diode-i-_{conduction}} = I_i(1 - D_i) * V_{Forward_{Diode}} \quad (4.71)$$

Similarly, the diode conduction loss on the output side could be expressed as:

$$P_{Diode-o-_{conduction}} = I_o(1 - D_o) * V_{Forward_{Diode}} \quad (4.72)$$

And the diode reverse recovery loss occurs during the transition from ON to OFF states is expressed below:

$$P_{Diode_{reverse\ recovery}} = (E_{Rec}) * f_s \quad (4.73)$$

Where E_{Rec} is the diode's recovery energy which is provided by the manufacturer in its datasheet which here has been ignored in the total losses calculations.

In the proposed MIMO step-up DC transformer, the total losses will be found for $(m + n)$ components including the power switches, diodes, inductors and capacitors. Figure 4.12 shows the effect of the number of outputs on the total losses and total output power in the proposed transformer. In this study, the total losses in the system found using the simulation of three-input with different number of outputs based on the following specifications: $R_{source} = 0.1\ \Omega, R_{ind} = 0.2\ \Omega$ and $R_{capacitor} = 0.2\ \Omega$ and the ON, OFF resistances of the diodes and switches $R_{ON} = 0.01\ \Omega, R_{OFF} = 1.0 * 10^6\ \Omega$. And the forward voltage drops of the diode $V_{Forwared} = 0.7\ V$ and of the IGBT switch $V_{switch-ON} = 3\ V$.

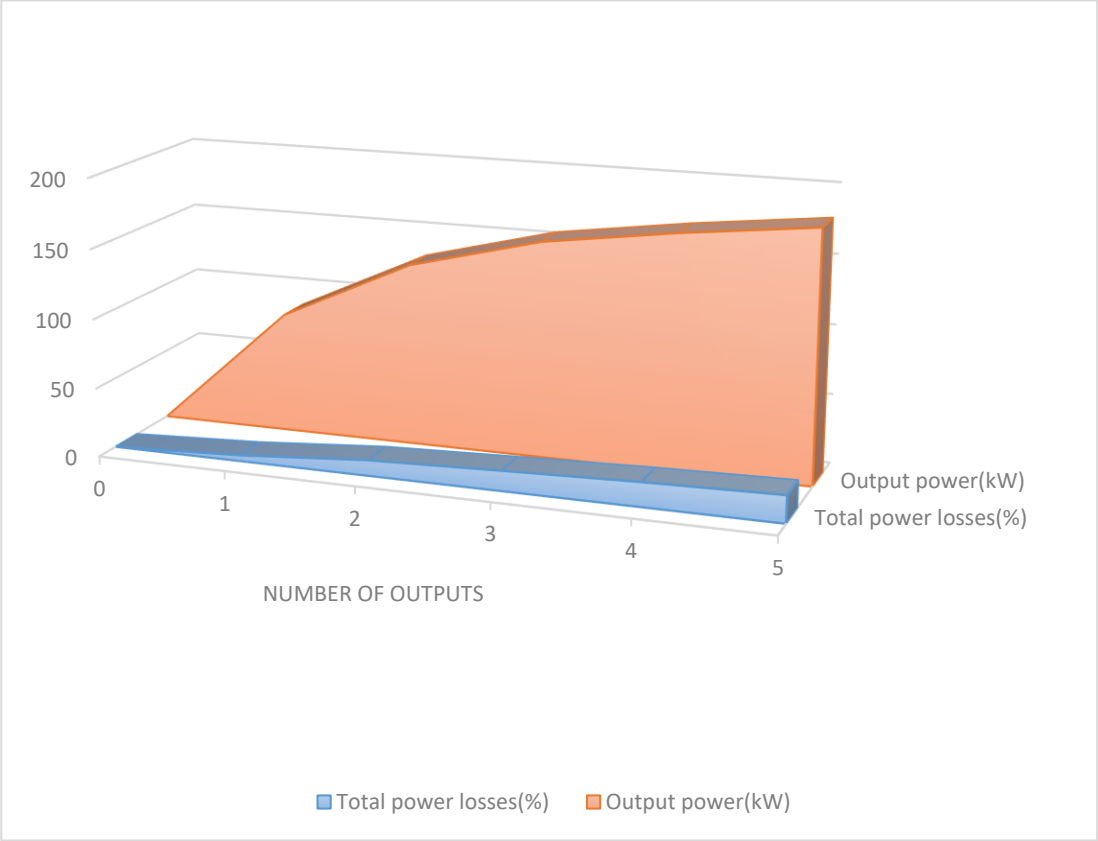


Figure 4.12 the effect of the number of outputs on the total output power and total power losses of the proposed DC transformer

Figure 4.12 suggests that as the number of outputs increase the total loss of the system will increase. This is due to having more module outputs will increase the number of used components such as power switch, diodes and the passive components. As will be discussed later in section 6.2 in general the total power loss of the proposed system is low compared

with different available topologies. Thus, the efficiency of the proposed MIMO DC transformer is high.

To determine the efficiency of the proposed DC transformer the following formula could be used

$$Efficiency = \frac{Total\ output\ power\ (P_{oTotal})}{Total\ input\ power\ (P_{iTotal})} * 100\% \tag{4.74}$$

For SISO DC transformer

- Ideal system

$$Efficiency = \frac{[\frac{V_{i1}}{(1-D_{i1})} * \frac{1}{(1-D_{o1})}]^2 / R_L}{V_{i1} * I_{i1}} * 100\% \tag{4.75}$$

- Non-Ideal system

$$Efficiency = \frac{(V_{o1_{(non-ideal)}})^2}{V_{i1} * I_{i1} * R_L} * 100\% \tag{4.76}$$

As the magnitude of the output voltage drops when the losses are included, this will lead to decreases in the transformer's efficiency. For example, if the efficiency of the proposed double-input single-output ideal transformer 100% then this efficiency will be reduced to 95.8% for non-ideal transformer. A drop of 4.2%. Figure 4.13 depicts the efficiency of the double-input multi-output ideal and non-ideal DC transformer.

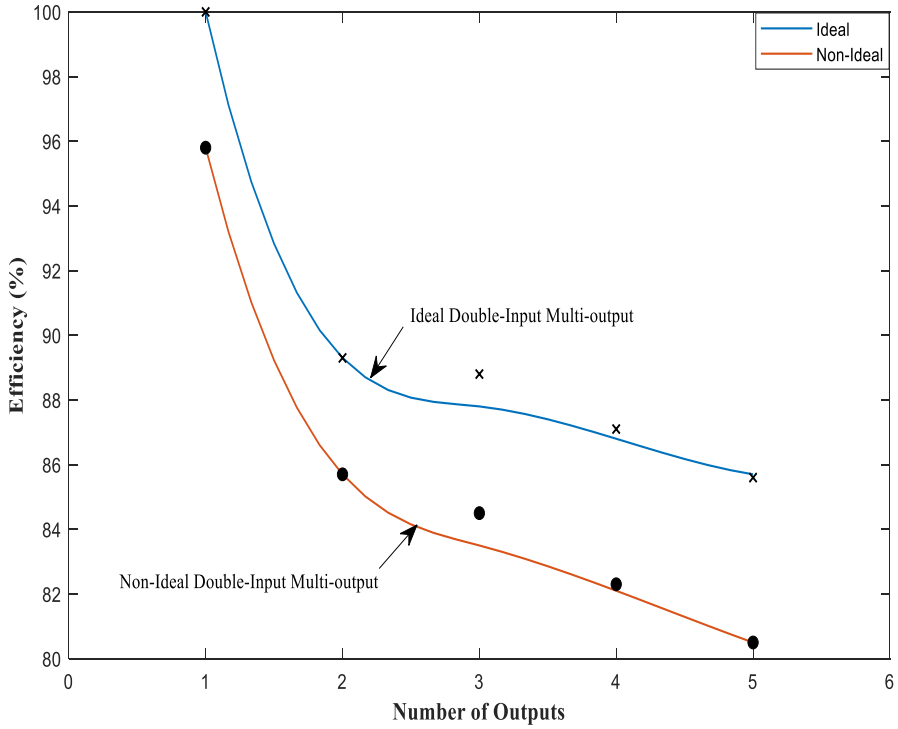


Figure 4.13 ideal and non-ideal double input DC transformer efficiency with different number of outputs where $V_{i1} = V_{i2} = 330\ V$.

4.3.3. The Optimal Operating Frequency of the Proposed MIMO DC Transformer

In this study IGBTs are used as the power switches. The operating frequency range for IGBTs are up to 100 kHz [131]. In designing DC transformer, it is important to find the best operating frequency of the utilised semiconductor power switches. In general operation of switches at higher frequencies leads to increase in losses, increase in cost of components and decrease in overall efficiency. Whilst operation of switches at lower frequencies increase the size of the components and efficiency. This suggests that determination of the optimal switching frequency is an essential requirement for optimum performance of a system.

Figure 4.14 depicts the effect of the switching frequency on the output voltage of SISO proposed DC transformer design. Analysis of figure 4.14 reveals that at lower frequencies the IGBTs deliver more current than at higher frequencies. However, the drawback of operating a system at frequencies $fs < 1\ kHz$ lies in increase of the output ripple voltage which is not of interest. In the proposed design, the optimum values of L and C parameters are calculated at 1 kHz as the performed simulations shown that the IGBTs perform better at 1 kHz frequency.

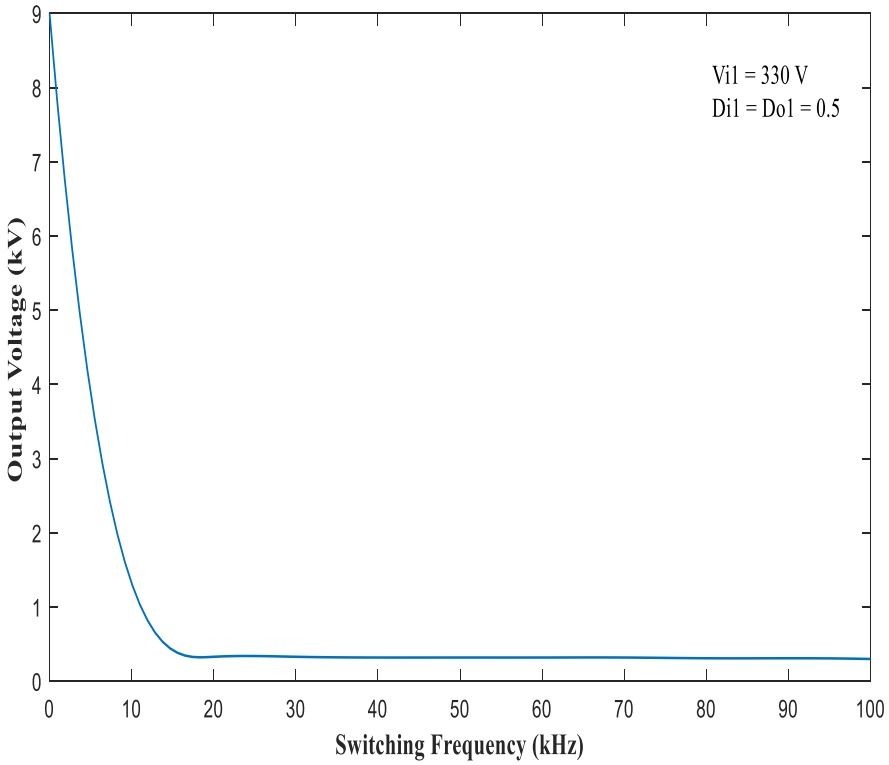


Figure 4.14 the output voltage of SISO DC transformer vs. the operating switching frequency

To demonstrate the above mentioned points, a two-input two-output of the proposed DC transformer design type as shown in figure 4.15 has taken as an example. The performance of this design under two different switching frequencies: namely $1\ kHz$ and $10\ kHz$ is investigated. At each frequency, under the following design requirements, parameters of the DC transformers are sized.

$$V_{i1} = V_{i2} = 330\ V$$

$$V_o = 2\ kV$$

$$V_{o1} = 8\ kV\ , V_{o2} = 11\ kV$$

$$D_{i1} = D_{i2} = 67\ \%$$

$$D_{o1} = 75\ \%\ ,\ D_{o2} = 81\ \%$$

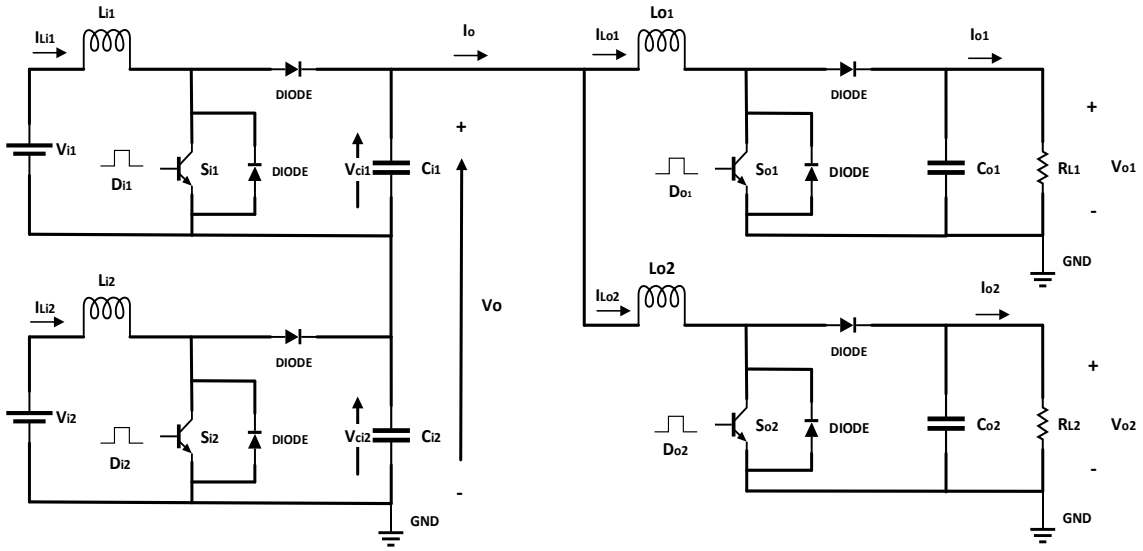


Figure 4.15 The proposed double-input double-output DC transformer diagram

For $f_s = 1\ kHz$,

$$L_{i1} = L_{i2} = 1.9 * 10^{-3}\ H$$

$$L_{o1} = L_{o2} = 91 * 10^{-3}\ H$$

$$C_{i1} = C_{i2} = 2.5 * 10^{-3}\ F$$

$$C_{o1} = C_{o2} = 25.1 * 10^{-6}\ F$$

$$R_{L1} = R_{L2} = 1\ \ k\Omega$$

For $f_s = 10\ kHz$,

$$L_{i1} = L_{i2} = 192.2 * 10^{-6}\ H$$

$$L_{o1} = L_{o2} = 9.1 * 10^{-3}\ H$$

$$C_{i1} = C_{i2} = 250 * 10^{-6}\ F$$

$$C_{o1} = C_{o2} = 2.5 * 10^{-6}\ F$$

$$R_{L1} = R_{L2} = 1\ \ k\Omega$$

The above data shows that at higher swicthing frequencies the value of the inductors, capacitors are less compared with those obtained at lower frequencies. The physical size of components have direct relation to their computed values as well as their wight and dimension. Also lower value of inductor, means less energy is stored or released in or from the inductor during ON or OFF switching. Furthermore, according to the following relation the ripple inductor current will be lower too.

$$L \geq \frac{V_i(V_o - V_i)}{V_o f_s \Delta I_L} \tag{4.77}$$

These are demonstrated for example by considering a fixed inductance value (computed above) and obtaining the peak-to-peak ripple inductor current at $f_s = 1\ kHz$ and $f_s = 10\ kHz$.

At $f_s = 1\ kHz$

$$\Delta I_{Lo1} = 17\ A \text{ and it will be reduced by } 89\%$$

$$\Delta I_{Lo2} = 16\ A$$

And at $f_s = 10\ kHz$

$$\Delta I_{Lo1} = 1.8\ A$$

$$\Delta I_{Lo2} = 1.6\ A$$

Also demonstrated is the effect of low and high switching frequencies on efficiency of the above example as shown below in step by step approach.

The efficiency of the above system at $f_s = 1\ kHz$ will be

$$P_{(in)_{Total}} = (I_{i1} * V_{i1}) + (I_{i2} * V_{i2}) \tag{4.78}$$

$$P_{(in)_{Total}} = (335 * 330) * 2$$

$$P_{(in)_{Total}} = 221.1\ kW$$

And the total output power for two outputs

$$P_{(o)_{Total}} = \frac{{V_{o1}}^2}{R_{L1}} + \frac{{V_{o2}}^2}{R_{L2}} \tag{4.79}$$

$$P_{(o)_{Total}} = 185\ kW$$

$$Efficiency = \frac{P_{(o)_{Total}}}{P_{(in)_{Total}}} * 100\% \tag{4.80}$$

$$Efficiency = 83.67\%$$

While, at $f_s = 10\ kHz$ using the above approach the efficiency will be:

$$P_{(in)_{Total}} = (380 * 330) * 2$$

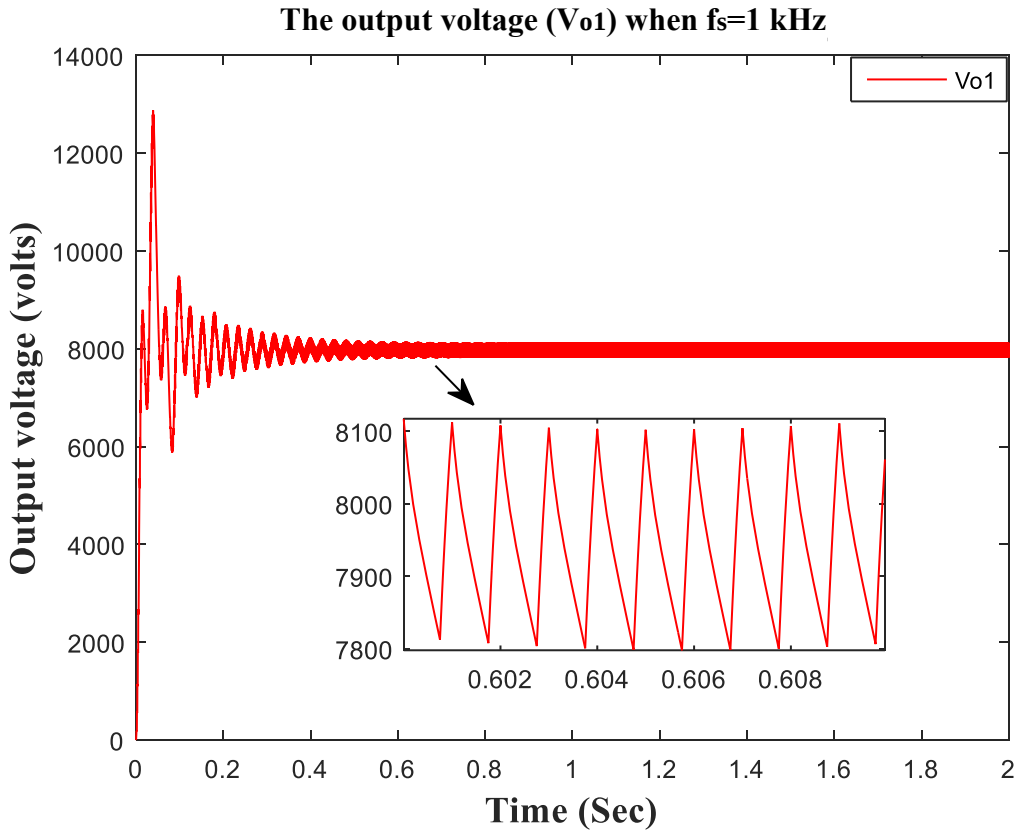
$$P_{(in)_{Total}} = 250.8\ kW$$

$$P_{(o)_{Total}} = 185\ kW$$

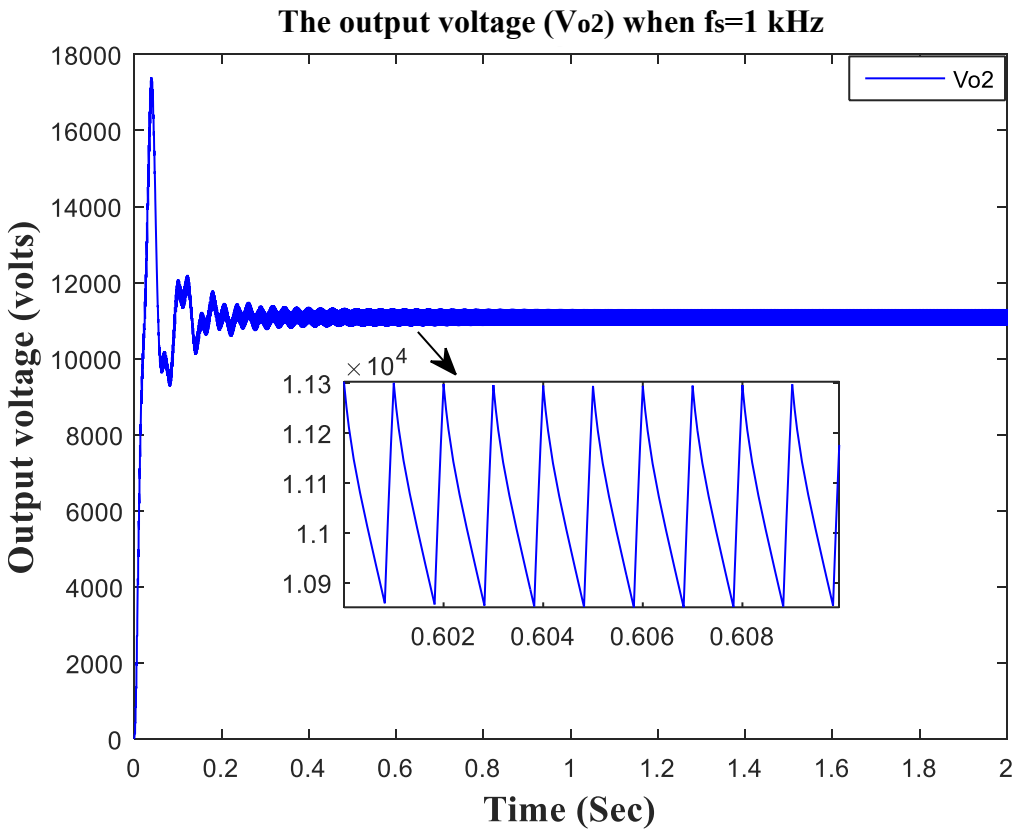
$$Efficiency = 73.76\%$$

It is clear that at lower frequencies the DC transformer will be more efficient than at higher frequencies.

Figures 4.16 and 4.17 depict the MATLAB/SIMULINK simulation results of the proposed double-input double-output DC transformer for two cases of switching frequencies namely 1 kHz and 10 kHz.

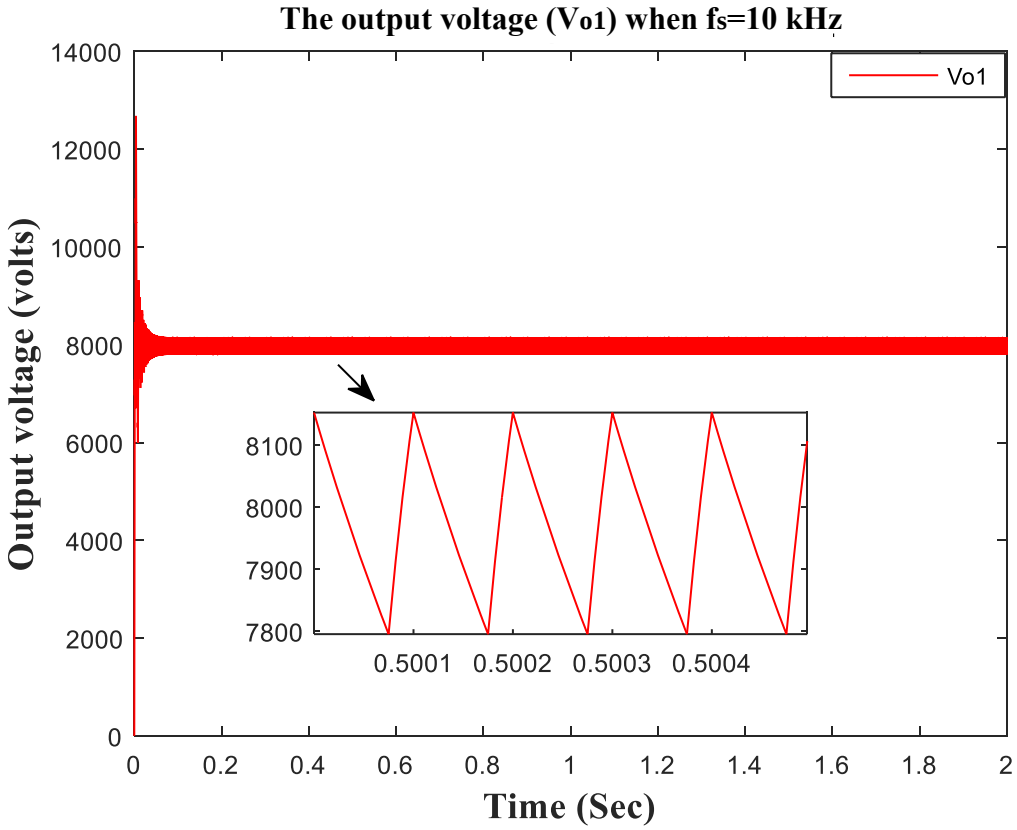


(a) the output voltage response curve V_{o1} of the proposed double-input double-output DC transformer at $f_s = 1\ kHz$

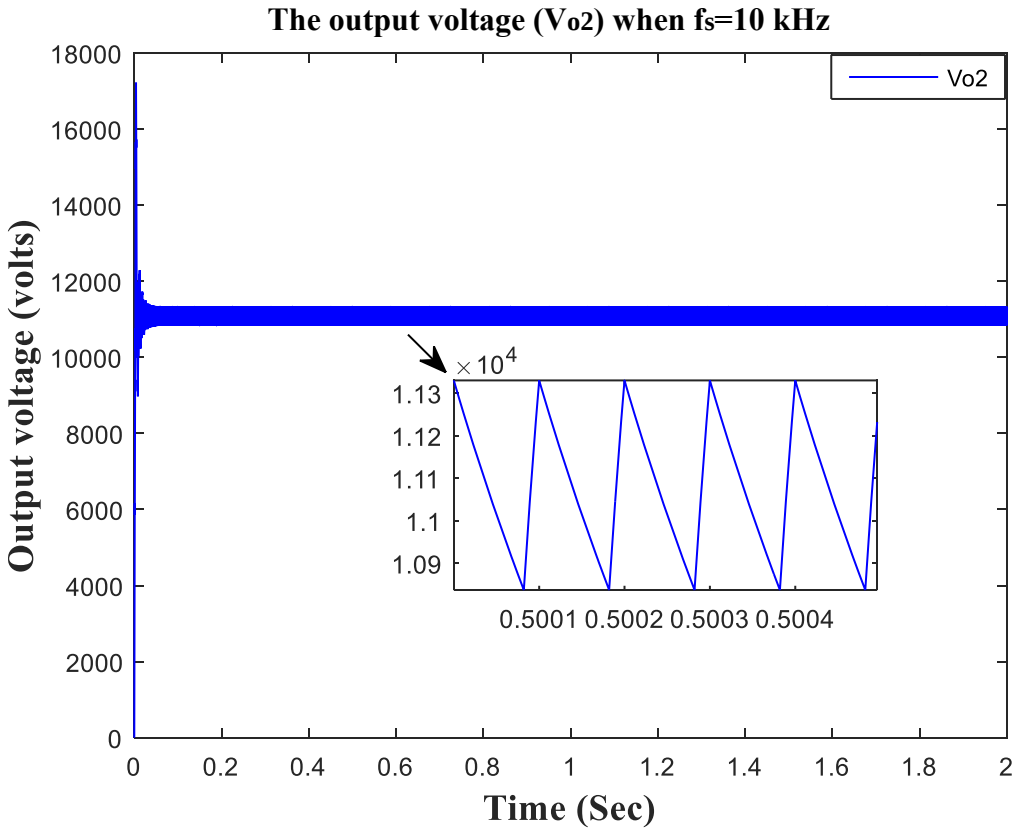


(b) the output voltage response curve V_{o2} of the proposed double-input double-output DC transformer at $f_s = 1\ kHz$

Figure 4.16 the output voltage response curves V_{o1}, V_{o2} of the proposed double-input double-output DC transformer at $f_s = 1\ kHz$



(a) The output voltage response curve V_{o1} of the proposed double-input double-output DC transformer at $f_s = 10\ kHz$



(b) The output voltage response curve V_{o2} of the proposed double-input double-output DC transformer at $f_s = 10\ kHz$

Figure 4.17 The output voltage response curves V_{o1}, V_{o2} of the proposed double-input double-output DC transformer at $f_s = 10\ kHz$

The peak-to-peak output voltage ripple ΔV_{o1} decreases as the switching frequency increases. This is shown below through the derived expressions.

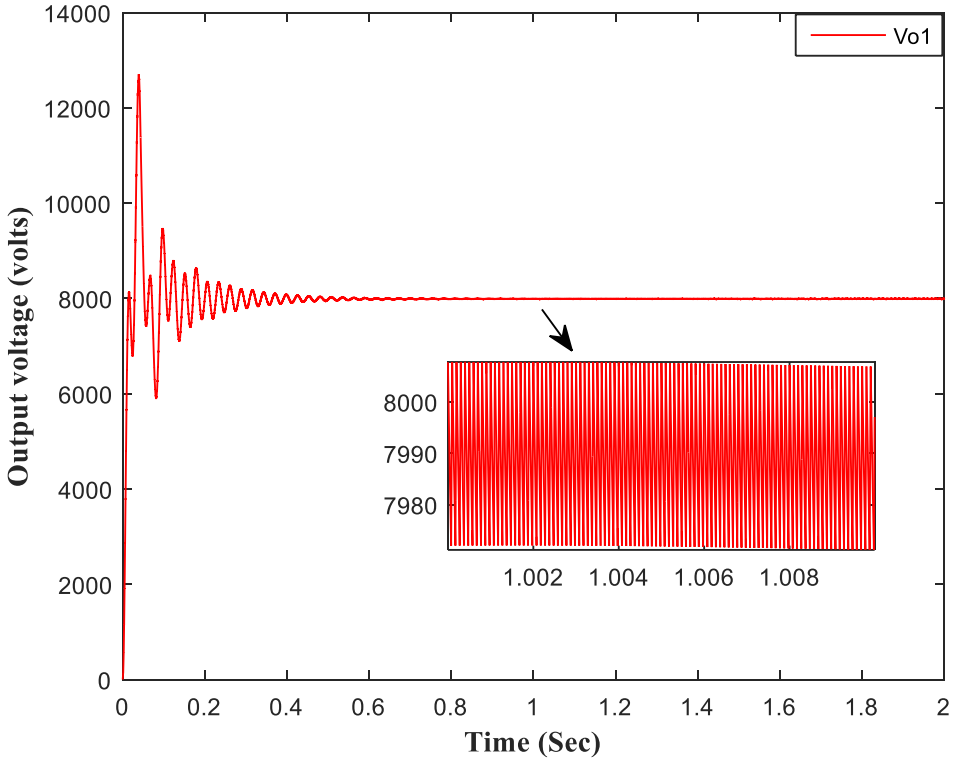
$$\Delta V_{o1} = \frac{V_{o1} D_{o1}}{R_L C_{o1} f_s} \tag{4.81}$$

$$\frac{\Delta V_{o1}}{\Delta V_{o1}{}^*} = \frac{f_s{}^*}{f_s} \tag{4.82}$$

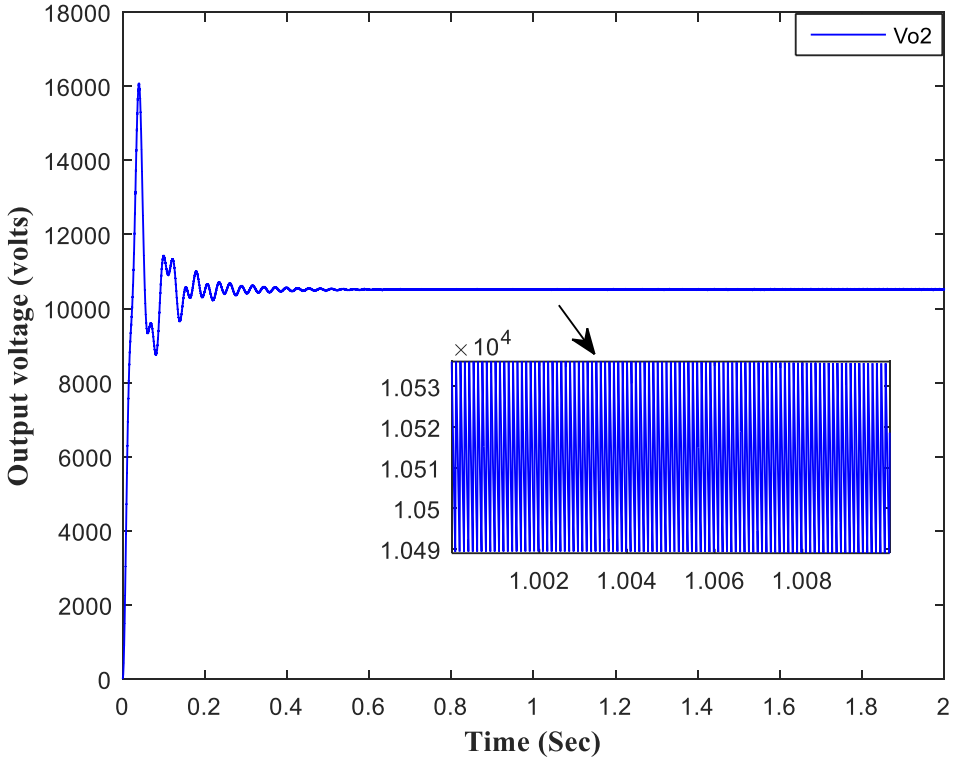
$$\Delta V_{o1}{}^* = \frac{\Delta V_{o1} f_s}{f_s{}^*} \tag{4.83}$$

Where $f_s{}^*$ is the new switching frequency.

The above statement is also demonstrated through simulation by assuming a scenario where L and C values are fixed and the peak-to-peak output ripple voltage (ΔV_{on}) is measured by zooming on the curves of figures 4.18 which show the output voltage at $10\ kHz$.



(a) The output voltage response curve V_{o1} of the proposed double-input double-output DC transformer at $f_s = 1\ kHz$ parameters selection and $f_s{}^* = 10\ kHz$



(b) The output voltage response curveV_{o2} of the proposed double-input double-output DC transformer at $f_s = 1\ kHz$ parameters selection and $f_s{}^* = 10\ kHz$

Figure 4.18 The output voltage response curves $V_{o1}V_{o2}$ of the proposed double input double output DC transformer at $f_s = 1\ kHz$ parameters selection and $f_s{}^* = 10\ kHz$

Under the same scenario as above where L and C values are fixed, the switching duty ratios as shown in figure 4.19 to have influence on the output voltage. However, this influence is abrupt for duty ratios rating 0.75 to 0.9. This is true for all considered switching frequencies ($1\ kHz$ to $10\ kHz$).

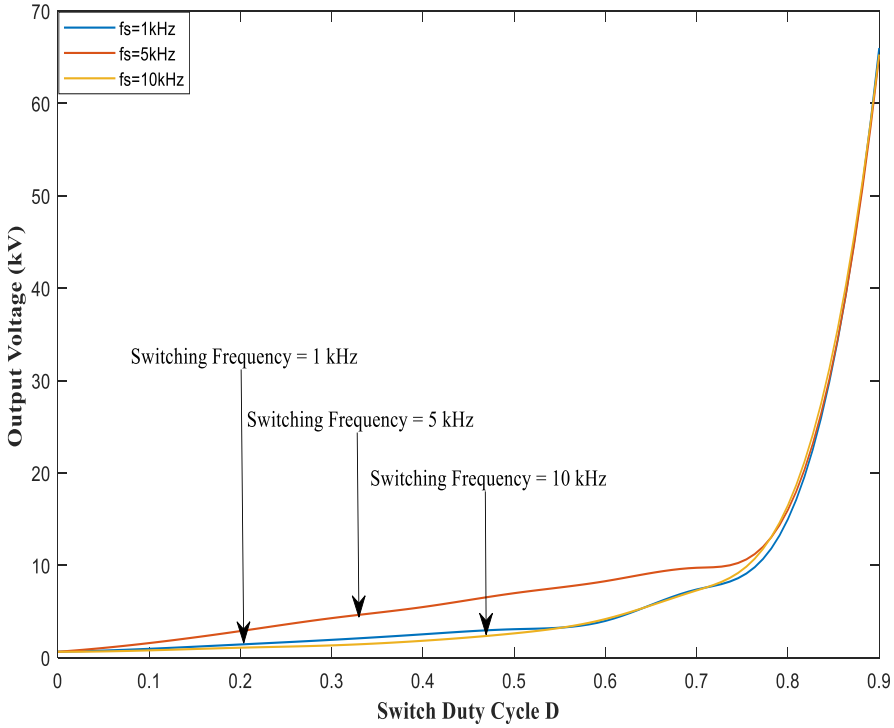


Figure 4.19 The relation between the output voltage and the duty cycle of the power switch operating under different switching frequencies

In general, one can suggest for cases where L and C are kept fixed, increase in the switching frequency f_s reduces the magnitude of the ripple inductor current and the magnitude of the ripple capacitor voltage. However, the change in the output voltage is not as such pronounced. This is not true for cases where L and C are computed at each swicthing frequency.

The studies so far suggest that in a design there should be a trade-off between the switching frequency, losses and the size of components. As in the proposed DC transformer design $m+n$ number of active power switches is used, in order to have less switching losses, a $1\ kHz$ has been chosen to operate the power switches of the proposed MIMO step-up DC transformer.

4.4.The DC Characteristics of the Proposed MIMO DC Transformer

In this section the DC characteristics of the proposed transformer are clarified theoretically, and the results are confirmed via simulations. The DC characteristics of the proposed DC

transformer at steady state condition include the step-up conversion gain, the voltage-current relation, the efficiency and the effect of the parasitic resistances on the output voltage of the designed transformer.

As mentioned in section 4.2.1.1 the ideal step-up conversion gain of the proposed MIMO DC transformer is

$$M(D) = \left[\sum_{k=1}^{k=m} \frac{1}{1 - \mathrm{D_{ik}}}\right]\left[\frac{1}{1 - D_{on}}\right] \tag{4.84}$$

To explore how the number of inputs will affect on the conversion gain of the proposed design, it is assumed that m number of identical inputs is connected together with such output. Then the conversion gain is expressed as:

$$\frac{V_{on}}{V_{im}} = \frac{m}{(1 - Di)(1 - Don)} \tag{4.85}$$

if

$$(D_{i1} = D_{i2} = \cdots D_{im} = D_i) \tag{4.86}$$

From the equations mentioned earlier the relation between the output voltage and the switch duty cycle D of the proposed DC transformer is a nonlinear. This is shown graphically in figure 4.20 for a SISO designed transformer. The graph of figure 4.20 shows that the output DC voltage V_{o1} is affected by the duty cycle D of the operating switches. For example, for the duty cycle less than 50%, there is a slight change on the output voltage, whereas a significant increase in V_{o1} can be observed for $D > 50\%$. Hence, the output voltage V_{o1} of the proposed DC transformer operating in an ideal mode depends on two parameters namely the duty cycle of the operating switches and the DC input voltage value. Consequently, the proposed DC transformer could have an optimum duty cycle value in order to obtain the desired voltage level.

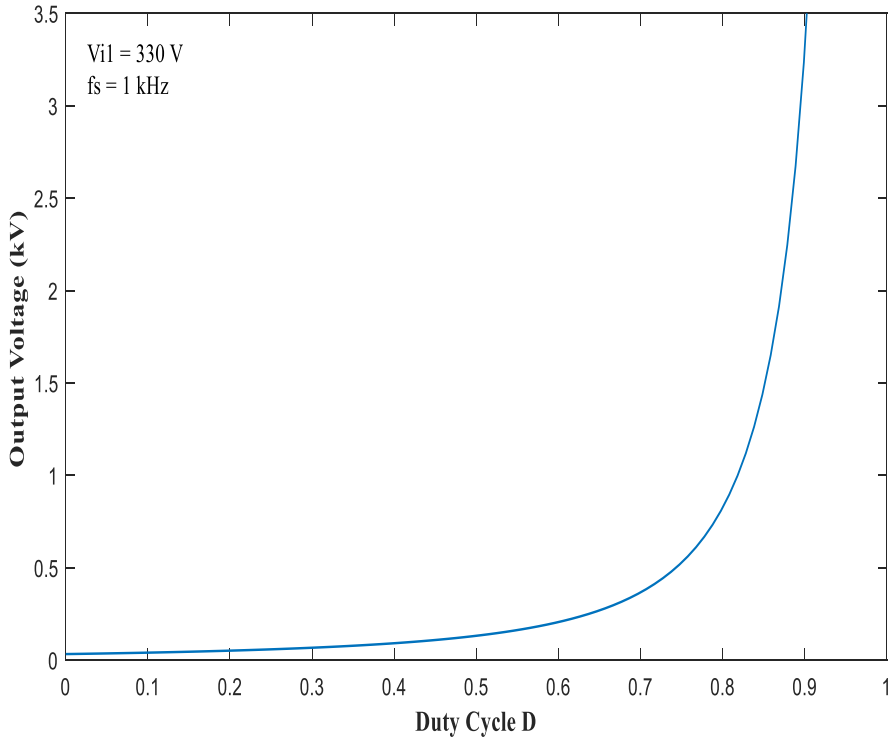


Figure 4.20 the relation between the output DC voltages V_{o1} and the switch duty cycle D of the proposed SISO DC transformer

Studies also revealed that the step-up conversion ratio is directly affected by the number of inputs (m) of the proposed DC transformer. Figure 4.21 demonstrates the findings graphically.

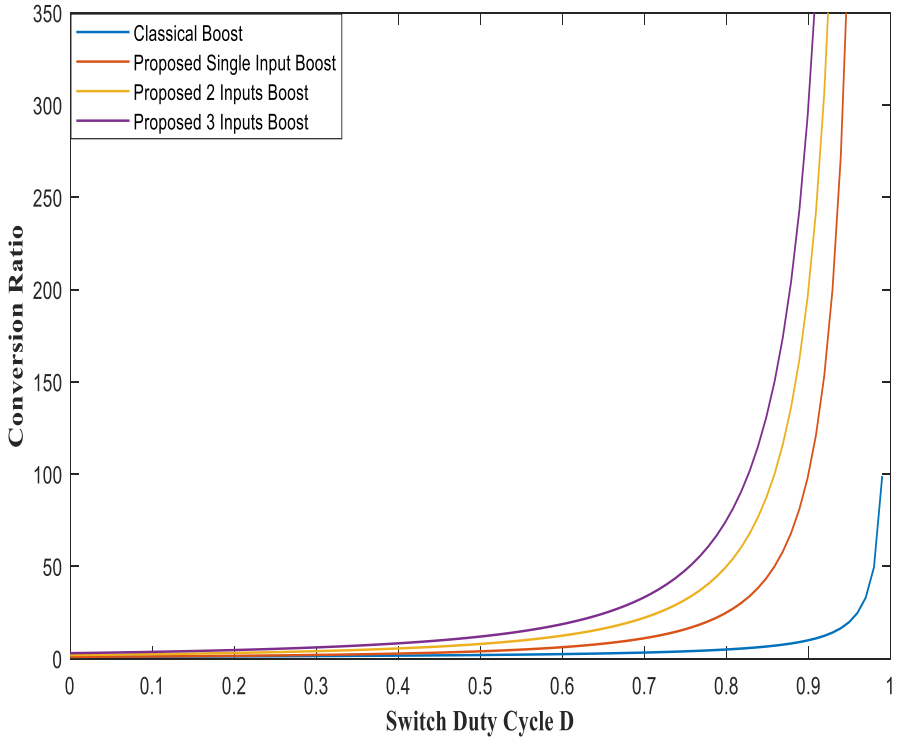


Figure 4.21 Comparison between the conversion ratio of the proposed MIMO step-up DC transformer and the classical (conventional) DC transformer when $(D_{i1} = D_{i2} = \cdots D_{im} = D_{on})$

The numbers of input sources (or larger input voltages) have direct influence on the output voltage and current of the proposed DC transformer. Figure 4.22 shows the plot of output current-voltage (I-V) curves obtained from the solution of equations (4.85) and (4.88) for a SISO configuration at various input voltage values by considering $D_{i1} = D_{o1}$.

The input current is:

$$I_{i1} = \frac{V_{i1}}{(1 - D_{i1})^4 * R_{Load}} \tag{4.87}$$

And the output current is expressed as:

$$I_{o1} = (1 - D_{i1})^2 * I_{i1} \tag{4.88}$$

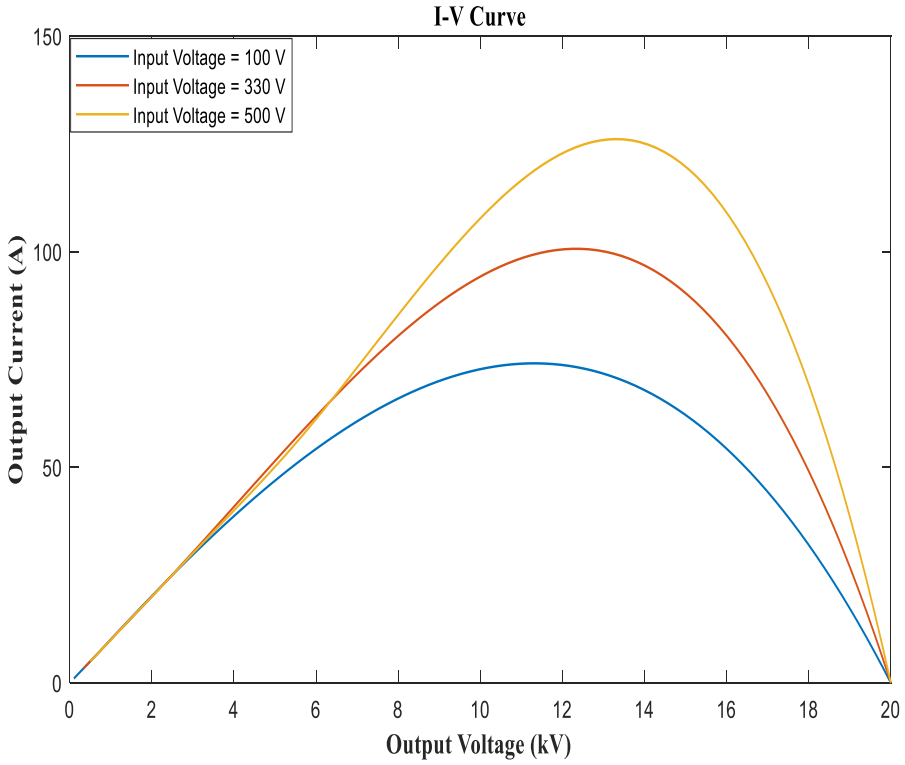


Figure 4.22 the current-voltage (I-V) curve of the SISO configuration of the proposed DC transformer at various input voltage values

Other parameters that affect the output voltage are the parasitic resistances i.e. the series resistance of inductors, capacitors, diodes and on state switches [132]. Figure 4.23 depicts the output voltage profile of a SISO DC transformer for conditions when $R_{Switch_{i1}} = R_{Switch_{o1}}$ and $R_{Diode_{i1}} = R_{Diode_{o1}}$. Analysis of the graphs suggests that, the series resistance of the inductor R_{ind} and the ON state switch resistance have significant influence on the output voltage when their value exceeds 50 $m\Omega$.

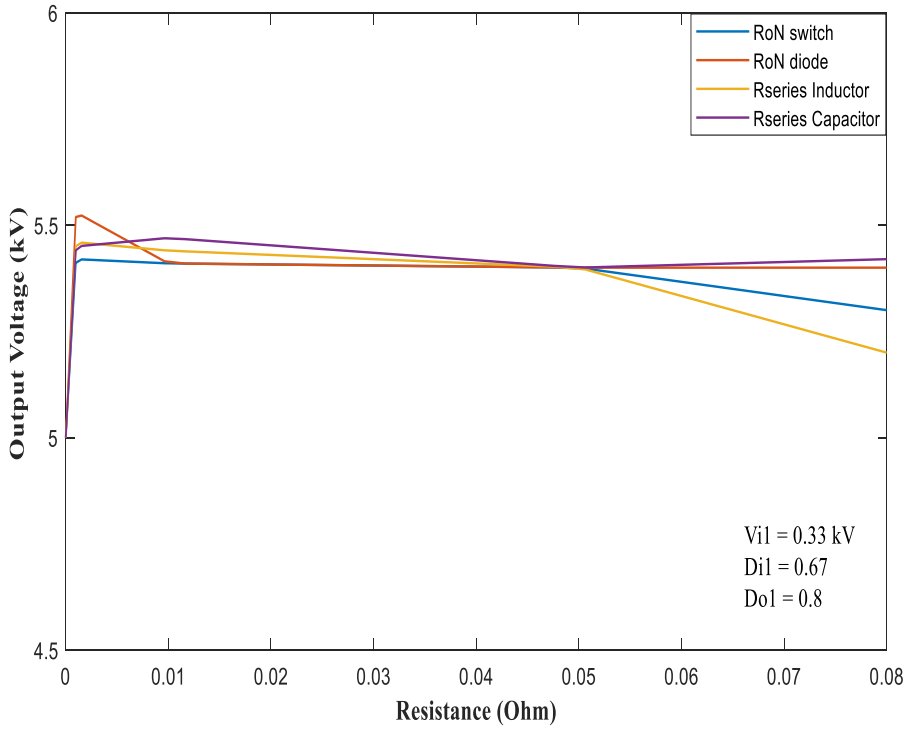


Figure 4.23 the effect of parasitic resistance variation on the output voltage V_{o1} of SISO DC transformer design

Figure 4.24 shows the normalised output voltage for SISO DC transformer against the duty ratio for a range of R_{ind}/R_{Load} which reveals that maximum conversion ratio could be obtained when R_{ind} is zero (ideal inductor) assuming that R_{Load} is fixed.

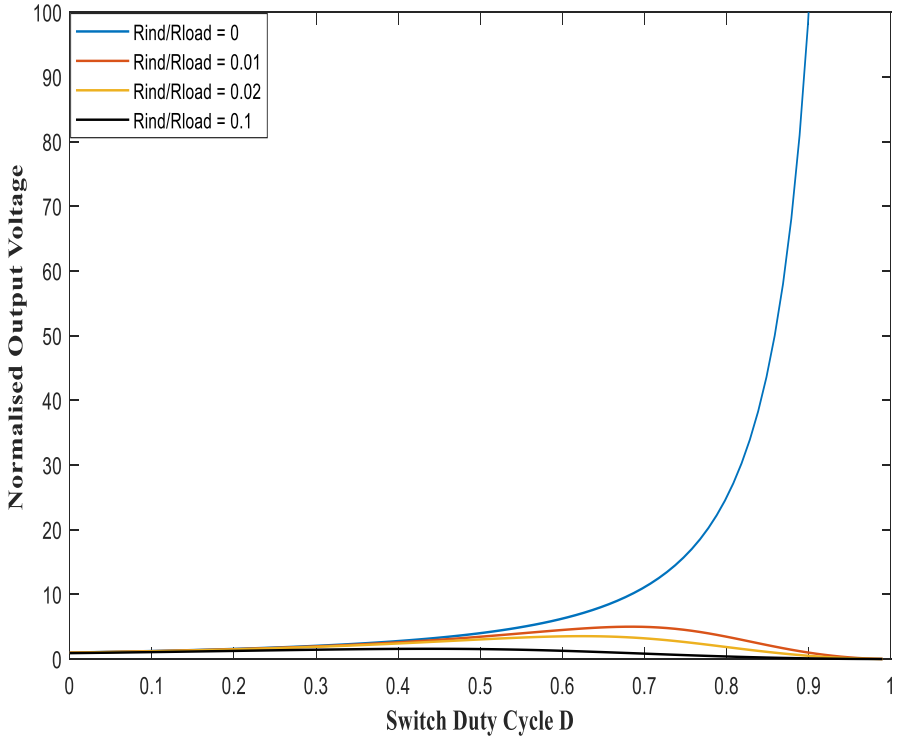


Figure 4.24 the normalised voltage of SISO proposed DC transformer with different switches' duty ratios for ideal and non-ideal inductor with $V_i = 330\ V$

In the proposed MIMO DC transformer, assume that

$$D_{i1} = D_{i2} = \cdots = D_{im} = D_{on} = D$$

For an ideal case where $R_{ind} = 0$, the normalised output voltage could be expressed as:

$$\frac{V_{on}}{V_{im}} = \frac{m}{(1-D)^2} \tag{4.89}$$

And for non-ideal case where $R_{ind} \neq 0$, the normalised output voltage could be expressed as:

$$\frac{V_{on_{(non-ideal)}}}{V_{im}} = \frac{m}{(1-D)^2\left[1 + \frac{R_{ind}}{(1-D)^4\, R_{Load}}\right]} \tag{4.90}$$

Figure 4.25 shows normalised voltage of the proposed transformer with the switches' duty cycle for different number of inputs in the case of ideal inductor. It is clear that the normalised voltage depends on the number of connected inputs as well as the duty ratio of the power switches' value.

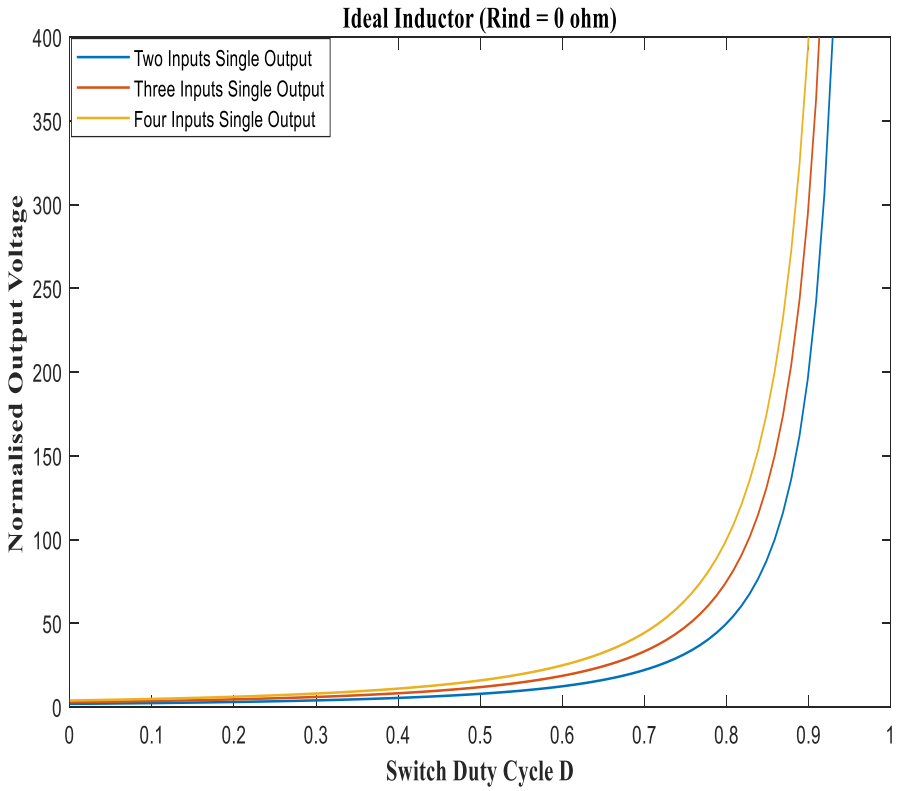


Figure 4.25 the normalised voltage of the proposed DC transformer with the switches' duty cycle for different number of inputs in the ideal case where $R_{ind} = 0$

Figures 4.26, 4.27 and 4.28 show the effect of inductors' resistance on the proposed DC transformer's normalised voltage for different number of inputs.

The results suggest that as the number of inputs increases the output voltage increases too. In addition, as expected the losses in the system will be increased as the inductors' resistance increases. Also, it is noticeable from the graphs that the proposed MIMO DC transformer delivers more power and performs better when the duty cycle value in the range of 60% – 80%.

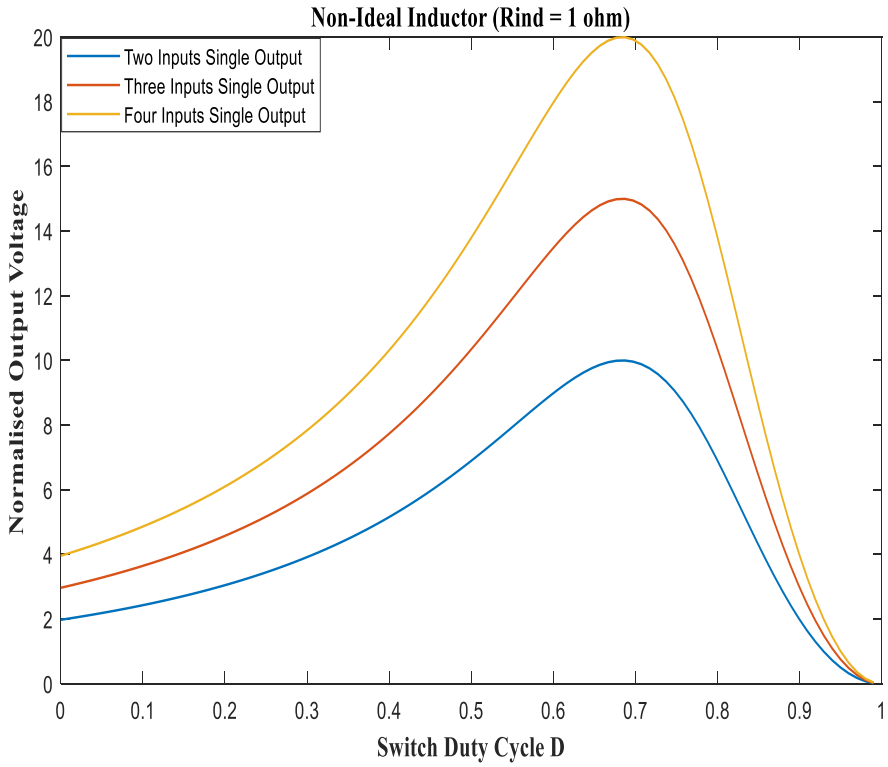


Figure 4.26 the normalised voltage of the proposed transformer with the switches' duty cycle for different number of inputs in the non-ideal case where $R_{ind}/\ R_{Load} = 0.01$, $V_i = 330\ V$

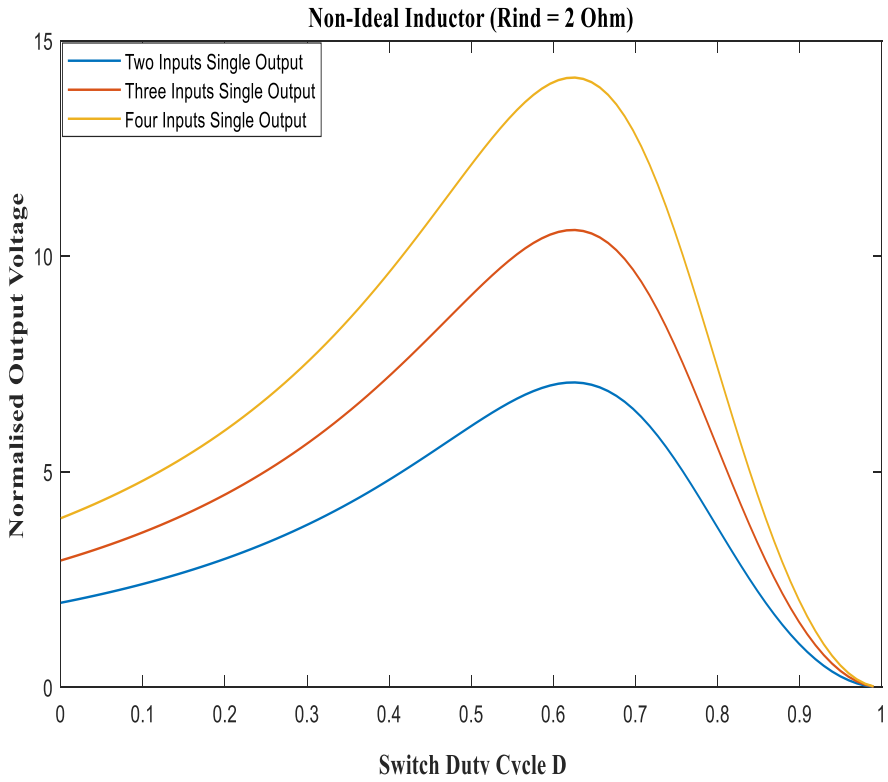


Figure 4.27 the normalised voltage of the proposed transformer with the switches' duty cycle for different number of inputs in the non-ideal case where $\frac{R_{ind}}{R_{Load}} = 0.02$, $V_i = 330V$

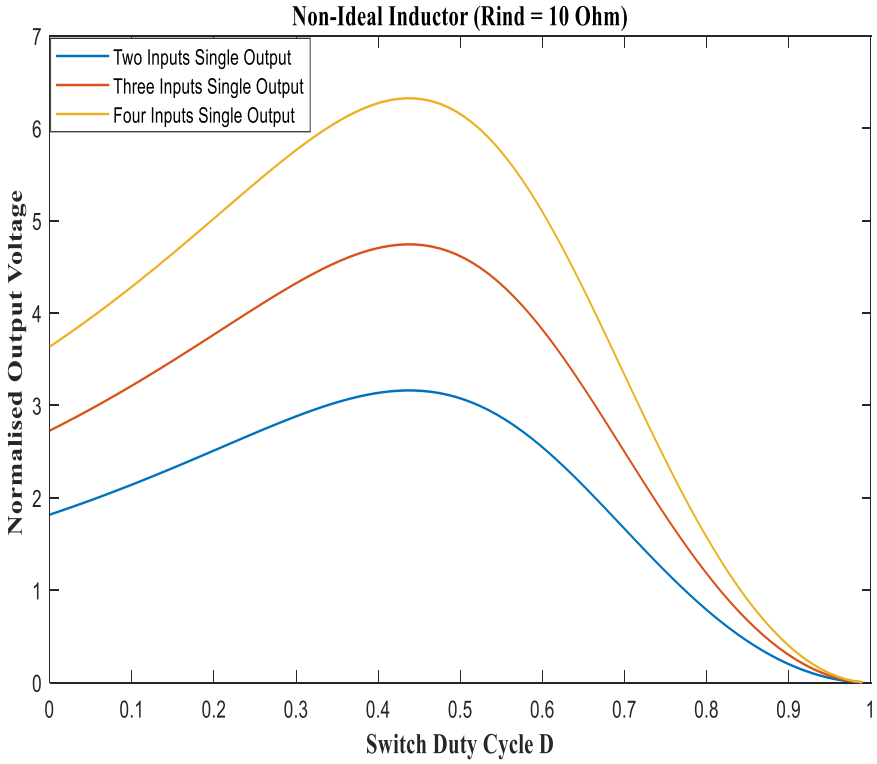


Figure 4.28 the normalised voltage of the proposed transformer with the switches' duty cycle for different number of inputs in the non-ideal case where $R_{ind}/\ R_{Load} = 0.1$, $V_i = 330\ V$

Since the output of the DC transformer is not a linear function of the duty cycle, then for any one output to input voltage ratio, there is an optimum duty cycle and any higher or lower value causes more losses. Furthermore, as the duty cycle increases the transformer's

efficiency decreases. This is related to when the duty cycle increases a higher inductor current is obtained which allows more to be transferred to the output. However, this power or current transfer happens during the OFF time. As the duty ratio increases, the OFF time $(1-D)$ decreases, which leads to a lesser time for the current to be transferred onto the load side. Thus, for cases where the load is kept constant, increasing the duty ratio D and $[R_{ind}/R_{Load}]$ value will result in lower system efficiency as shown in figure 4.29.

The output voltage of the proposed DC transformer in non-ideal mode considering the R_{ind} value, $(D_{i1} = D_{o1} = D)$ and neglecting the effect of the other parasitic resistances in the transformer could be calculated as:

$$V_{o1_{(non-ideal)}} = \frac{V_{i1}}{(1-D)^2} - \left[\frac{D}{(1-D)^2} * \frac{V_{i1}}{(1-D)^4 R_{Load}}\ R_{ind} + \frac{D}{(1-D)}\ R_{ind} * \frac{V_{i1}}{(1-D)^3 R_{Load}}\right] \quad (4.91)$$

$$\frac{V_{o1_{(non-ideal)}}}{V_{i1}} = \frac{1}{\left[(1-D)^2\left(1 + \frac{R_{ind}}{(1-D)^4 * R_{Load}}\right)\right]} \quad (4.92)$$

Then the efficiency could be expressed as:

$$Efficiency = \frac{V_{o1_{(non-ideal)}}}{V_{i1}} * (1-D)^2 * 100\% \quad (4.93)$$

$$Efficiency = \frac{1}{\left[1 + \frac{R_{ind}}{(1-D)^4 R_{Load}}\right]} * 100\% \quad (4.94)$$

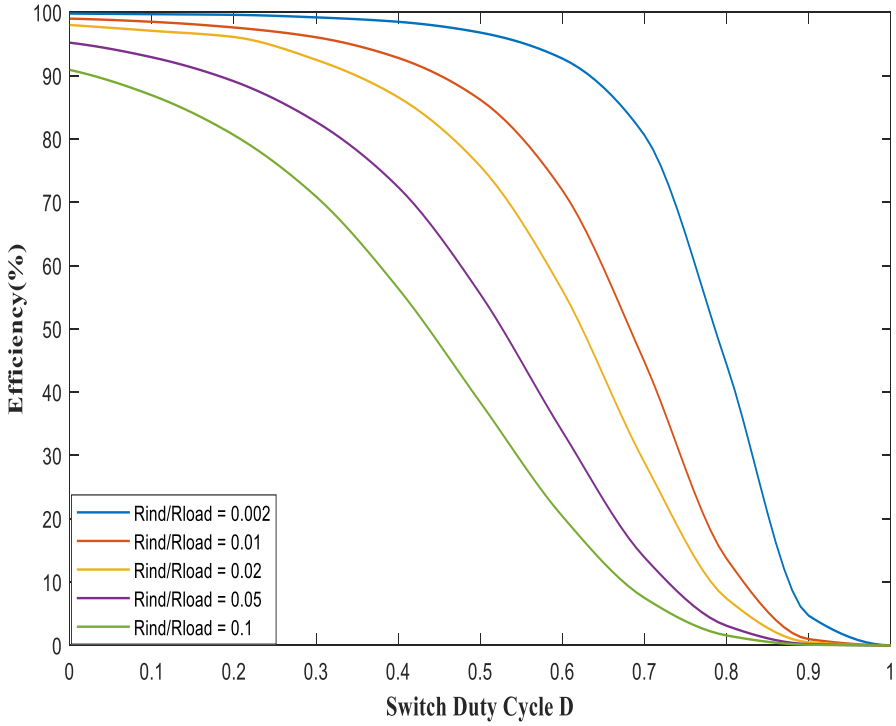


Figure 4.29 the effect of the variation of the inductors' resistance with different switches' duty ratio on the transformer's efficiency for SISO DC transformer when $V_i = 330\,V$

Analyzing of figure 4.29 suggests that a higher efficiency could be obtained with lower value of inductor's resistance as the parasitic inductance resistance degrades the voltage gain of the proposed DC transformer. Also, connection of more inputs in the system will increase the number of components and therefore the losses.

4.5.Summary

A new efficient MIMO step-up DC transformer for renewable energy systems has been proposed and presented. This proposed topology can be used to obtain different output voltage levels from several power sources, such as wind turbines, photovoltaic arrays, fuel cells, etc. Multi-Input Multi-Output transformers provide flexibility in terms of the choice and the availability of power source, reduction in the number of power lines to transfer power to pre-specified locations as well as enhancement in system reliability. The comprehensive operating principle, theoretical analysis and designing criteria have been discussed in this chapter.

The designed DC transformer has the advantages of simple configuration, fewer components, high step-up conversion ratio without using an internal AC transformer and high efficiency. Inputs and outputs are related mathematically in terms of L, C and the duty cycle of the power switches. Also discussed is the derivation of the employed the inductance L and the capacitance C in terms of size for a particular application.

The derived input and output expressions (for ideal and non-ideal transformer) are solved numerically and the results of input/output relation are validated through MATLAB/SIMULINK simulation. Tentative analysis of the results shows a close correlation.

The power losses and efficiency of the proposed DC transformer have been discussed considering the effect of the parasitic resistances of the components. As the resistance of the inductor R_{ind} significantly affects the performance of the DC transformer compared with the other parasitic resistances, therefore, it is considered in calculation of the output voltage and the transformer's efficiency.

The choice of the optimum operating switching frequency of the proposed DC transformer based on the application. In this study with the view of the proposed transformer to be connected to high voltage renewable sources and having high efficiency and conversion gain,$1\ kHz$ is chosen as the switching frequency. A case study has been performed to examine the performance of the design under two different switching frequencies:$1\ kHz$ and $10\ kHz$. The parameters have been sized under each frequency for simulation purposes. The results revealed that higher switching frequency means reduction in components' size, dimension, weight, ripple current and ripple voltage. The proposed three-input double-output DC transformer achieves the predetermined $8\ kV, 11\ kV$ which shows a high step-up conversion ratio (almost more than 20 times), with peak-to-peak ripple voltage for V_{o1}, V_{o2} will be $250\ V, 400\ V$ respectively. And with low ripple on the DC bus voltage V_o is acquired where the peak ripple voltage is $6\ V$ and the peak ripple current is $10\ A$.

CHAPTER FIVE

DEVELOPMENT AND EVALUATION OF THE PROPOSED MIMO DC TRANSFORMER CONTROLLER/s

In this chapter, the modelling and control algorithm of the proposed Multi-Input Multi-Output (MIMO) step-up DC transformer will be discussed. Where Proportional Integral Derivative (PID) controllers will be designed and integrated to control and operate the proposed DC transformer in Continuous Conduction Mode (CCM) utilising the concept of closed loop Voltage Mode Control (VMC). And then the validity of the DC transformer's control performance is demonstrated through MATLAB\SIMULINK software simulation under different scenarios of operation. Also, the system's stability will be discussed in this chapter as well as the performance of the proposed DC transformer under faulty conditions will be studied.

5.1 Introduction

In order to design a system or a plant to perform in a specific way, the relation of how the outputs react with changes in the inputs must be understood and this is captured in the mathematical modelling of the system [135]. The mathematical modelling of the linear system could be a differential equation, a transfer function, or a state space representation [135]. For example, if the system input is given as U(s) and its output Y(s) then the transfer function of the system G(s) is presented as follows:

$$G(s) = \frac{Y(s)}{U(s)} \tag{5.1}$$

Figure 5.1 depicts block representation of a transfer function.

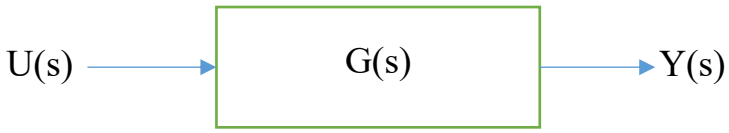


Figure 5.1 Block representation of a transfer function

To design the system or the plant controller using the classical control approach the mathematical modelling of the plant is required. This model contains all the dynamics of the plant that affects controlling it. This type of control is called a mathematician approach [136], where the designer must mathematically model the plant to be controlled. The classical

control known as the linear control depends more on the designer understanding of the plant to be controlled, as it requires some design strategies.

Within closed loop systems, the PID control is considered as a traditional linear control method which is commonly used in many applications. The PID controller is a popular control feedback used in industry due to its flexibility, robustness and easy implementation in real applications [137].

Basically, the signal driving the plant is made up of a proportional gain (K_p), an integral gain (K_i) and a derivative gain (K_d). The PID control signal is formulated as follows:

$$m(t) = K_p\, e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{5.2}$$

Where $m(t)$ is the control variable and $e(t)$ is the error over time. Figure 5.2 depicts a block diagram of a PID controller in a feedback loop.

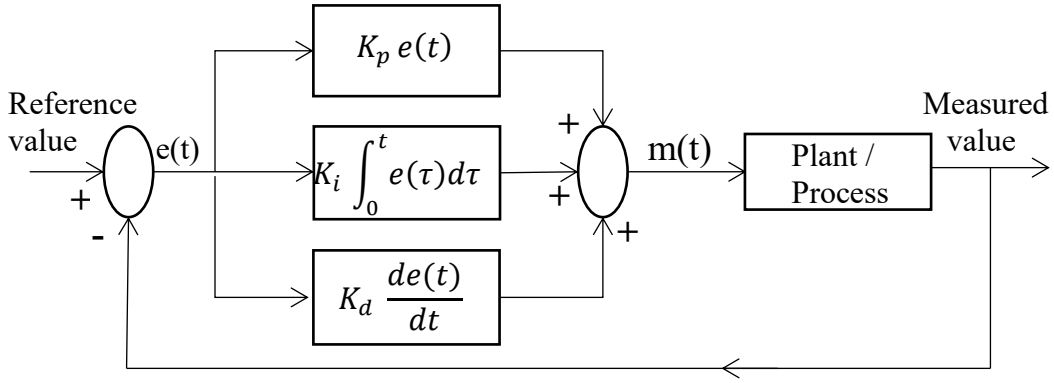


Figure 5.2 A block diagram of a PID controller in a feedback loop

Many control methods are used where the simple and low cost controller structure is always in demand for most industrial and high performance applications [135], thus classical control systems are preferable. However, intelligent control systems are used particularly for highly non-linear systems where a system or a plant model is difficult or impossible to obtain or for cases when classical control methods fail to control the system [136]. In this research a classical PID controller has been used to control the proposed MIMO DC transformer.

5.2 The proposed MIMO DC transformer Structure and Operation Principles

The DC transformers have two distinct operation modes: CCM and DCM. In practice, a transformer may operate in both modes, which have significantly different characteristics. However, in this research the MIMO DC transformer has been considered to operate only in CCM. The CCM is used for efficient power conversion especially for renewable energy

system applications [42] while, DCM is considered in low power applications or stand-by operation [133] as well as for large load variation applications.

In order to design the system controller using the classical PID control method, the mathematical modelling of the plant is required. This model contains all the dynamics of the plant that are needed for the design. Thus, to formulate the dynamic model of the system or the plant, design structure and its operation principles must be obtained.

Figure 5.3 shows the general block diagram of the proposed MIMO DC transformer with local and master control. It is clear that the control variables in the system will depend on the number of inputs and outputs. Thus, in order

to find the mathematical model of the design an example of three-input double-output DC transformer configuration has been chosen as shown in figure 5.4.

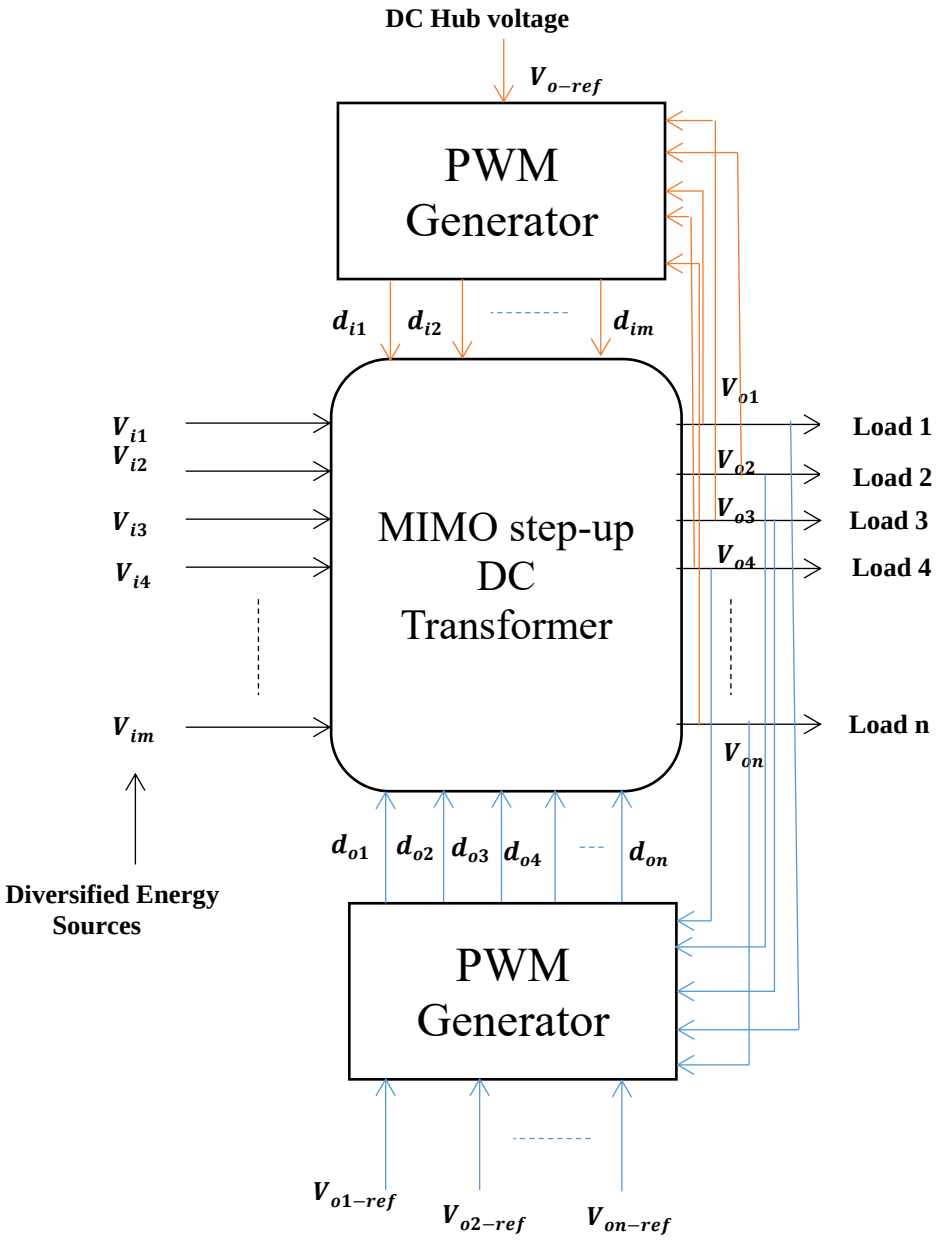


Figure 5.3 the general block diagram of the proposed MIMO DC transformer with local and master control

As discussed in the previous chapter, figure 5.4 depicts the proposed DC transformer topology of three-input two-output configuration where a three input sources V_{i1}, V_{i2} and V_{i3} are responsible for supplying the loads (R_{L1} and R_{L2}). The transformer is designed to operate in CCM where the inductor's current will never go to zero. In this mode the five switches($S_{i1}, S_{i2}, S_{i3}, S_{o1}$ and S_{o2}) of figure 5.4 are active. For example, S_{i1}, S_{i2} and S_{i3} are active to regulate the inductor currents I_{Li1}, I_{Li2} and I_{Li3} from the input sources V_{i1}, V_{i2} and V_{i3} to the desired value by controlling their respective switching duty ratio. This in turn will regulate the DC bus voltage $V_o = (V_{ci1} + V_{ci2} + V_{ci3})$ to a desired value. Similarly, the output voltage V_{o1} and V_{o2} are regulated by controlling the output power switches S_{o1} and S_{o2}.

The switching algorithm of the proposed design has been discussed in section 4.2 and the switching states have been provided including the mathematical representation of the inductors and capacitors currents and voltages in steady state condition. While here the dynamic modelling of the proposed design will be provided based on the discussed switching states as shown in figure 5.5. It is clear that there are five active switches of the proposed three-input two-output topology and each switch has two switching states ON and OFF.

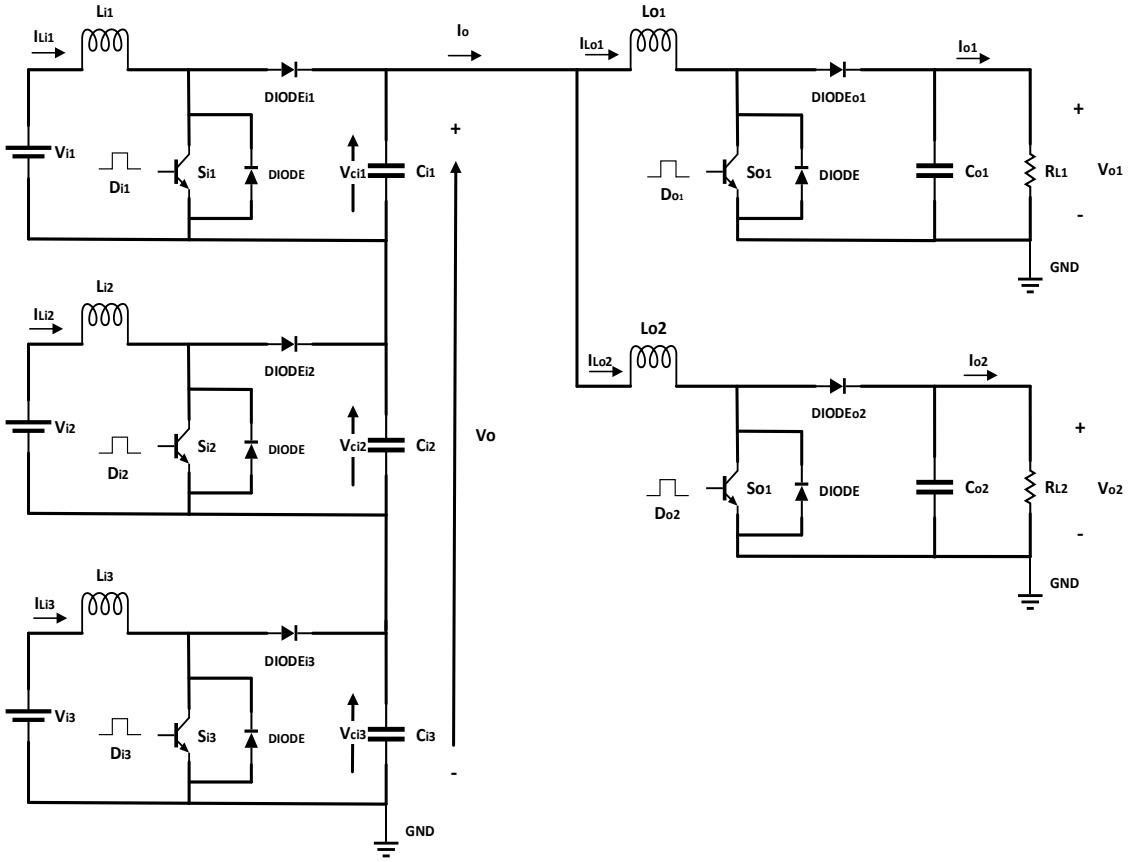


Figure 5.4 Three input double output step-up DC transformer topology

According to the switches' states, there are four different switching states in one switching period as shown in figure 5.5. For each state the inductor and capacitor equations have been derived as follows:

e) Switching state 1: In this state, the input power switches S_{i1} , S_{i2} and S_{i3} are turned ON, while the output switches $S_{o1}$and S_{o2} are turned OFF. When the input switches are ON the input stage diodes are reverse biased. Assuming that the output capacitors are fully charged, and the power is delivered to the loads; $R_{L1}$and R_{L2}. The equivalent circuit of the proposed transformer in this state is shown in figure 5.5(a). In this state, V_{i1}, V_{i2} and V_{i3} charge the inductors L_{i1}, L_{i2} and L_{i3}respectively, so the inductors' currents increase, and the output capacitors are discharged.

The equations for the inductors and capacitors in this state are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= v_{i1} \\ L_{i2}\frac{di}{dt} &= v_{i2} \\ L_{i3}\frac{di}{dt} &= v_{i3} \\ C_{i1}\frac{dv_{ci1}}{dt} &= -i_o \\ C_{i2}\frac{dv_{ci2}}{dt} &= -i_o \\ C_{i3}\frac{dv_{ci3}}{dt} &= -i_o \\ L_{o1}\frac{di}{dt} &= v_o - v_{co1} \\ L_{o2}\frac{di}{dt} &= v_o - v_{co2} \\ C_{o1}\frac{dv_{co1}}{dt} &= i_{Lo1} - \frac{v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= i_{Lo2} - \frac{v_{o2}}{R_{L2}} \end{aligned}\right\} \quad (5.3)$$

f) Switching state 2: In this state, the input power switches S_{i1} , S_{i2} and S_{i3} are still ON, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are ON, the input stage diodes are reversed biased. Assuming that the input capacitors are fully charged, thus the power will deliver to the load $R_{L1}$and R_{L2}. Equivalent circuit of the proposed transformer in this state is shown in figure 5.5(b). In this state, V_{i1}, V_{i2} and V_{i3} charge the inductors L_{i1}, L_{i2} and L_{i3} respectively, also the output inductors L_{o1} and L_{o2} are charged from the capacitors C_{i1}, C_{i2} and C_{i3}. Consequently, the inductors' currents I_{Lo1}, I_{Lo2} increase and the capacitors C_{o1}, C_{o2} are discharged.

The equations for the inductors and capacitors in this state are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= v_{i1} \\ L_{i2}\frac{di}{dt} &= v_{i2} \\ L_{i3}\frac{di}{dt} &= v_{i3} \\ L_{o1}\frac{di}{dt} &= v_{o} \\ L_{o2}\frac{di}{dt} &= v_{o} \\ C_{i1}\frac{dv_{ci1}}{dt} &= -(i_{Lo1}+i_{Lo2}) \\ C_{i2}\frac{dv_{ci2}}{dt} &= -(i_{Lo1}+i_{Lo2}) \\ C_{i3}\frac{dv_{ci3}}{dt} &= -(i_{Lo1}+i_{Lo2}) \\ C_{o1}\frac{dv_{co1}}{dt} &= \frac{-v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= \frac{-v_{o2}}{R_{L2}} \end{aligned}\right\} \quad (5.4)$$

g) Switching state 3: In this state, the input power switches S_{i1} , S_{i2} and S_{i3} are turned OFF, and also the output switches S_{o1} and S_{o2} are turned OFF. When the input switches are OFF the input stage diodes are forward biased. In this state the stored energy in the input inductors will be used to charge the capacitors C_{i1}, C_{i2} and C_{i3}. Similarly, the stored energy in the output inductors will be used to charge the output capacitors C_{o1} and C_{o2} and also the stored energy in each output capacitor is delivered to the loads R_{L1} and R_{L2} . The equivalent circuit of the proposed transformer in this state is shown in figure 5.5(c). In this state, the inductors' current I_{Li1}, I_{Li2} and I_{Li3} will decrease while charging the capacitors C_{i1}, C_{i2} and C_{i3}.

The equations for the inductors and capacitors in this state are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= v_{i1} - v_{ci1} \\ L_{i2}\frac{di}{dt} &= v_{i2} - v_{ci2} \\ L_{i3}\frac{di}{dt} &= v_{i3} - v_{ci3} \\ L_{o1}\frac{di}{dt} &= v_{o} - v_{co1} \\ L_{o2}\frac{di}{dt} &= v_{o} - v_{co2} \\ C_{i1}\frac{dv_{ci1}}{dt} &= i_{Li1} - i_{o} \\ C_{i2}\frac{dv_{ci2}}{dt} &= i_{Li2} - i_{o} \\ C_{i3}\frac{dv_{ci3}}{dt} &= i_{Li3} - i_{o} \\ C_{o1}\frac{dv_{co1}}{dt} &= i_{Lo1} - \frac{v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= i_{Lo2} - \frac{v_{o2}}{R_{L2}} \end{aligned}\right\} \quad (5.5)$$

h) Switching state 4: In this state, the input power switches S_{i1} , S_{i2} and S_{i3} are still OFF, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are OFF the input stage diodes are forward biased. In this state the stored energy in the input inductors keep charging the capacitors C_{i1}, C_{i2} and C_{i3}. In addition, the stored energy in the input inductors will be delivered to L_{o1} and L_{o2} through the switches S_{o1} and S_{o2} respectively. So, the inductors' current I_{Li1}, I_{Li2} and I_{Li3} keep decreasing, while I_{Lo1} and I_{Lo2} increases. In addition, the capacitors C_{o1} and C_{o2} will discharge through the loads $R_{L1}$and R_{L2}. The equivalent circuit of the proposed DC transformer in this state is shown in figure 5.5(d). In this state, the capacitors C_{i1}, C_{i2} and C_{i3} are charged.

The equations for the inductors and capacitors in this state are as follows:

$$\left.\begin{aligned} L_{i1}\frac{di}{dt} &= v_{i1} - v_{ci1} \\ L_{i2}\frac{di}{dt} &= v_{i2} - v_{ci2} \\ L_{i3}\frac{di}{dt} &= v_{i3} - v_{ic3} \\ L_{o1}\frac{di}{dt} &= v_o \\ L_{o2}\frac{di}{dt} &= v_o \\ C_{i1}\frac{dv_o}{dt} &= i_{Li1} - i_o \\ C_{i2}\frac{dv_o}{dt} &= i_{Li2} - i_o \\ C_{i3}\frac{dv_o}{dt} &= i_{Li3} - i_o \\ C_{o1}\frac{dv_{co1}}{dt} &= \frac{-v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} &= \frac{-v_{o2}}{R_{L2}} \end{aligned}\right\} \quad (5.6)$$

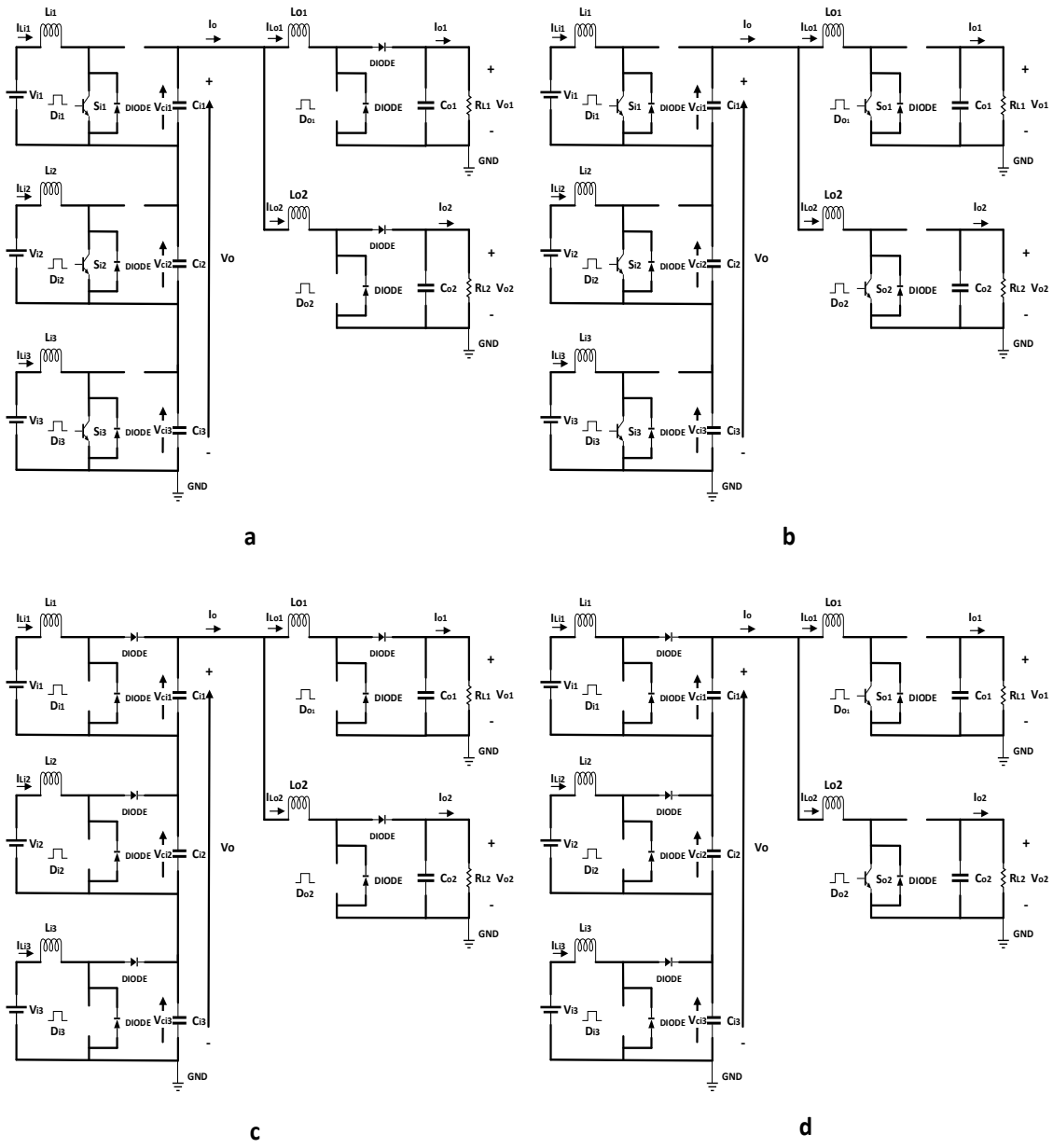


Figure 5.5 Equivalent circuit of step-up DC transformer operation mode, (a) switching state 1, (b) switching state 2, (c) switching state 3, (d) switching state 4.

5.3 Dynamic Modelling of the Proposed MIMO DC Transformer

The proposed DC transformer is controlled by $S_{i1}, S_{i2}, S_{i3}, S_{o1}$and S_{o1} switches. Each switch has its own specific duty ratio. By proper regulation of switches' duty cycles, the output voltages V_{o1}, V_{o2} are adjustable.

To design the closed loop control for the transformer, first the dynamic model must be obtained. Then as stated before in the operation mode section, in order to control the two output voltages; regulation of the DC bus voltage V_o is needed. Furthermore, as each input circuit has its own power switch and different values for parameters, thus different controllers need to be designed.

The concept of Small Signal Model (SSM) as mentioned in section 3.3 is the basis for optimised controller design. Especially, for MIMO DC transformers, an effective model will be helpful to realise the closed loop control, and to optimise the transformer dynamics [138]. Unlike the conventional Single Input Single Output (SISO) transformers, the MIMO DC transformer is a high order system and hence the derivation of the transfer function of each plant is extensive.

5.3.1 Linearisation of MIMO DC Transformer Using State Space Averaging Approach

The dynamics of any plant can be described in a matrix form which represents its transfer functions. Based on the small signal modelling method [20], the state variables (x), the duty ratios (d) and the input voltages (v), all contains two components namely: DC values (X, D, and V) and disturbance values ($\hat{x}, \hat{d}, \hat{v}$). It is assumed that the deviations of a system from its normal state, caused by an outside influence (uncontrollable influences) are small and do not vary significantly during one switching period. So, the dynamic of the considered example of the proposed DC transformer equations are as follows:

$$\left.\begin{aligned} i_{Li}(t) &= I_{Li} + \hat{\imath}_{Li}(t) \\ i_{Lo}(t) &= I_{Lo} + \hat{\imath}_{Lo}(t) \\ v_{o1}(t) &= V_{o1} + \hat{v}_{o1}(t) \\ v_{o2}(t) &= V_{o2} + \hat{v}_{o2}(t) \\ d_{i1}(t) &= D_{i1} + \hat{d}_{i1}(t) \\ d_{i2}(t) &= D_{i2} + \hat{d}_{i2}(t) \\ d_{i3}(t) &= D_{i3} + \hat{d}_{i3}(t) \\ d_{o1}(t) &= D_{o1} + \hat{d}_{o1}(t) \\ d_{o2}(t) &= D_{o2} + \hat{d}_{o2}(t) \end{aligned}\right\} \quad (5.7)$$

Where $i_{Li}(t)$ and $i_{Lo}(t)$ are the input and output inductors' current and the output capacitors' voltage $v_{o1}(t)$ and $v_{o2}(t)$ are the plant state variables. The system could be represented in a matrix form using a state space averaging model that has been widely used as a way to formulate various small signal and averaged DC transfer functions [139]. As a result, a model could be developed which ignores the effects of the high frequency switching which, allows for a linear SSM to be developed [140].

The SSM could be developed using the state space model technique which takes the following form:

$$\left.\begin{aligned} \frac{dx}{dt} &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t) \end{aligned}\right\} \quad (5.8)$$

Where $x(t)$ is a matrix containing the state variables, $u(t)$ is a matrix containing the control inputs $d_{i1}(t), d_{i2}(t), d_{i3}(t), d_{o1}(t), d_{o2}(t)$ and $y(t)$ is a matrix containing the system outputs $v_{o1}(t), v_{o2}(t)$ for three-input two-output DC transformer.

Matrices $x(t)$, $y(t)$ and $u(t)$ take following form:

$$x(t) = \begin{bmatrix} i_{Li1}(t) \\ v_{ci1}(t) \\ i_{Li2}(t) \\ v_{ci2}(t) \\ i_{Li3}(t) \\ v_{ci3}(t) \\ i_{Lo1}(t) \\ v_{o1}(t) \\ i_{Lo2}(t) \\ v_{o2}(t) \end{bmatrix}, y(t) = \begin{bmatrix} v_{ci1}(t) \\ v_{ci2}(t) \\ v_{ci3}(t) \\ v_{o1}(t) \\ v_{o2}(t) \end{bmatrix}, \; u(t) = \begin{bmatrix} d_{i1}(t) \\ d_{i2}(t) \\ d_{i3}(t) \\ d_{o1}(t) \\ d_{o2}(t) \end{bmatrix} \tag{5.9}$$

A, B, C and D are the system matrices $S\ (A, B, C, D)$ as discussed in section 3.3.1.

It is clear that there are ten state variables for the system (three-input two-output) as shown in equation (5.9). To find the A, B matrices the averaging model of the previous inductors' and capacitors' equations (5.3)- (5.6) for each switching state is applied.

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \\ \dot{x_4} \\ \dot{x_5} \\ \dot{x_6} \\ \dot{x_7} \\ \dot{x_8} \\ \dot{x_9} \\ \dot{x_{10}} \end{bmatrix} = \begin{bmatrix} a_{11} & \cdots & a_{110} \\ \vdots & \ddots & \vdots \\ a_{101} & \cdots & a_{1010} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ x_{10} \end{bmatrix} + \begin{bmatrix} b_{11} & \cdots & b_{15} \\ \vdots & \ddots & \vdots \\ b_{101} & \cdots & b_{105} \end{bmatrix} u \tag{5.10}$$

The state space variables $x_1$to x_{10} of the system could be found by substitution of (5.7) into (5.3) - (5.6). Then the averaging model is applied and multiplied by its corresponding duty cycle value. This is done by dividing the system into five subsystems and each subsystem has two state variables.

The state variables of the first input subsystem are as follows:

$$x_1 = i_{Li1}(t)$$
$$x_2 = v_{ci1}(t)$$

$$\dot{x_1} = \frac{1}{L_{i1}}\,(V_{i1} + \hat{v}_{i1}(t)) - \frac{\left(1 - (D_{i1} + \hat{d}_{i1}(t))\right)}{L_{i1}}\,(V_{ci1} + \hat{v}_{ci1}(t)) \tag{5.11}$$

$$\dot{x_1} = \frac{1}{L_{i1}}\left(V_{i1} + \hat{v}_{i1}(t)\right) - \frac{(1 - D_{i1})}{L_{i1}}\,V_{ci1} - \underbrace{\frac{V_{ci1}}{L_{i1}}\hat{d}_{i1}(t) + \frac{(1 - D_{i1})}{L_{i1}}\hat{v}_{ci1}(t)}_{\text{First order AC terms (linear)}} \underbrace{- \frac{1}{L_{i1}}\hat{v}_{ci1}(t)\hat{d}_{i1}(t))}_{\text{Second order AC terms (nonlinear) (neglected)}} \tag{5.12}$$

$$\dot{x_2} = \frac{\left(1 - (D_{i1} + \hat{d}_{i1}(t)\right)}{C_{i1}}(I_{Li1} + \hat{\imath}_{Li1}(t)) - \frac{1}{C_{i1}}((I_{Lo1} + \hat{\imath}_{Lo1}(t)) + (I_{Lo2} + \hat{\imath}_{Lo2}(t))) \tag{5.13}$$

$$\dot{x_2} = \frac{(1 - D_{i1})}{C_{i1}}I_{Li1} - \frac{I_{Li1}}{C_{i1}}\,\hat{d}_{i1}(t)) - \frac{1}{C_{i1}}(I_{Lo1} + \hat{\imath}_{Lo1}(t)) - \frac{1}{C_{i1}}(I_{Lo2} + \hat{\imath}_{Lo2}(t)) \tag{5.14}$$

Similarly, for the second input subsystem, the state variables are:

$$x_3 = i_{Li2}(t)$$

$$x_4 = v_{ci2}(t)$$

$$\dot{x_3} = \frac{1}{L_{i2}}\,(V_{i2} + \hat{v}_{i2}(t)) - \frac{\left(1 - (D_{i2} + \hat{d}_{i2}(t)\right)}{L_{i2}}\,(V_{ci2} + \hat{v}_{ci2}(t)) \tag{5.15}$$

$$\dot{x_4} = \frac{\left(1 - (D_{i2} + \hat{d}_{i2}(t)\right)}{C_{i2}}\,(I_{Li2} + \hat{\imath}_{Li2}(t)) - \frac{1}{C_{i2}}((I_{Lo1} + \hat{\imath}_{Lo1}(t)) + (I_{Lo2} + \hat{\imath}_{Lo2}(t))) \tag{5.16}$$

And for the third input subsystem,

$$x_5 = i_{Li3}(t)$$

$$x_6 = v_{ci3}(t)$$

$$\dot{x_5} = \frac{1}{L_{i3}}\,(V_{i3} + \hat{v}_{i3}(t)) - \frac{\left(1 - (D_{i3} + \hat{d}_{i3}(t)\right)}{L_{i3}}\,(V_{ci3} + \hat{v}_{ci3}(t)) \tag{5.17}$$

$$\dot{x_6} = \frac{\left(1-(D_{i3}+\hat{d}_{i3}(t)\right)}{C_{i3}}\left(I_{Li2}+\hat{\imath}_{Li2}(t)\right) - \frac{1}{C_{i3}}\left(\left(I_{Lo1}+\cdots\right.\right. \\ \left.\left.\hat{\imath}_{Lo1}(t)\right)+\left(I_{Lo2}+\hat{\imath}_{Lo2}(t)\right)\right) \tag{5.18}$$

For the first output subsystem the two state variable are:

$$x_7 = i_{Lo1}(t)$$

$$x_8 = v_{o1}(t)$$

$$\dot{x_7} = \frac{(D_{o1}+\hat{d}_{o1}(t)}{L_{o1}}\left(V_o+\hat{v}_o(t)\right)+\cdots \\ \frac{\left(1-(D_{o1}+\hat{d}_{o1}(t)\right)}{L_{o1}}\left(V_o+\hat{v}_o(t)\right)-\left(V_{o1}+\cdots\right. \\ \left.\hat{v}_{o1}(t)\right)\big) \tag{5.19}$$

As,

$$v_o(t) = v_{ci1}(t)+v_{ci2}(t)+v_{ci3}(t) \tag{5.20}$$

$$v_o(t) = x_2+x_4+x_6 \tag{5.21}$$

Substitute $v_o(t)$ then

$$\dot{x_7} = \frac{1}{L_{o1}}(x_2)+\frac{1}{L_{o1}}(x_4)+\frac{1}{L_{o1}}(x_6)+\frac{-\left(1-(D_{o1}+\hat{d}_{o1}(t)\right)}{L_{o1}}(x_8) \tag{5.22}$$

$$\dot{x_8} = \frac{-1}{R_{L1}C_{o1}}\left(V_{o1}+\hat{v}_{o1}(t)\right)+\frac{\left(1-(D_{o1}+\hat{d}_{o1}(t)\right)}{C_{o1}}\left(I_{Lo1}+\hat{\imath}_{Lo1}(t)\right) \tag{5.23}$$

And similarly, for the second output subsystem, the state variables are:

$$x_9 = i_{Lo2}(t)$$

$$x_{10} = v_{o2}(t)$$

$$\dot{x_9} = \frac{(D_{o2}+\hat{d}_{o2}(t)}{L_{o2}}\left(V_o+\hat{v}_o(t)\right)+\frac{\left(1-(D_{o2}+\hat{d}_{o2}(t)\right)}{L_{o2}}\left(V_o+\hat{v}_o(t)\right)-\left(V_{o2}\right. \\ \left.+\cdots\quad\hat{v}_{o2}(t)\right)\big) \tag{5.24}$$

$$\dot{x_9} = \frac{1}{L_{o2}}(x_2)+\frac{1}{L_{o2}}(x_4)+\frac{1}{L_{o2}}(x_6)+\frac{-\left(1-(D_{o2}+\hat{d}_{o2}(t)\right)}{L_{o2}}(x_{10}) \tag{5.25}$$

$$\dot{x_{10}} = \frac{-1}{R_{L2}C_{o2}}(V_{o2} + \hat{v}_{o2}(t)) + \frac{\left(1 - (D_{o2} + \hat{d}_{o2}(t)\right)}{C_{o2}} (I_{Lo2} + \hat{\imath}_{Lo2}(t)) \tag{5.26}$$

$$\dot{x_{10}} = \frac{-1}{R_{L2}C_{o2}}(x_{10}) + \frac{\left(1 - (D_{o2} + \hat{d}_{o2}(t)\right)}{C_{o2}} (x_9) \tag{5.27}$$

Hence, the general stat space representation equations of the proposed MIMO DC transformer on the input and output sides are described in the following.

- The input side of the proposed MIMO DC transformer

The chosen state variables are:

$$\left.\begin{matrix} x_{(2k-1)} = i_{Lik}(t) \\ x_{(2k)} = v_{cik}(t) \end{matrix}\right\} \ , k = 1,2,3, \dots \dots, m$$

The time derivation of the chosen system's states variables are defined as:

$$\left.\begin{matrix} \dot{x_{(2k-1)}} = \frac{1}{L_{ik}} V_{ik} - \frac{(1 - d_{ik})}{L_{ik}} x_{(2k)} \\ \dot{x_{(2k)}} = \frac{-d_{ik}}{C_{ik}} \left(\sum_{j=m+1}^{n} x_{(2j-1)} \right) + \frac{(1 - d_{ik})}{C_{ik}} x_{(2k-1)} \end{matrix}\right\} \tag{5.28}$$

Where (m) is the number of inputs of the proposed transformer and (n) is the number of outputs.

And the duty ratio on the input side is expressed as:

$$d_i = \frac{t_{on}}{t_{on} + t_{off}} \tag{5.29}$$

To illustrate the above general expressions, as an example the first input is taken as $k = 1$, and its corresponding two states variables are defined as:

$$\left.\begin{matrix} x_{(1)} = i_{Li1}(t) \\ x_{(2)} = v_{ci1}(t) \end{matrix}\right\}$$

And the derivative of the first state variables is:

$$\dot{x_{(1)}} = \frac{dI_{Li1}(t)}{dt} = \frac{1}{L_{i1}} V_{L_{i1}} \tag{5.30}$$

The inductor's voltage over ON and OFF states is:

$$\left.\begin{aligned} V_{L_{i1_{ON}}} &= V_{i1}d_{i1}\,, & S_{i1}\ ON \\ V_{L_{i1_{OFF}}} &= (V_{i1}-V_{ci1})(1-d_{i1})\,, & S_{i1}\ OFF \end{aligned}\right\} \tag{5.31}$$

Then for one switching period the inductor's voltage is:

$$V_{L_{i1}} = V_{L_{i1_{ON}}} + V_{L_{i1_{OFF}}} \tag{5.32}$$

Substituting for parameters in the above equation yields:

$$\dot{x_{(1)}} = \frac{1}{L_{i1}}V_{i1} - \frac{(1-d_{i1})}{L_{i1}}x_{(2)} \tag{5.33}$$

And the second state variable can be expressed as:

$$\dot{x_{(2)}} = \frac{1}{C_{i1}}i_{ci1}(t) \tag{5.34}$$

$$\left.\begin{aligned} I_{c_{i1_{ON}}} &= -\,i_o(t)d_{i1}, & S_{i1}\ ON \\ I_{c_{i1_{OFF}}} &= i_{Li1}(t)(1-d_{i1})\,, & S_{i1}\ OFF \end{aligned}\right\} \tag{5.35}$$

Referring to figure 5.4 the output current $i_o(t)$ in general is given as:

$$i_o(t) = -[(I_{Lo_1}(t) + I_{Lo_2}(t) + \cdots .. + I_{Lo_n}(t)] \tag{5.36}$$

$$\dot{x_{(2)}} = \frac{1}{C_{i1}}\left[\left(-d_{i1}\sum_{j=m+1}^{k=m+n} x_{(2j-1)}\right) + i_{Li1}(t)(1-d_{i1})\right] \tag{5.37}$$

In the considered example where $m = 3$ (number of inputs), $j = m+1 = 4$ and $n = 2$ (number of outputs), equation (5.37) becomes:

$$\dot{x_{(2)}} = \frac{-d_{i1}}{C_{i1}}[x_{(7)} + x_{(9)}] + \frac{(1-d_{i1})}{C_{i1}}x_{(1)} \tag{5.38}$$

Then on the input side of the proposed DC transformer all the state variables could be found following the above procedure.

- The outputs side of the proposed MIMO DC Transformer

Each output has two state variables such as:

$$\left.\begin{aligned} x_{(2j-1)} &= i_{Lo(j-m)}(t) \\ x_{(2j)} &= v_{co(j-m)}(t) \end{aligned}\right\}\ , j = (m+1), (m+2), \ldots, (m+n) \tag{5.39}$$

The general time derivation of the system's states variables are:

$$\left.\begin{aligned} \dot{x_{(2j-1)}} &= \frac{1}{L_{o(j-m)}}\left(\sum_{i=1}^{m} x_{(2i)}\right) - \frac{\left(1-d_{o(j-m)}\right)}{L_{o(j-m)}} x_{(2j)} \\ \dot{x_{(2j)}} &= \frac{\left(1-d_{o(j-m)}\right)}{C_{o(j-m)}}\, x_{(2j-1)} + \frac{-1}{R_L C_{o(j-m)}} x_{(2j)} \end{aligned}\right\} \tag{5.40}$$

5.3.2 MIMO DC Transformer Transfer Functions

To find the system's transfer functions, the System matrices $S\,(A,B,C,D)$ could be represented from the above state space model as:

$$A = \begin{bmatrix} 0 & \frac{-(1-D_{i1})}{L_{i1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-D_{i1})}{C_{i1}} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_{i1}} & 0 & \frac{-1}{C_{i1}} & 0 \\ 0 & 0 & 0 & \frac{-(1-D_{i2})}{L_{i2}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{(1-D_{i2})}{C_{i2}} & 0 & 0 & 0 & \frac{-1}{C_{i2}} & 0 & \frac{-1}{C_{i2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-(1-D_{i3})}{L_{i3}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{(1-D_{i3})}{C_{i3}} & 0 & \frac{-1}{C_{i3}} & 0 & \frac{-1}{C_{i3}} & 0 \\ 0 & \frac{1}{L_{o1}} & 0 & \frac{1}{L_{o1}} & 0 & \frac{1}{L_{o1}} & 0 & \frac{-(1-D_{o1})}{L_{o1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-D_{o1}}{C_{o1}} & \frac{-1}{R_{L1}C_{o1}} & 0 & 0 \\ 0 & \frac{1}{L_{o2}} & 0 & \frac{1}{L_{o2}} & 0 & \frac{1}{L_{o2}} & 0 & 0 & 0 & \frac{-(1-D_{o2})}{L_{o2}} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{(1-D_{o2})}{C_{o2}} & \frac{-1}{R_{L2}C_{o2}} \end{bmatrix} \tag{5.41}$$

$$B = \begin{bmatrix} \frac{-V_{ci1}}{L_{i1}} & 0 & 0 & 0 & 0 \\ \frac{I_{Li1}}{C_{i1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-V_{ci2}}{L_{i2}} & 0 & 0 & 0 \\ 0 & \frac{I_{Li2}}{C_{i2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{-V_{ci3}}{L_{i3}} & 0 & 0 \\ 0 & 0 & \frac{I_{Li3}}{C_{i3}} & 0 & 0 \\ 0 & 0 & 0 & \frac{V_{o1}}{L_{o1}} & 0 \\ 0 & 0 & 0 & \frac{-I_{Lo1}}{C_{o1}} & 0 \\ 0 & 0 & 0 & 0 & \frac{V_{o2}}{L_{o2}} \\ 0 & 0 & 0 & 0 & \frac{-I_{Lo2}}{C_{o2}} \end{bmatrix} \tag{5.42}$$

Knowing that,

$$y(t) = Cx(t) + Du(t) \tag{5.43}$$

Given,

$$C = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{5.44}$$

From the system state space equations, one can see that there is no direct effect from the control variables to the system output. As the system output is related to the matrix C and the system's state variables, thus the D matrix is represented as a null matrix:

$$D = [0]$$

In the matrices A, B, C and D, all parameters except duty cycle of the five power switches D_{i1}, D_{i2} and D_{i3} (for three inputs), D_{o1} and D_{o2} (for two outputs) are known. The duty cycle ratio value of all the switches are obtained by steady state equations which are expressed as:

$$D_{i1} = 1 - \frac{V_{i1}}{V_{ci1}} \tag{5.45}$$

$$D_{i2} = 1 - \frac{V_{i2}}{V_{ci2}} \tag{5.46}$$

$$D_{i3} = 1 - \frac{V_{i3}}{V_{ci3}} \tag{5.47}$$

$$D_{o1} = 1 - \frac{V_o}{V_{o1}} \tag{5.48}$$

$$D_{o2} = 1 - \frac{V_o}{V_{o2}} \tag{5.49}$$

In the considered example system (three-input two-output), the state variables controlled by five control variables $\hat{d}_{i1}(t), \hat{d}_{i2}(t), \hat{d}_{i3}(t), \hat{d}_{i4}(t)$and $\hat{d}_{i5}(t)$. The transfer function matrix of the transformer is obtained from the SSM represented by state space equations as follows:

$$G = C(SI - A)^{-1}B + D \tag{5.50}$$

The rank of the transfer function matrix depends on the control variables. Therefore, in the considered example system (three-input two-output), the rank of the transfer function matrix G is 5×5.

Hence in general form:

$$y = Gu \tag{5.51}$$

Or in a matrix form:

$$\begin{bmatrix} \hat{y}_1 \\ \hat{y}_2 \\ \hat{y}_3 \\ \hat{y}_4 \\ \hat{y}_5 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} & g_{15} \\ g_{21} & g_{22} & g_{23} & g_{24} & g_{25} \\ g_{31} & g_{32} & g_{33} & g_{34} & g_{35} \\ g_{41} & g_{42} & g_{43} & g_{44} & g_{45} \\ g_{51} & g_{52} & g_{53} & g_{54} & g_{55} \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \\ \hat{u}_3 \\ \hat{u}_4 \\ \hat{u}_5 \end{bmatrix} \tag{5.52}$$

Where y and u are the system (three-input two-output DC transformer) output and input vectors respectively, and component g_{ij} represents the transfer function between $\hat{y}_i$ and $\hat{u}_j$. So, the five transfer functions are as follows:

$$\begin{bmatrix} \hat{v}_{ci1} \\ \hat{v}_{ci2} \\ \hat{v}_{ci3} \\ \hat{v}_{o1} \\ \hat{v}_{o2} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} & g_{15} \\ g_{21} & g_{22} & g_{23} & g_{24} & g_{25} \\ g_{31} & g_{32} & g_{33} & g_{34} & g_{35} \\ g_{41} & g_{42} & g_{43} & g_{44} & g_{45} \\ g_{51} & g_{52} & g_{53} & g_{54} & g_{55} \end{bmatrix} \begin{bmatrix} \hat{d}_{i1} \\ \hat{d}_{i2} \\ \hat{d}_{i3} \\ \hat{d}_{o1} \\ \hat{d}_{o2} \end{bmatrix} \tag{5.53}$$

$$\left.\begin{aligned} g_{11} &= \frac{\hat{v}_{ci1}}{\hat{d}_{i1}} \\ g_{22} &= \frac{\hat{v}_{ci2}}{\hat{d}_{i2}} \\ g_{33} &= \frac{\hat{v}_{ci3}}{\hat{d}_{i3}} \\ g_{44} &= \frac{\hat{v}_{o1}}{\hat{d}_{o1}} \\ g_{55} &= \frac{\hat{v}_{o2}}{\hat{d}_{o2}} \end{aligned}\right\} \tag{5.54}$$

As demonstrated so far, the transfer functions of the system or plant are extensive and need a lot of mathematical operations. To overcome this MATLAB software has been used to obtain the transfer functions of the system as follows:

$$g_{11}=\frac{\hat{v}_{ci1}}{\hat{d}_{i1}}=\frac{0.08X_1S^9+(0.64X_1-14.8X_2)S^8+(1.48X_1-111X_2)S^7+(0.68*10^5X_1-273X_2)S^6+(0.68*10^9X_1-140.6X_2)S^5+(1.86*10^9X_1-125.8X_2)S^4+(0.86*10^{13}X_1-344.1X_2)S^3+(1.22*10^{13}X_1-159.1X_2)S^2+(0.3*10^{17}X_1-225.7X_2)S-55.5*10^{17}X_2}{L_{i1}C_{i1}(0.09S^{10}+0.65\,S^9+1.6*10^4\,S^8+8.7*10^4\,S^7+8.8*10^8\,S^6+2.8*10^9\,S^5+1.6*10^{13}\,S^4+3.4*10^{14}\,S^3+1.2*10^{17}\,S^2+1.3*10^{17}\,S+2.8*10^{20})} \quad (5.54.a)$$

$$g_{22}=\frac{\hat{v}_{ci2}}{\hat{d}_{i2}}=\frac{0.09X_3S^9+(0.66X_3-6.02X_4)S^8+(1.3*10^3X_3-43X_4)S^7+(0.65*10^5X_3-86*10^4X_4)S^6+(5.85*10^8X_3-25.8*10^5X_4)S^5+(1.3*10^9X_3-38.7*10^9X_4)S^4+(0.71*10^{13}X_3-8.6*10^{10}X_4)S^3+(7.8*10^{12}X_3-47.3*10^{13}X_4)S^2+(2.6*10^{16}X_3-51.6*10^{13}X_4)S-17.2*10^{17}X_4}{L_{i2}C_{i2}(0.09S^{10}+0.65\,S^9+1.6*10^4\,S^8+8.7*10^4\,S^7+8.8*10^8\,S^6+2.8*10^9\,S^5+1.6*10^{13}\,S^4+3.4*10^{14}\,S^3+1.2*10^{17}\,S^2+1.3*10^{17}\,S+2.8*10^{20})} \quad (5.54.b)$$

$$g_{33}=\frac{\hat{v}_{ci3}}{\hat{d}_{i3}}=\frac{0.09X_5S^9+(0.64X_5-2.8X_6)S^8+(1.4*10^3X_5-21X_6)S^7+(71*10^3X_5-49*10^4X_6)S^6+(6.4*10^8X_5-24.8*10^5X_6)S^5+(1.6*10^9X_5-22.4*10^9X_6)S^4+(0.77*10^{13}X_5-3.85*10^{12}X_6)S^3+(9.7*10^{12}X_5-26.6*10^{13}X_6)S^2+(2.6*10^{16}X_5-34.6*10^{13}X_6)S-9.1*10^{17}X_6}{L_{i3}C_{i3}(0.09S^{10}+0.65\,S^9+1.6*10^4\,S^8+8.7*10^4\,S^7+8.8*10^8\,S^6+2.8*10^9\,S^5+1.6*10^{13}\,S^4+3.4*10^{14}\,S^3+1.2*10^{17}\,S^2+1.3*10^{17}\,S+2.8*10^{20})} \quad (5.54.c)$$

$$g_{44}=\frac{\hat{v}_{o1}}{\hat{d}_{o1}}=\frac{-0.05X_8S^9+(149.5X_7-0.35X_8)S^8+(518.1X_7-10.03*10^3X_8)S^7+(1.5*10^7X_7-25*10^3X_8)S^6+(3.32*10^7X_7-3*10^8X_8)S^5+(3.3*10^{11}X_7-43*10^9X_8)S^4+(4.9*10^{11}X_7-3.4*10^{11}X_8)S^3+(2.7*10^{15}X_7-2*10^{12}X_8)S^2+(2.24*10^{15}X_7-1.3*10^{16}X_8)S+75*10^{17}X_7}{L_{o1}C_{o1}(0.09S^{10}+0.65\,S^9+1.6*10^4\,S^8+8.7*10^4\,S^7+8.8*10^8\,S^6+2.8*10^9\,S^5+1.6*10^{13}\,S^4+3.4*10^{14}\,S^3+1.2*10^{17}\,S^2+1.3*10^{17}\,S+2.8*10^{20})} \quad (5.54.d)$$

$$g_{55}=\frac{\hat{v}_{o2}}{\hat{d}_{o2}}=\frac{-0.084X_{10}S^9+(237.5X_9-0.28X_{10})S^8+(883.5X_9-13.2*10^3X_{10})S^7+(30.4*10^6X_9-2.7*10^5X_{10})S^6+(49.4*10^6X_9-4.62*10^8X_{10})S^5+(74.1*10^{10}X_9-4.3*10^8X_{10})S^4+(74.1*10^{10}X_9-5.7*10^{12}X_{10})S^3+(66.5*10^{14}X_9-2.1*10^{12}X_{10})S^2+(3.3*10^{15}X_9-23.8*10^{15}X_{10})S+20*10^{18}X_9}{L_{o2}C_{o2}(0.09S^{10}+0.65\,S^9+1.6*10^4\,S^8+8.7*10^4\,S^7+8.8*10^8\,S^6+2.8*10^9\,S^5+1.6*10^{13}\,S^4+3.4*10^{14}\,S^3+1.2*10^{17}\,S^2+1.3*10^{17}\,S+2.8*10^{20})} \quad (5.54.e)$$

where

$$X_1=L_{i1}I_{Li1},\qquad X_2=C_{i1}V_{ci1}$$

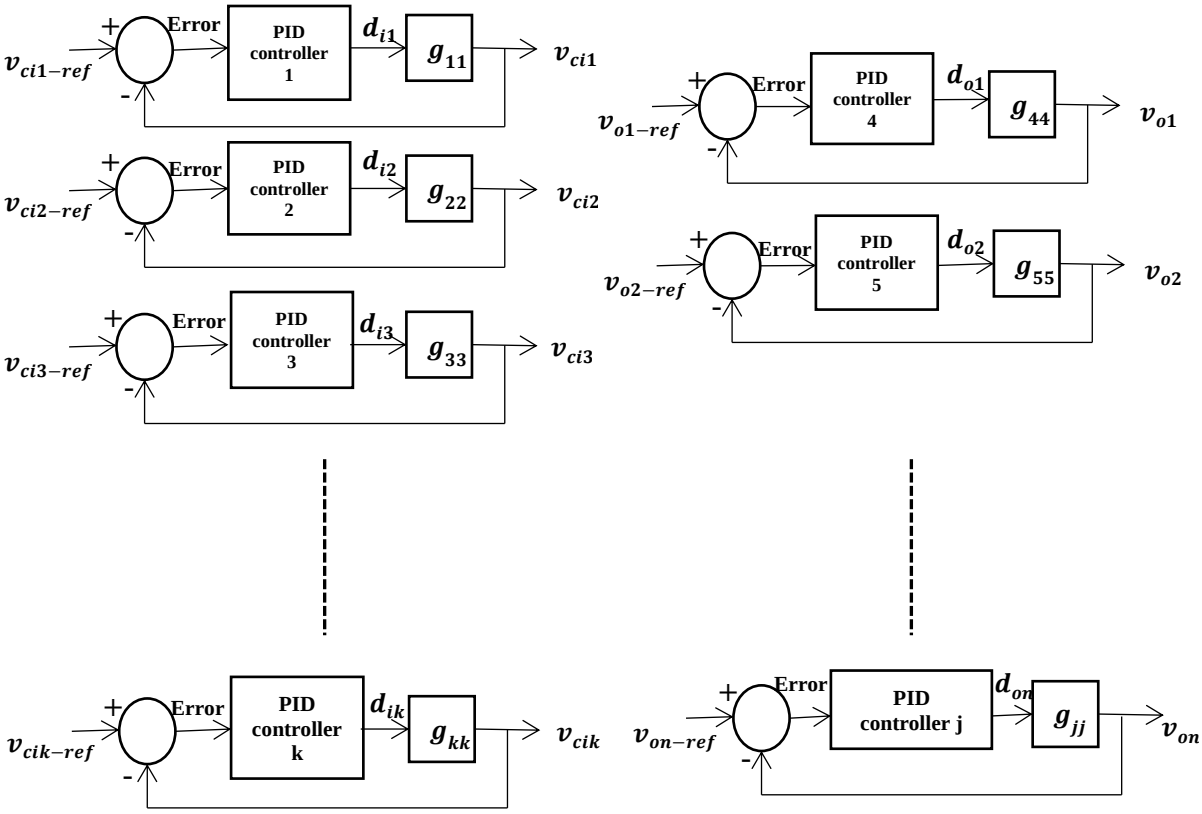
$$X_3=L_{i2}I_{Li2},\qquad X_4=C_{i2}V_{ci2}$$

$$X_5=L_{i3}I_{Li3},\qquad X_6=C_{i3}V_{ci3}$$

$$X_7=C_{o1}V_{co1},\qquad X_8=L_{o1}I_{Lo1}$$

$$X_9=C_{o2}V_{co2},\qquad X_{10}=L_{o2}I_{Lo2}$$

High order transfer functions that are needed for the proposed MIMO DC transformer will further complicate the analysis of the designed controller. Thus, integration of the PID controllers is introduced in order to simplify the controller design as well as possibility to add more inputs\outputs without redesigning the whole control. Figure 5.6 shows the general block diagram of the PID controller integration for the proposed MIMO DC transformer where m is the number of inputs and n is the number of outputs of the proposed DC transformer.



Where $\begin{cases} k = 1,\ 2,\ 3, \ldots,\ m \\ j = m+1,\ m+2,\ \ldots, m+n \end{cases}$

Figure 5.6 the general block diagram of the PID controller integration for the proposed MIMO DC transformer [169].

For the considered example, three-input two-output, integration of five PID controllers (subsystems) is required. Figure 5.7 depicts the designed system control flow chart where each subsystem has two state variables. Then the transfer function of each subsystem has been derived using the averaging method as stated in section 5.3.1 by dividing the system into five subsystems. In this research it is found that the choice of the second order transfer function is adequate for obtaining the pre-defined output voltages. These are as follows:

$$g_{11} = \frac{\hat{v}_{ci1}}{\hat{d}_{i1}} = \frac{V_{i1}}{\left((1 - D_{i1})(1 + \frac{Li1Ci1}{(1-Di1)^2})S^2\right)} \quad (5.55)$$

$$g_{22} = \frac{\hat{v}_{ci2}}{\hat{d}_{i2}} = \frac{V_{i2}}{\left((1 - D_{i2})(1 + \frac{Li2Ci2}{(1-Di2)^2})S^2\right)} \quad (5.56)$$

$$g_{33} = \frac{\hat{v}_{ci3}}{\hat{d}_{i3}} = \frac{V_{i3}}{\left((1 - D_{i3})(1 + \frac{Li3Ci3}{(1-Di3)^2})S^2\right)} \quad (5.57)$$

$$g_{44} = \frac{\hat{v}_{o1}}{\hat{d}_{o1}} = \frac{V_o(1 - \frac{L_{o1}}{(1-D_{o1})^2 R_{L1}}S)}{\left((1 - D_{o1})(1 + \frac{(1-D_{o1})^2 R_{L1}\sqrt{\frac{C_{o1}}{L_{o1}}}}{\sqrt{L_{o1}C_{o1}}})S + \frac{L_{o1}C_{o1}}{(1-D_{o1})^2}S^2\right)} \quad (5.58)$$

$$g_{55} = \frac{\hat{v}_{o2}}{\hat{d}_{o2}} = \frac{V_o(1 - \frac{L_{o2}}{(1-D_{o2})^2 R_{L2}}S)}{\left((1 - D_{o2})(1 + \frac{(1-D_{o2})^2 R_{L2}\sqrt{\frac{C_{o2}}{L_{o2}}}}{\sqrt{L_{o2}C_{o2}}})S + \frac{L_{o2}C_{o2}}{(1-D_{o2})^2}S^2\right)} \quad (5.59)$$

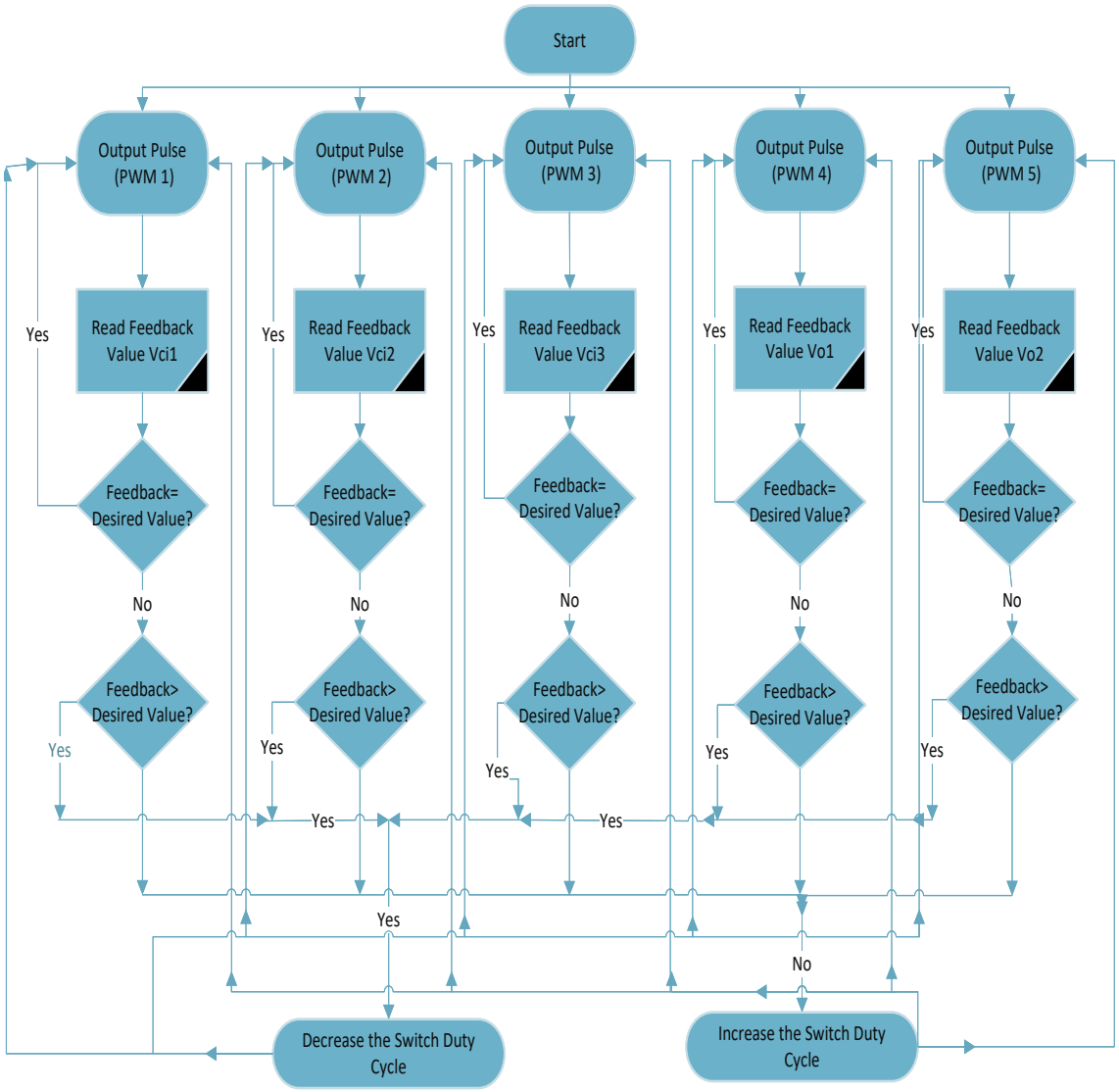


Figure 5.7 The control flow chart of three-input double-output DC transformer design

5.3.3 PID Controllers Tuning Method

Using MATLAB/SIMULINK the Ziegler-Nichols (Z-N) PID tuning method as shown in figure 5.8 can be carried out for each subsystem of the considered example. In this PID tuning method, K_p will be increased until it reaches ultimate gain K_u, at which the output of the control loop has stable oscillation. K_u and the oscillation period T_u are used to set the P, I and D parameters depending on the type of controller is used as illustrated in table 5.1.

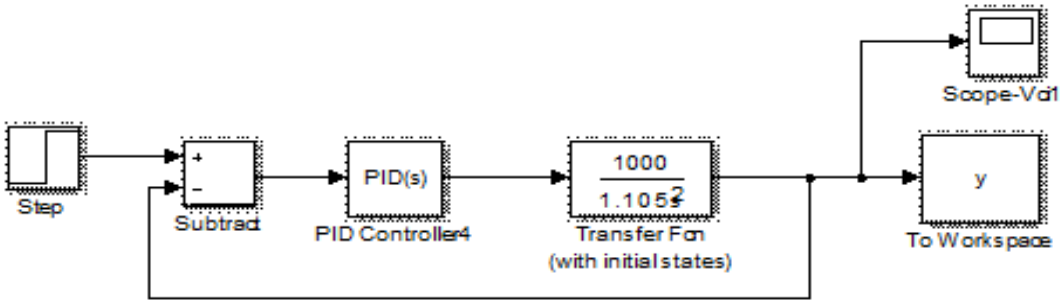


Figure 5.8 SIMULINK block diagram of Z-N method

Table 5.1 Ziegler-Nichols (Z-N) tuning method [138]

Control Type	K_p	K_i	K_d
P	$0.5 * K_u$	-	-
PI	$0.45 * K_u$	$T_u/1.2$	-
PID	$0.6 * K_u$	K_u/ T_i	$K_p * T_d$

Where

$$T_i = 0.5 * T_u$$

$$T_d = 0.125 * T_u$$

For the considered example (three-input two-output) of the proposed DC transformer, the classical Z-N tuning method is used for all its subsystems as shown in figure 5.9. Figure 5.9 also shows the transfer functions of the subsystems. Based on the earlier statement, the PID parameters have been found and listed in table 5.2.

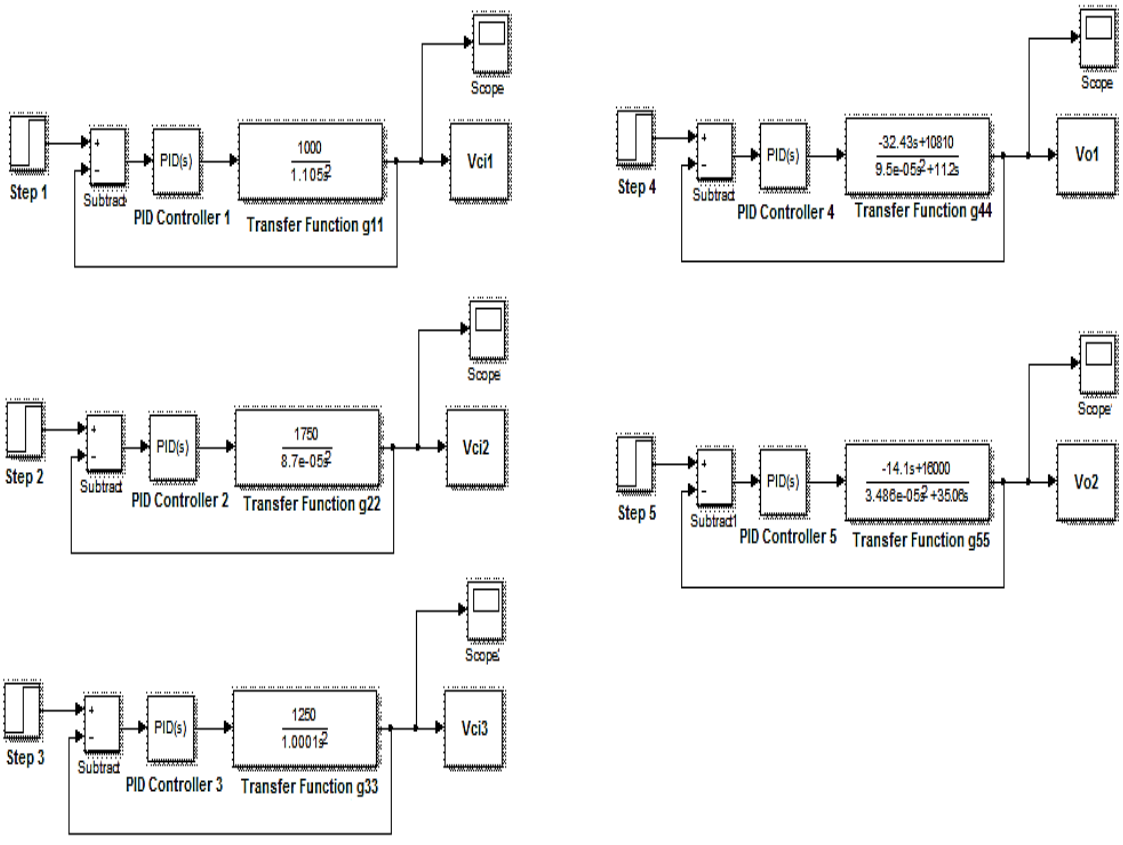


Figure 5.9 the SIMULINK of the subsystems of the proposed three inputs double output DC transformer utilised with PID controllers

Table 5.2 PID controllers' parameters using Ziegler-Nichols tuning method

	K_p	K_i	K_d
PID Controller1	0.7338	0.5769	0.0847
PID Controller2	0.0014	0.0085	5.0271
PID Controller3	0.3530	0.2194	0.1164
PID Controller4	0.1721	0.0963	0.0002
PID Controller5	1.2412	2.5784	0.0004

The three input DC sources for the considered example are chosen to be $V_{i1} = 350\ V$, $V_{i2} = 700\ V$ and $V_{i3} = 500\ V$ to provide a constant DC bus voltage of $V_o = 4\ kV$, and the output voltages of $V_{o1} = 8\ kV$ and $V_{o2} = 11\ kV$.

Then under the above conditions, the considered example is simulated within the MATLAB\SIMULINK platform to show the response of the output voltages when PID controllers are performed in association with Z-N tuning method. The simulation results are shown in figures 5.10 to 5.12.

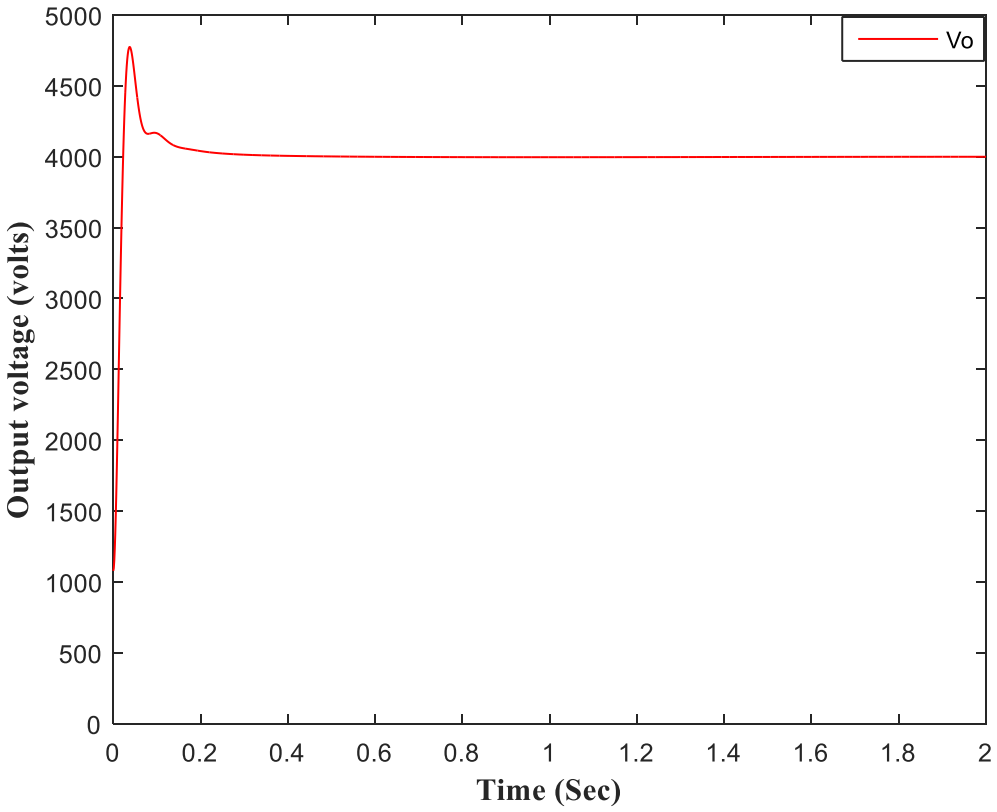


Figure 5.10 the output voltage V_o using Z-N method

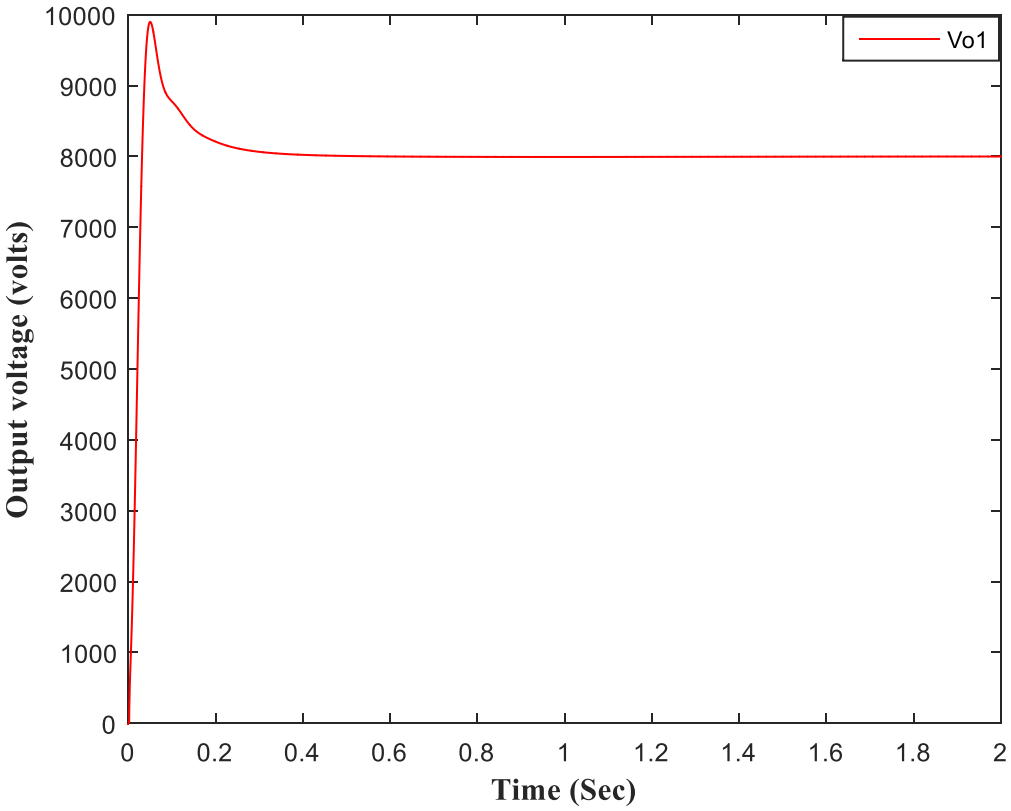


Figure 5.11 the output voltage V_{o1}using Z-N method

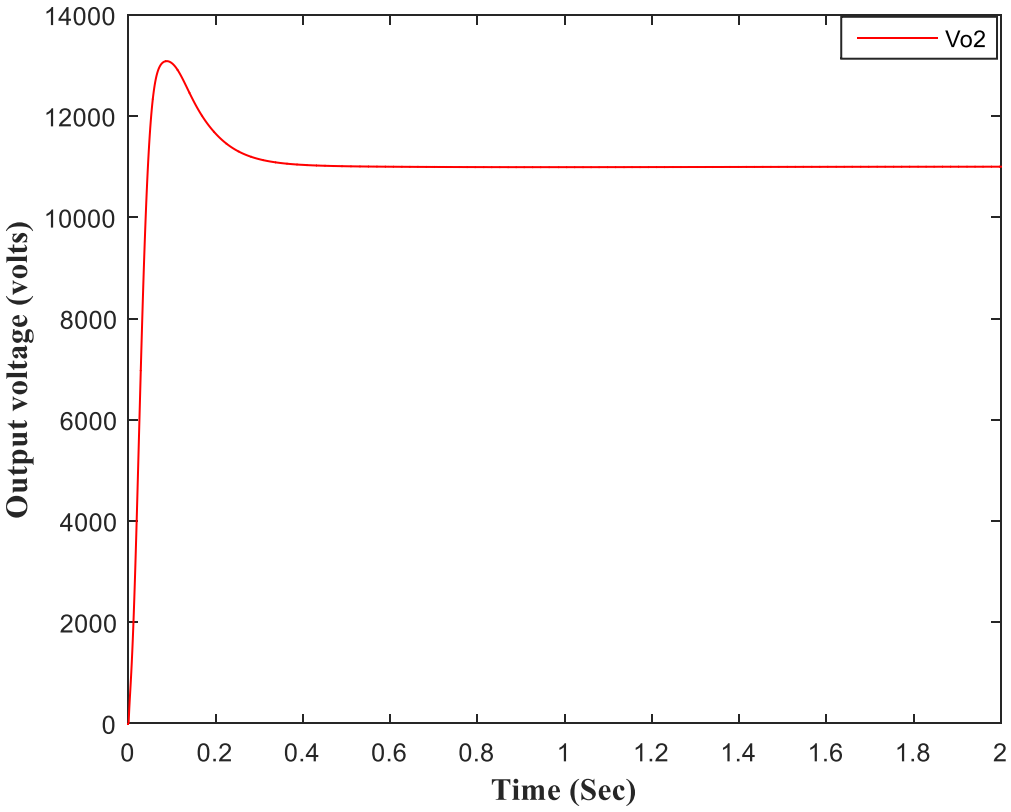


Figure 5.12 the output voltage V_{o2}using Z-N method

Inspection of figures 5.10 to 5.12 suggest that the PID controllers action in conjunction with Z-N tuning method has improved the response of the output curves in terms of reduction in percentage of overshoot and approximately 50% decrease in the rise time of the response curves. Also reduced or eliminated is the steady state error due to the integration component of the PID controllers.

For the purposes of comparison, the above findings are summarised in tabular form. These are shown in table 5.3.

Table 5.3 *Effects of the PID controller action on the time response curve specifications*

The time response curve specifications	Without the PID controllers action	With the PID controllers action
Percentage Overshoot (P.O)	$P.O_{vo1} = 83.9$ % overshooting $P.O_{vo2} = 154.7$ % overshooting	$P.O_{vo1} = 9.3$ % overshooting $P.O_{vo2} = 7.2$ % overshooting
Rise Time (Sec)	$t_{r-vo1} = 0.007$ $t_{r-vo2} = 0.013$	$t_{r-vo1} = 0.004$ $t_{r-vo2} = 0.007$
Settling Time (Sec)	$t_{s-vo1} = 0.43$ $t_{s-vo2} = 0.5$	$t_{s-vo1} = 0.43$ $t_{s-vo2} = 0.46$
Steady State error (%)	$S.S.e_{vo1} = 3.75$ % $S.S.e_{vo2} = 6.36$ %	$S.S.e_{vo1} = 0$ % $S.S.e_{vo2} = 0$ %
Peak-to-Peak ripple voltage (Volts)	$\mathrm{V_{o1}}_{(\mathrm{ripple})(\mathrm{p-p})} = 250$ $\mathrm{V_{o2}}_{(\mathrm{ripple})(\mathrm{p-p})} = 400$	$\mathrm{V_{o1}}_{(\mathrm{ripple})(\mathrm{p-p})} = 40$ $\mathrm{V_{o2}}_{(\mathrm{ripple})(\mathrm{p-p})} = 40$

5.4 Stability analysis of the designed MIMO DC Transformer

The stability analysis of a system is essential, as it provides important relationships or information among process dynamics, controller tuning and desirable performance [141]. The analysis method of the linear or linearized systems could be carried out with the knowledge of the models transfer function. This will result in determining the stability of the controller design and selection of tuning constant values [141].

As the proposed transformer is composed of a number of series (on the input side) and parallel (on the output side) connected modules (known as subsystems), hence the stability analysis should be carried out for each module. The system or plant will be stable if all subsystems are stable and similarly if any subsystem is unstable this will lead to instability of the whole system [142].

In this research, stability analysis of the proposed MIMO DC transformer will be done based on the phase and gain margins magnitude information which are obtained from the bode plots of each subsystem's transfer function using the control toolbox of MATLAB\SIMULINK. The transfer functions are derived via mathematical modelling of DC transformer as presented previously in section 5.3.1.

However, in order to distinguish between the stability and the transient behaviour of a system or plant, a stability rule for PID controller tuning is devised using Routh-Hurwitz stability criterion. This stability rule or criteria is defined from the characteristic graphs of bode plot or the pole-zero map. The effectiveness of this approach is examined via simulations under different scenarios or cases.

5.4.1 Dependency of Stability on PID Gain Selection

A Routh-Hurwitz criterion is an important criterion that gives necessary and sufficient stability conditions for all of the roots of the characteristic polynomial to lie in the Left Half of the complex S-Plane (LHP) [143]. As the locations of the poles and the values of the real and imaginary parts of the pole determine the response of the system and also weather the system is stable or not. It has been reported in [144] that when the poles of closed loop transfer function of a specific system are in the Right Half of the S-Plane (RHP), the system becomes unstable. This is illustrated graphically in figure 5.13.

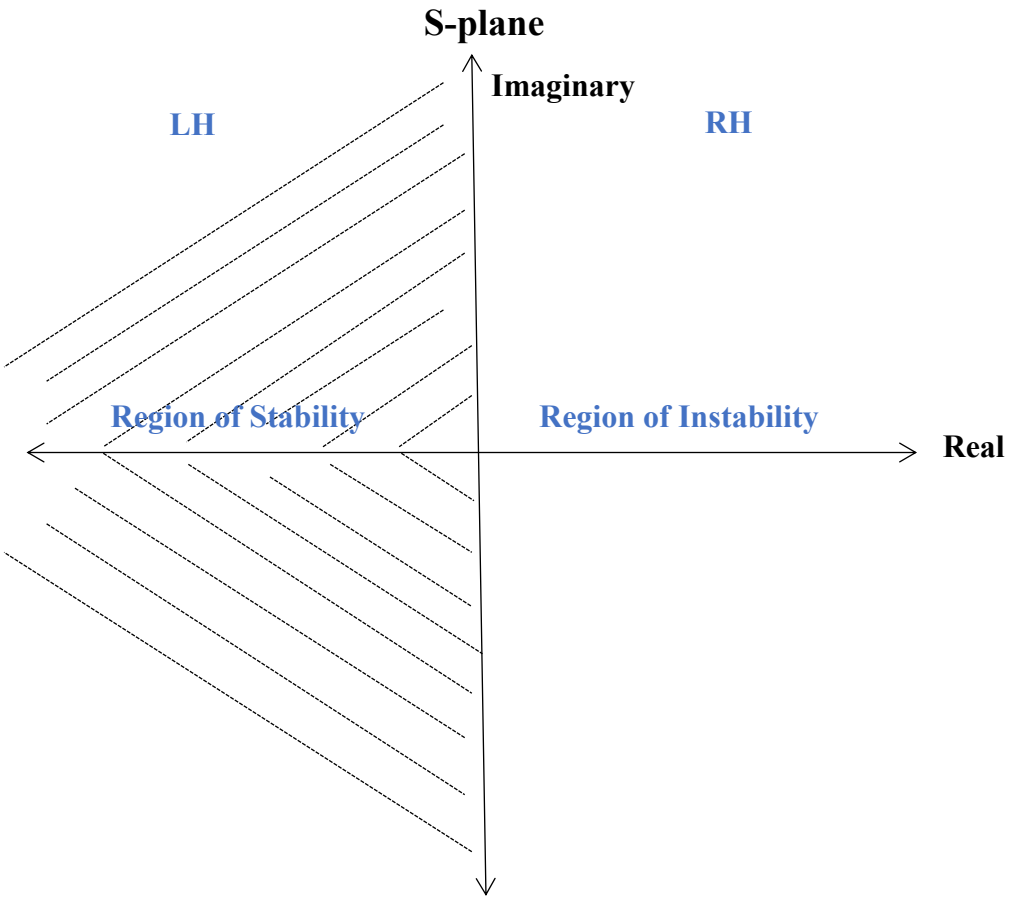


Figure 5.13 S-plane and region of stability [145]

Based on the above information, in order to find the stability conditions of the proposed MIMO DC transformer the characteristic equation of the closed loop transfer function is needed for each subsystem module. Figure 5.14 shows the closed loop control structure of each module of the proposed DC transformer.

It is clear that the relation between the error from the output without variation and the PID gain with disturbance will affect the system's stability, thus the stability conditions of each module are presented in this section in order to guarantee the system's stability.

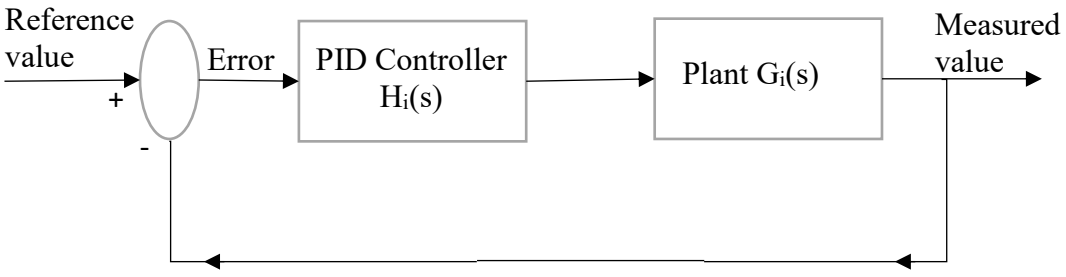


Figure 5.14 Closed loop control structure [136]

For the system without any disturbances, the PID control must operate with stability. The gains of PID control should be designed for Q_i to be positive real, that is all elements of the

first column of the Routh Array of Q_i are positive [146]. Where Q_i is the closed loop transfer function of each subsystem as follows:

$$Q_i(s) = \frac{H_i(s)G_i(s)}{1 + H_i(s)G_i(s)} \tag{5.60}$$

where

$$H_i(s) = \frac{k_P S + k_I + k_D S^2}{S} \tag{5.61}$$

$$G_i(s) = \frac{V_i}{(1 - D_i)(1 + \frac{L_i C_i}{(1 - D_i)^2})S^2} \tag{5.62}$$

$Q_i(s)$ is the closed loop transfer function.

$H_i(s)$ is the PID controller transfer function.

$G_i(s)$ is the plant transfer function in the input side of the proposed DC transformer.

The poles and zeros of the closed loop transfer function are the values of S which the denominator $(1 + H_i(s)G_i(s))$ and the numerator $(H_i(s)G_i(s))$ of the closed loop transfer function becomes zero respectively.

As the Routh-Hurwitz stability criterion has been used to determine the stability conditions of the proposed system. The characteristic equation of Q_i is essential in order to build the Routh Array which will define the system's stability [143].

The characteristic equation of Q_i become as follows

$$\Lambda_i(s) = 1 + H_i(s)G_i(s) \tag{5.63}$$

$$\Lambda_i(s) = (\frac{L_i C_i}{(1 - D_i)^2})S^3 + (V_{ref-i}k_D)S^2 + \left(1 + V_{ref-i}k_P\right)S + V_{ref-i}k_I \tag{5.64}$$

$$(i = 1, \ldots., m)$$

$\Lambda_i(s)$ is the characteristic equation of Q_i.

m represents the number of inputs of the proposed DC transformer.

The general Routh Array of the input side of the considered example with three inputs double output of the proposed DC transformer will be as follows:

$$\begin{array}{lcc} S^3 & \frac{L_i C_i}{(1-D_i)^2} & (1+V_{ref-i}k_P) \\ S^2 & (V_{ref-i}k_D) & V_{ref-i}k_I \\ S^1 & (1+V_{ref-i}k_P - \frac{L_i C_i}{(1-D_i)^2}\frac{k_I}{k_D}) & 0 \\ S^0 & V_{ref-i}k_I & 0 \end{array} \quad (5.65)$$

All coefficients of the first column in the Routh Array being positive are necessary for all roots to be located in the LHP in order to guarantee the system's stability. Thus, the PID gains should meet these conditions as a stable design rule:

$$\left.\begin{array}{c} k_D > 0 \\ \frac{k_I}{k_D} < \frac{(1+V_{ref-i}k_P)(1-D_i)^2}{L_i C_i} \\ k_I > 0 \end{array}\right\} for\ Q_i\ (i = 1, \dots, m) \quad (5.66)$$

As the system of considered example has three inputs $m = 3$ and two outputs $n = 2$ then the stability analysis should be examined over the transfer function of each subsystem (module). Thus, for the input side $\{Q_1, Q_2, Q_3\}$ are presented to determine the stability conditions as follows

Routh Array of Q_1

$$\begin{array}{lcc} S^3 & 1.105 & 10^3 * k_P \\ S^2 & 10^3 * k_D & 10^3 * k_I \\ S^1 & 10^3 * k_P - \frac{1.105 * k_I}{k_D} & 0 \\ S^0 & 10^3 * k_I & 0 \end{array} \quad (5.67)$$

Then the stability condition of PID_1

$$\left.\begin{array}{c} k_D > 0 \\ k_P > 1.105 * 10^{-3}\ \frac{k_I}{k_D} \\ k_I > 0 \end{array}\right\} for\ Q_1 \quad (5.68)$$

Routh Array of Q_2

$$\begin{array}{lcc} S^3 & 8.7 * 10^{-5} & 1750 * k_P \\ S^2 & 1750 * k_D & 1750 * k_I \\ S^1 & 1750 * k_P - \frac{0.000087 * k_I}{k_D} & 0 \\ S^0 & 1750 * k_I & 0 \end{array} \quad (5.69)$$

Then the stability condition of PID_2

$$\left.\begin{array}{c} k_D > 0 \\ k_P > 4.97 * 10^{-8}\ \dfrac{k_I}{k_D} \\ k_I > 0 \end{array}\right\} for\ Q_2 \tag{5.70}$$

Routh Array of Q_3

$$\begin{array}{lcc} S^3 & 1.0001 & 1250 * k_P \\ S^2 & 1250 * k_D & 1250 * k_I \\ S^1 & 1250 * k_P - \dfrac{1.0001 * k_I}{k_D} & 0 \\ S^0 & 1250 * k_I & 0 \end{array} \tag{5.71}$$

Then the stability condition of PID_3

$$\left.\begin{array}{c} k_D > 0 \\ k_P > 0.0008\ \dfrac{k_I}{k_D} \\ k_I > 0 \end{array}\right\} for\ Q_3 \tag{5.72}$$

The characteristic equation of the closed loop transfer function on the output side Q_{oj} where $(j = 1, \dots, n)$ and n is the number of outputs of the proposed DC transformer become as follows

$$\Lambda_{oj}(s) = 1 + H_{oj}(s)G_{oj}(s) \tag{5.73}$$

$$H_{oj}(s) = \frac{k_P S + k_I + k_D S^2}{S} \tag{5.74}$$

$$G_{oj}(s) = \frac{V_O\left(1 - \frac{L_{oj}}{(1-D_{oj})^2 R_{Lj}} S\right)}{\left((1 - D_{oj})\left(1 + \frac{(1-D_{oj})^2 R_{Lj}\sqrt{\frac{C_{oj}}{L_{oj}}}}{\sqrt{L_{oj}C_{oj}}}\right) S + \frac{L_{oj}C_{oj}}{(1-D_{oj})^2} S^2\right)} \tag{5.75}$$

After substitution the general characteristic equations will be

$$\begin{aligned}\Lambda(\mathrm{s})_{oj} = &\left(\frac{L_{oj}C_{oj}}{\left(1-D_{oj}\right)^2}-\frac{V_{ref-j}L_{oj}k_D}{\left(1-D_{oj}\right)^2R_{Lj}}\right)S^3 \ldots\\ &+\left(1+\frac{\left(1-D_{oj}\right)^2R_{Lj}\sqrt{\frac{C_{oj}}{L_{oj}}}}{\sqrt{L_{oj}C_{oj}}} \ldots\right.\\ &\left.-\frac{V_{ref-j}L_{oj}k_P}{\left(1-D_{oj}\right)^2R_{Lj}}+V_{ref-j}k_D\right)S^2 \ldots\\ &+\left(V_{ref-j}k_P-\frac{V_{ref-j}L_{oj}k_I}{\left(1-D_{oj}\right)^2R_{Lj}}\right)S+\ V_{ref-j}k_I\end{aligned} \tag{5.76}$$

The general Routh Array of the output side of the proposed DC transformer will be as follows:

$$\begin{array}{lcc} S^3 & \frac{L_{oj}C_{oj}}{\left(1-D_{oj}\right)^2} & V_{ref-j}k_P-\frac{V_{ref-j}L_{oj}k_I}{\left(1-D_{oj}\right)^2R_{Lj}} \\ S^2 & 1+\frac{\left(1-D_{oj}\right)^2R_{Lj}\sqrt{\frac{C_{oj}}{L_{oj}}}}{\sqrt{L_{oj}C_{oj}}}-\frac{V_{ref-j}L_{oj}k_P}{\left(1-D_{oj}\right)^2R_{Lj}}+V_{ref-j}k_D & V_{ref-j}k_I \\ S^1 & a & 0 \\ S^0 & V_{ref-j}k_I & 0 \end{array} \tag{5.77}$$

And

$$\mathrm{a} = V_{ref-j}k_P-\frac{V_{ref-j}L_{oj}k_I}{\left(1-D_{oj}\right)^2R_{Lj}}-\frac{V_{ref-j}L_{oj}C_{oj}R_{Lj}k_I+{V_{ref-j}}^2L_{oj}k_Ik_D}{\left(1-D_{oj}\right)^2R_{Lj}\left(1+\frac{\left(1-D_{oj}\right)^2R_{Lj}\sqrt{\frac{C_{oj}}{L_{oj}}}}{\sqrt{L_{oj}C_{oj}}}-\frac{V_{ref-j}L_{oj}k_P}{\left(1-D_{oj}\right)^2R_{Lj}}+V_{ref-j}k_D\right)} \tag{5.78}$$

All coefficient of the first column of the Routh Array should be positive to ensure the system's stability. In the output side of the considered example there are two outputs with two PID controllers to control the voltages so, the characteristic equations and the Routh array of Q_{o1}, Q_{o2} will be:

$$\Lambda(s)_{o1} = (0.0091 * 10^{-3} - 2.91\,k_D)\,S^3 + (3.76 + 8000\,k_D - 2.91\,k_P)S^2 \ldots + (8000\,k_P - 2.91\,k_I)\,S + 8000\,k_I \tag{5.79}$$

Routh Array of Q_{o1}

$$\begin{array}{lcc} S^3 & 0.0091 * 10^{-3} - 2.91\,k_D & 8000\,k_P - 2.91\,k_I \\ S^2 & 3.76 + 8000\,k_D - 2.91\,k_P & 8000\,k_I \\ S^1 & 8000\,k_P - 2.91\,k_I - \dfrac{0.0728 * k_I - 23.28 * 10^3 k_D\,k_I}{3.76 + 8000\,k_D - 2.91\,k_P} & 0 \\ S^0 & 8000 * k_I & 0 \end{array} \tag{5.80}$$

Then the stability condition of PID_{o1}

$$\left.\begin{array}{c} k_D < 0.0031 * 10^{-3} \\ k_P < 2.75 * 10^3\,k_D + 1.29 \\ k_I < 2.75 * 10^3\,k_P - \dfrac{0.0728\,k_I - 23.28 * 10^3 k_D\,k_I}{10.9 + 23.28 * 10^3\,k_D - 8.46\,k_P} \\ k_I > 0 \end{array}\right\} for\ Q_{O1} \tag{5.81}$$

And for the second output the characteristic equation will be

$$\Lambda(s)_{o2} = (97.05 * 10^{-6} - 24.76\,k_D)\,S^3 \ldots + (325.8 + 11000\,k_D - 24.76\,k_P)S^2 \ldots + (11000\,k_P - 24.76\,k_I)\,S + 11000\,k_I \tag{5.82}$$

Routh Array of Q_{o2}

$$\begin{array}{lcc} S^3 & 97.05 * 10^{-6} - 24.76\,k_D & 11000\,k_P - 24.76\,k_I \\ S^2 & 325.8 + 11000\,k_D - 24.76\,k_P & 11000\,k_I \\ S^1 & 11000\,k_P - 24.76\,k_I - \dfrac{1.06 * k_I - 272.36 * 10^3 k_D\,k_I}{325.8 + 11000\,k_D - 24.76\,k_P} & 0 \\ S^0 & 11000 * k_I & 0 \end{array} \tag{5.83}$$

Then the stability condition of PID_{o2}

$$\left.\begin{array}{c} k_D < 0.0039 * 10^{-3} \\ k_P < 444.3\,k_D + 13.16 \\ k_I < 444.3\,k_P - \dfrac{1.06\,k_I - 272.36 * 10^3 k_D\,k_I}{8066.8 + 272.36 * 10^3\,k_D - 613.05\,k_P} \\ k_I > 0 \end{array}\right\} for\ Q_{O2} \tag{5.84}$$

To examine the effectiveness of the PID gain selection rule that is suggested above for guaranteeing the stability of the system or the plant, simulations within

MATLAB\SIMULINK environment is performed under two cases or scenarios namely without disturbances and with disturbance in the system or the plant.

1) Case 1: stability analysis using bode plot concept of the proposed DC transformer without disturbance

In this case the PID controller gains have been selected taking the previous design conditions into account during the tuning method for each module or subsystem under normal condition i.e. without any disturbances or variation in the system. The bode plot is presented using the control toolbox of MATLAB\SIMULINK to define the stability of each subsystem depending on the gain and phase margin values. Where the bode plot is a graph of the frequency response of a system which is a combination of a magnitude plot and a phase plot. Both quantities are plotted against low to high frequency range [147]. From the plot it could be directly comment on the stability of a system or a plant without any calculations, as it provides a relative stability in terms of the gain and phase margin values [147].

Figure 5.15 depicts the definition of the gain and phase margin of the bode plots in order to define the stability of a closed loop system.

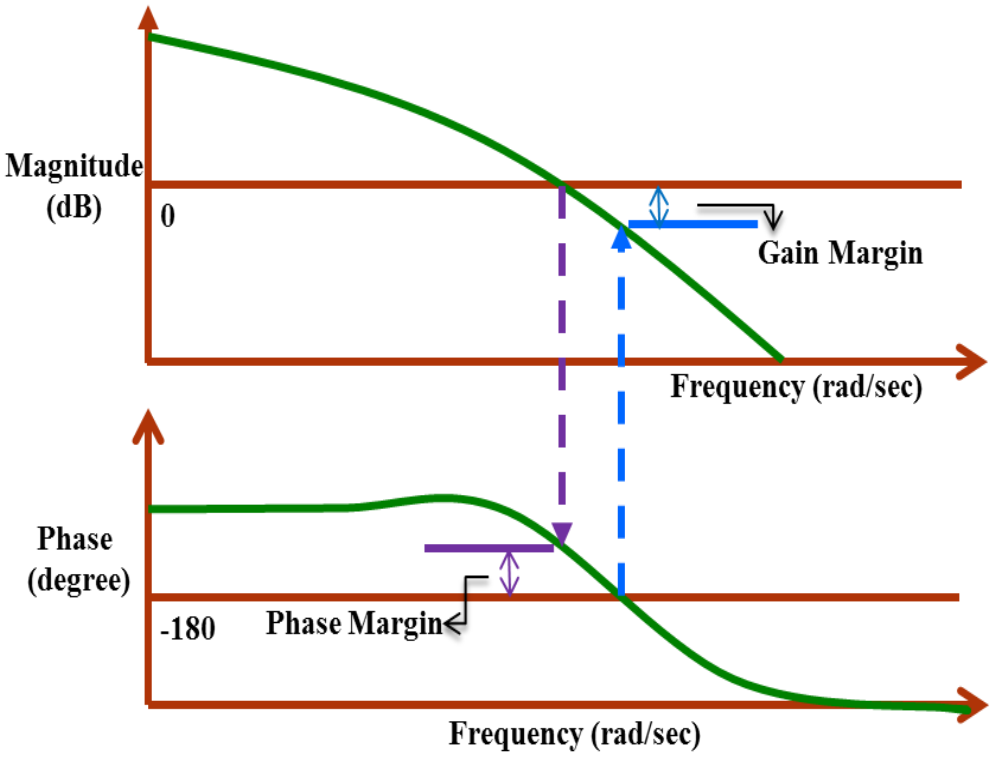


Figure 5.15 Gain and Phase margin definition of the bode plots [148]

Stability criteria of bode plots are defined in [147] as:

- The system is stable if both gain and phase margin are positive, or the phase margin is greater than the gain margin.
- The system is unstable if both gain and phase margin are negative, or the phase margin is less than the gain margin.
- The system is marginally stable (oscillation on the time response curve as no steady state value) if both gain and phase margin equal to zero or if the phase and gain margin have the same value.

The stability of the considered example of the proposed DC transformer (three-input two-output) is studied using the concept above. This is achieved by investigating the stability of each subsystem through their respective transfer functions under the stable PID gain selection rules or stable design rule.

Table 5.4 represents the stability conditions of PID_1 gain selection for $subsystem_1$ and the selected gain.

Table 5.4 The stability condition of PID_1 gains

Condition (stable design rule) Q_1	Gain selection
$k_P > 0.012$	$k_P = 0.733$
$k_I > 0$	$k_I = 0.576$
$k_D > 0$	$k_D = 0.05$

Figure 5.16 shows the bode plot of gain and phase margins of the 1st subsystem for stability verification of the closed loop control.

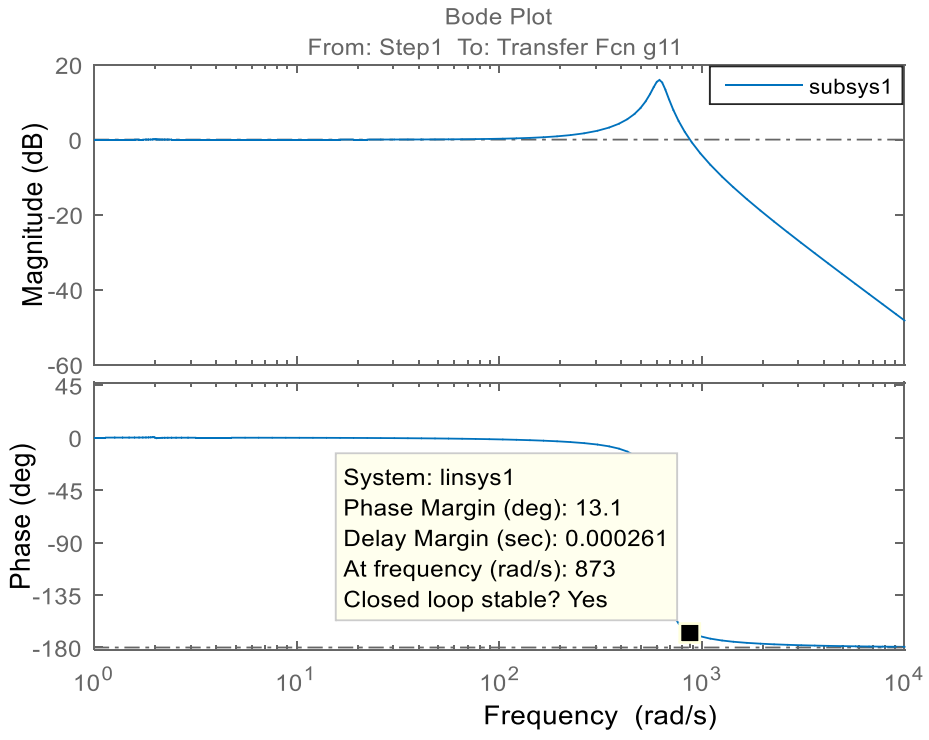


Figure 5.16 the bode plot (gain and phase) margins of the1st subsystem

Table 5.5 represents the stability conditions of PID_2 gain selection for $subsystem_2$ and the selected gain.

Table 5.5 The stability condition of PID_2 gains

Condition (stable design rule) Q_2	Gain selection
$k_P > 0.019 * 10^{-5}$	$k_P = 0.1325$
$k_I > 0$	$k_I = 17.07$
$k_D > 0$	$k_D = 4.26$

Figure 5.17 shows the bode plot of gain and phase margins of the 2nd subsystem for stability verification of the closed loop control.

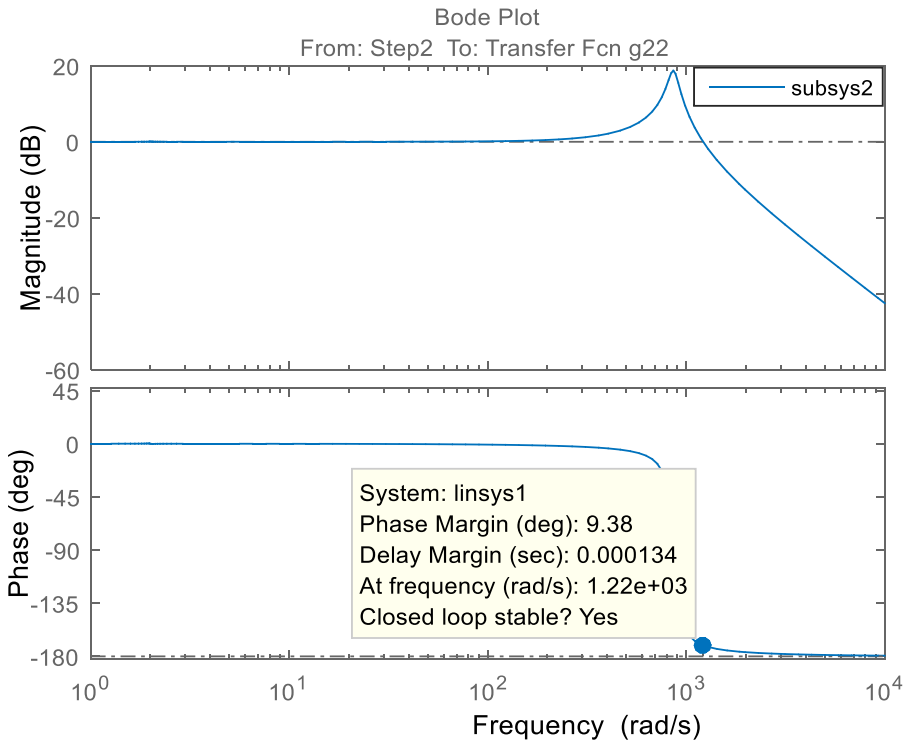


Figure 5.17 the bode plot (gain and phase) margins of the2nd subsystem

Table 5.6 represents the stability conditions of PID_3 gain selection for $subsystem_3$ and the selected gain.

Table 5.6 The stability condition of PID_3 gains

Condition (stable design rule) Q_3	Gain selection
$k_P > 0.003$	$k_P = 0.353$
$k_I > 0$	$k_I = 0.219$
$k_D > 0$	$k_D = 0.05$

Figure 5.18 shows the bode plot of gain and phase margins of the 3rd subsystem for stability verification of the closed loop control.

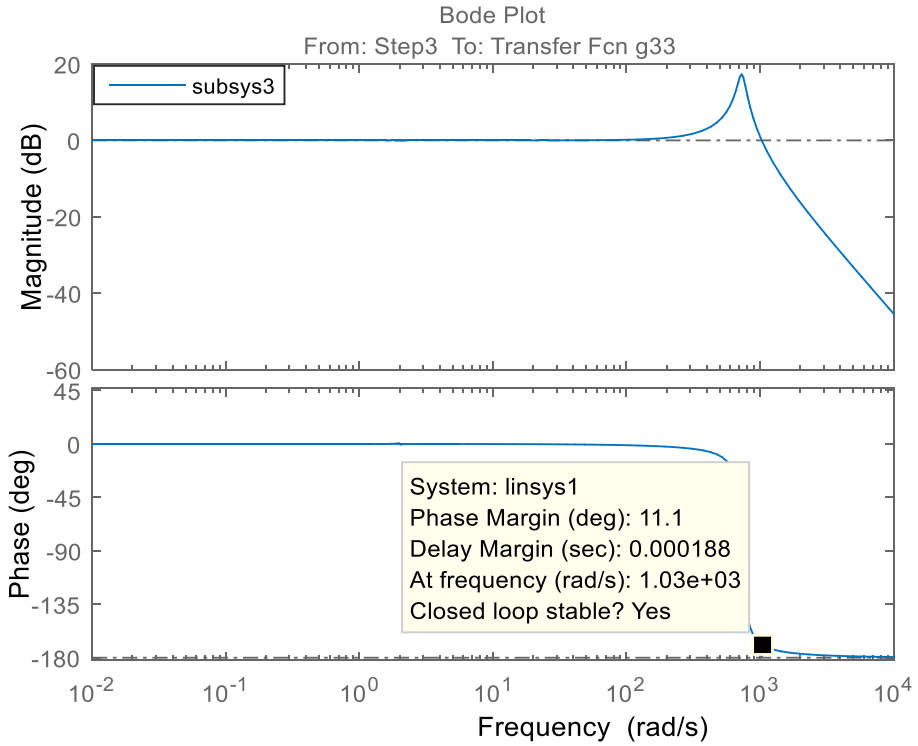


Figure 5.18 the bode plot (gain and phase) margins of the3rd subsystem

Table 5.7 represents the stability conditions of PID_{o1} gain selection for subsystem4 (1st output) and the selected gain.

Table 5.7 The stability condition of PID_{o1} gains

Condition (stable design rule) Q_{o1}	Gain selection
$\boldsymbol{k_P < 1.295}$	$k_P = 0.172$
$\boldsymbol{k_I < 472}$	$k_I = 0.096$
$\boldsymbol{k_D < 3.1 * 10^{-6}}$	$k_D = 2 * 10^{-6}$

Figure 5.19 shows the bode plot of gain and phase margins of the 4th subsystem for stability verification of the closed loop control.

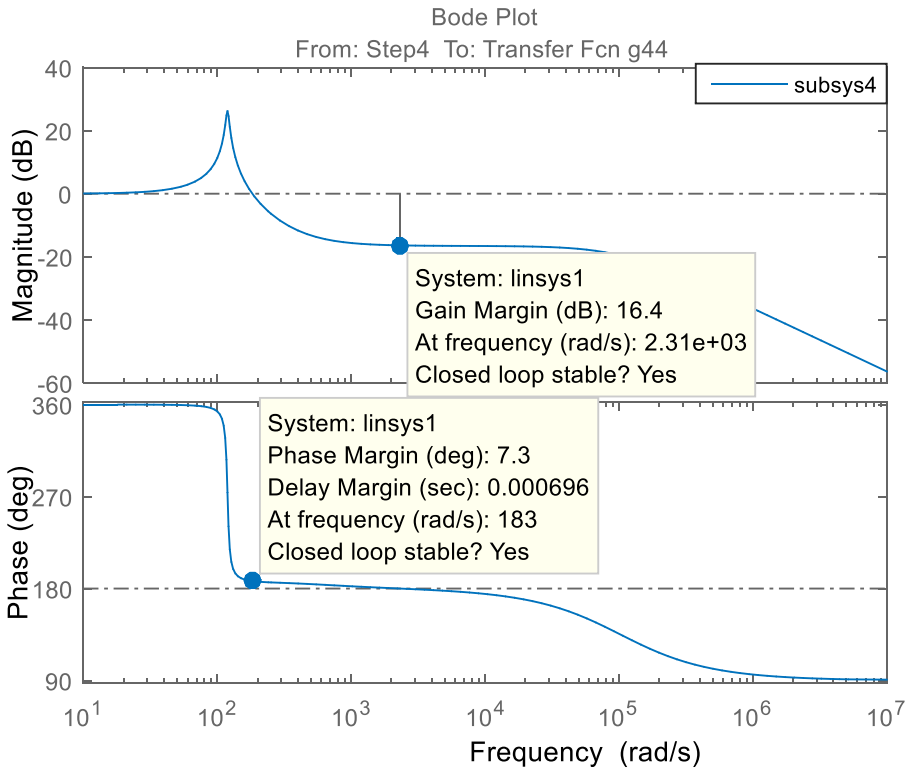


Figure 5.19 the bode plot (gain and phase) margins of the4th subsystem

Table 5.8 represents the stability conditions of PID_{o2} gain selection for $subsystem_5$ (2nd output) and the selected gain.

Table 5.8 The stability condition of PID_{o2} gains

Condition (stable design rule) Q_{o2}	Gain selection
$\boldsymbol{k_P < 13.16}$	$k_P = 0.0447$
$\boldsymbol{k_I < 19.8}$	$k_I = 12.837$
$\boldsymbol{k_D < 3.9 * 10^{-6}}$	$k_D = 0$

Figure 5.20 shows the bode plot of gain and phase margins of the 5th subsystem for stability verification of the closed loop control.

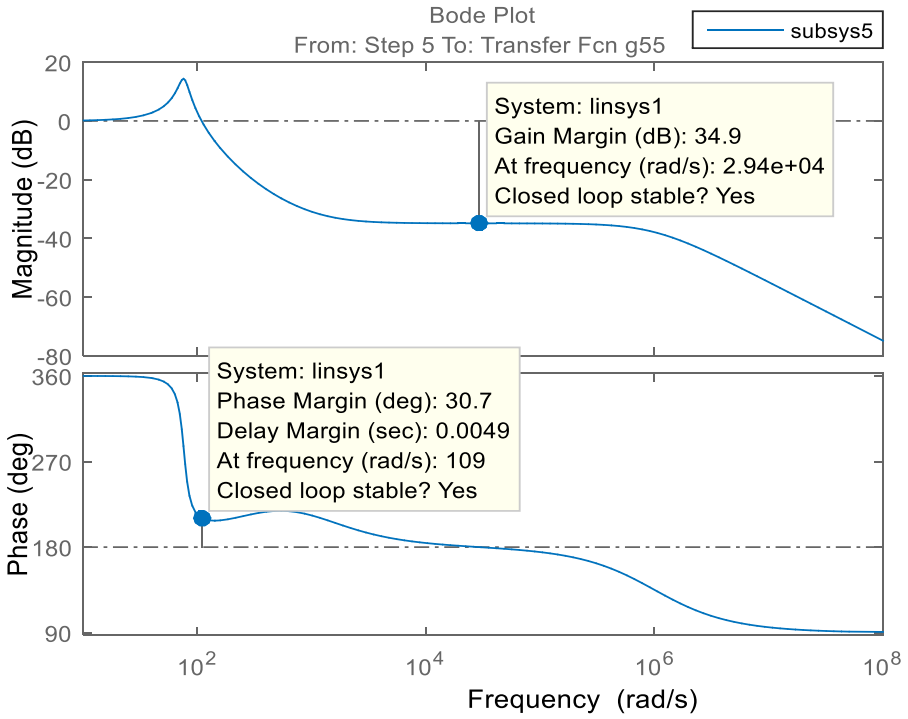


Figure 5.20 the bode plot (gain and phase) margins of the5th subsystem

In the bode plots of the input side of the considered example (three-input two-output) of the proposed DC transformer it is clear that the phase margin is positive, and the gain margin is infinity. As the phase plot never crosses the -180° line, thus the system is inherently stable as the system could operate at any gain without losing stability [149]. While the bode plots of the output side subsystems provide the values of both gain and phase margin with positive values which are sufficient to indicate that the subsystems are stable.

As the result, one with confident could state that the considered example (three-input two-output) of the proposed DC transformer is stable, as the whole subsystems with the stable PID gain selection rule are stable.

2) Case 2: stability analysis using S-plane concept (pole-zero map) of the proposed DC transformer with disturbance

The value of the error due to disturbance will have effect on the PID gain selection. Therefor to guarantee the system's stability under any disturbances, the stable design rule should be considered in conjunction with the tuning the PID for better performance with zero error.

To demonstrate the concept, the stability of the considered example (three-input two-output) is tested with two different percentages of error following the pole/zero map discussed earlier (S-plane concept). The percentage of the error is defined as:

$$\%Error = \frac{Actual\ value - Available\ value}{Actual} * 100\%$$

A. Case 1: Error 14% V_{ci1} due to disturbance in the first input voltage source

For demonstration purposes only results from the 1st subsystem will be shown in this section. Table 5.9 shows the stability condition that is required for the PID gain of subsystem$_1$ i.e. zero error and no overshoot.

Table 5.9 The stability condition of PID$_1$ gains (zero error and no overshoot)

Condition (stability rule with zero error) Q_1	**Gain selection**	**Pole/zero analysis**
$\boldsymbol{k_P > 0.012 \& k_P > 0.733}$	$k_P = 0.8$	$s_{z1} = -1.56$
$\boldsymbol{k_I > 0}$ & $\boldsymbol{k_I > 0.576}$	$k_I = 1$	$s_{z2} = -5.94$
$\boldsymbol{k_D > 0}$ & $\boldsymbol{k_D > 0.05}$	$k_D = 0.1$	$s_{p1} = -6.58$
		$s_{p2} = -45.9 + 73.8\,i$
		$s_{p3} = -45.9 - 73.8\,i$

Where s_z , s_p are the zeros and poles respectively of the closed loop transfer function Q_1.

Figure 5.21 shows the pole-zero map of Q_1. Which reveals the location of the zeros and poles on the LHP means that the first subsystem is stable.

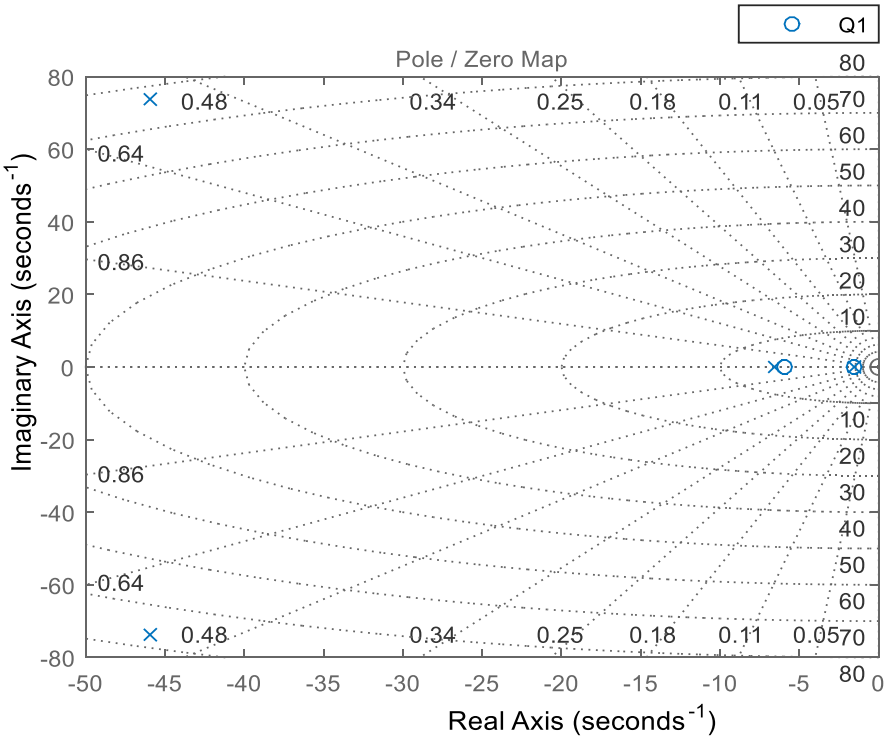


Figure 5.21 the pole-zero map of subsystem Q_1

B. Case 2: Error 40% V_{ci3} due to disturbance in the third input voltage source

For demonstration purposes only results from the 3rd subsystem will be shown in this section. Table 5.10 shows the stability condition that is required for the PID gain of subsystem$_3$ i.e. zero error and no overshoot.

Table 5.10 The stability condition of PID$_3$ gains (zero error and no overshoot)

Condition (stability rule with zero error) Q_3	Gain selection	Pole/zero analysis
$k_P > 0.003$ & $k_P > 0.353$	$k_P = 0.4$	$s_{z1} = -1.97 + 2.39\,i$
$k_I > 0$ & $k_I > 0.219$	$k_I = 1$	$s_{z2} = -1.97 - 2.39\,i$
$k_D > 0$ & $k_D > 0.05$	$k_D = 0.1$	$s_{p1} = -48 + 71.4\,i$
		$s_{p2} = -48 - 71.4\,i$

Where s_z , s_p are the zeros and poles respectively of the closed loop transfer function Q_3.

Figure 5.22 shows the pole-zero map of Q_3. Which reveals the location of the zeros and poles on the LHP means that the third subsystem is stable.

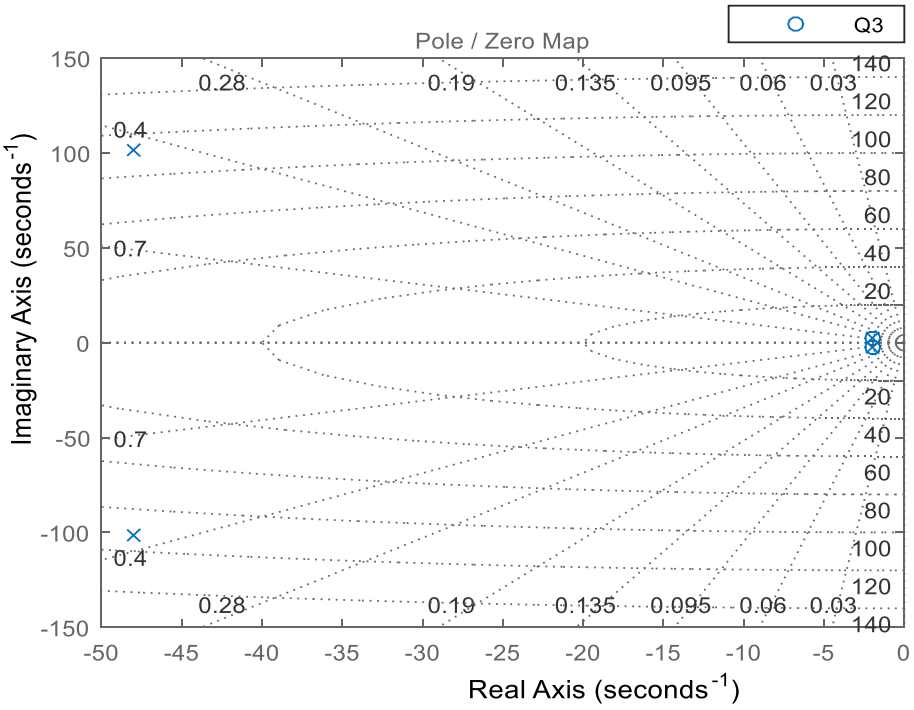


Figure 5.22 the pole-zero map of subsystem Q_3

It can be noticed from the pole-zero analysis that the PID gains design rule is useful to guarantee the system's stability as the poles and zeros lies on the Left Half side of the S-Plane (LHP). In this case the output response curve is shown in figure 5.23, which has a good performance with a steady state value of 8 kV.

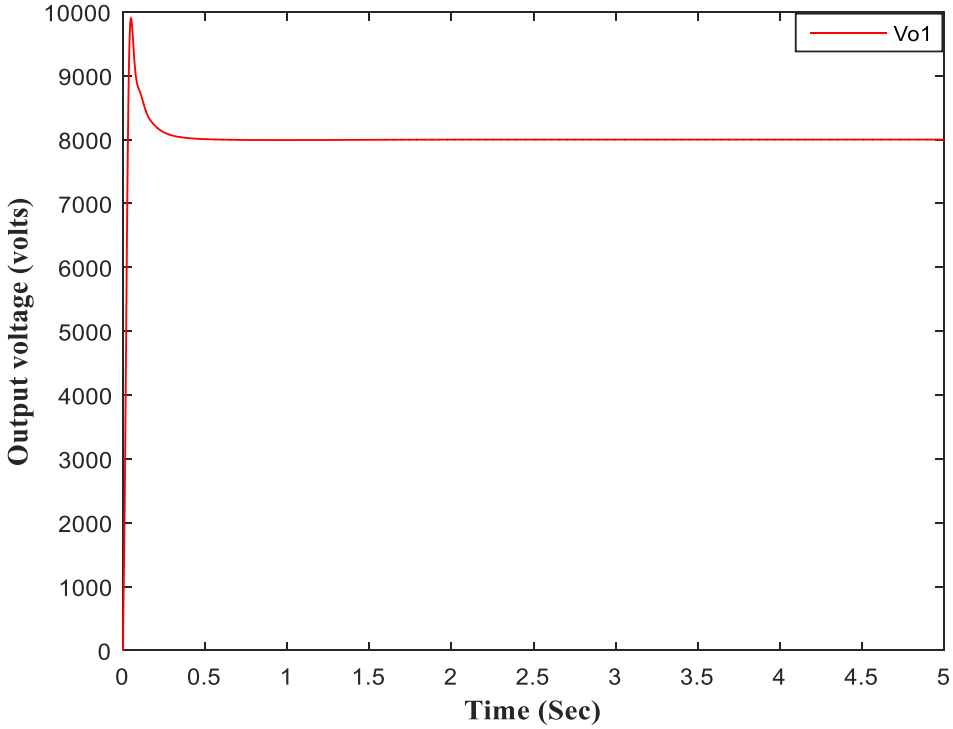


Figure 5.23 the output response curve V_{o1} of the considered example of the proposed DC transformer with stable subsystems

In the same case for subsystem$_3$, if the gain selected in such a way that the stable rule design not being considered as presented in table 5.11. The corresponding pole-zero map is shown in the S-plane of figure 5.24 where one zero lies on its RHP. This leads to have instability as can be seen in the response curve of V_{ci3} in figure 5.25. This instability also will have a knocking effect on the stability of whole system and hence the output voltage. Figure 5.26 exhibits this knocking effect on V_{o1} where its response curve goes to zero as the time increases which means unstable system.

Table 5.11 The stability condition of PID$_3$ gains (zero error and no overshoot)

Condition (stability rule with zero error) Q_3	**Gain selection**	**Pole/zero analysis**
$\boldsymbol{k_P > 0.003}$ & $\boldsymbol{k_P > 0.353}$	$k_P = 0.4$	$s_{z1} = 1.75$
$\boldsymbol{k_I > 0}$ & $\boldsymbol{k_I > 0.219}$	$k_I = -1$	$s_{z2} = -5.5$
$\boldsymbol{k_D > 0}$ & $\boldsymbol{k_D > 0.05}$	$k_D = 0.1$	$s_{p1} = -5.81$
		$s_{p2} = -48 - 71.5\,i$
		$s_{p3} = -48 + 71.5\,i$

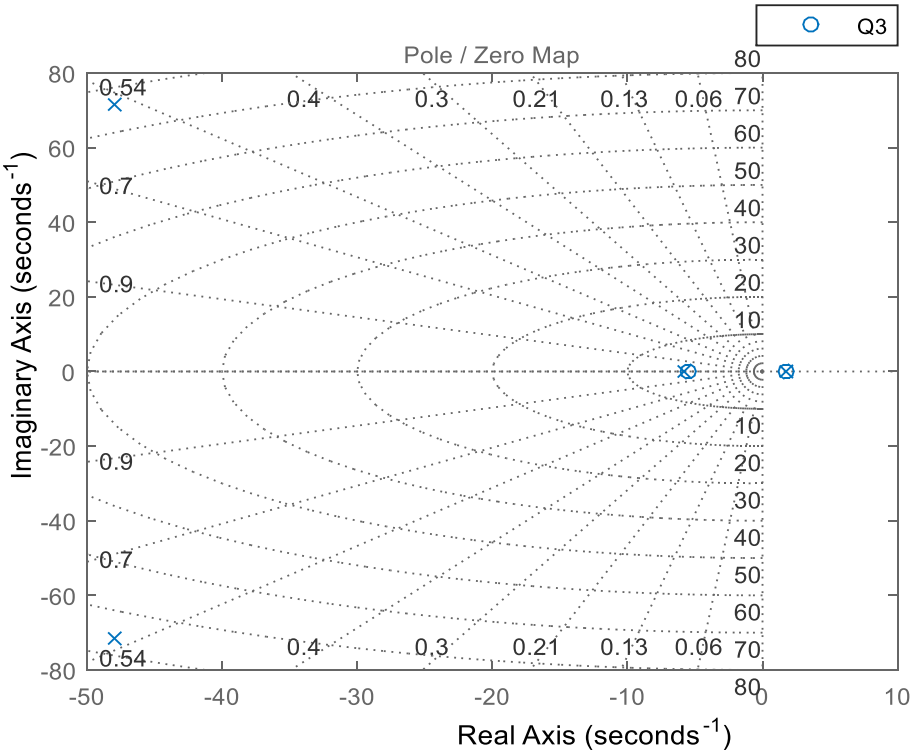


Figure 5.24 the pole-zero map of subsystem Q_3

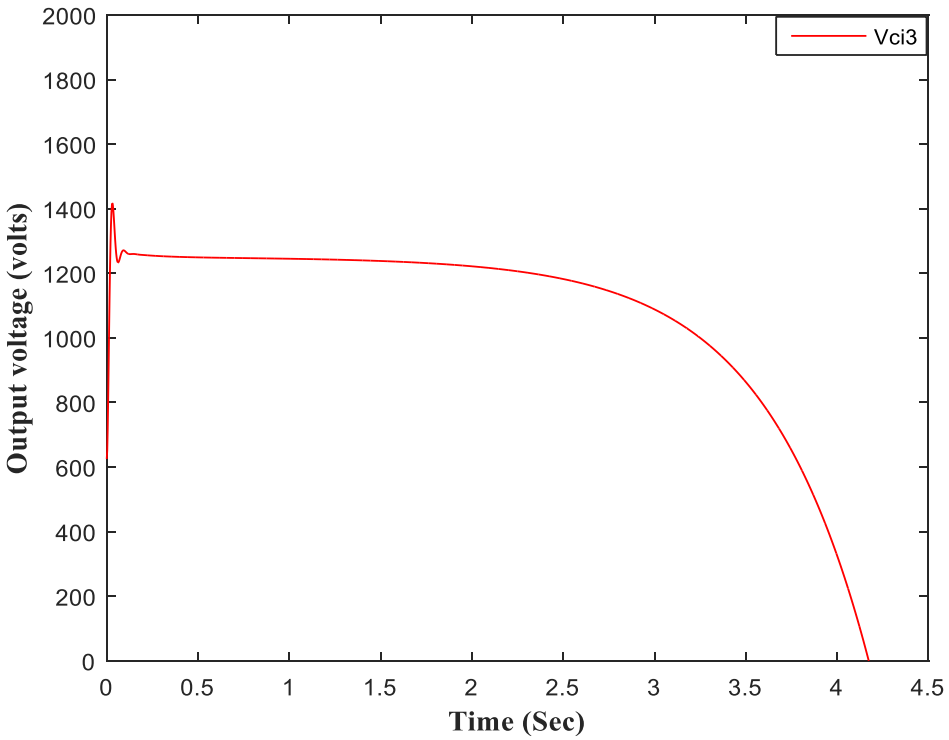


Figure 5.25 the output response curve V_{ci3} as a subsystem (module) of the proposed DC transformer with instability condition

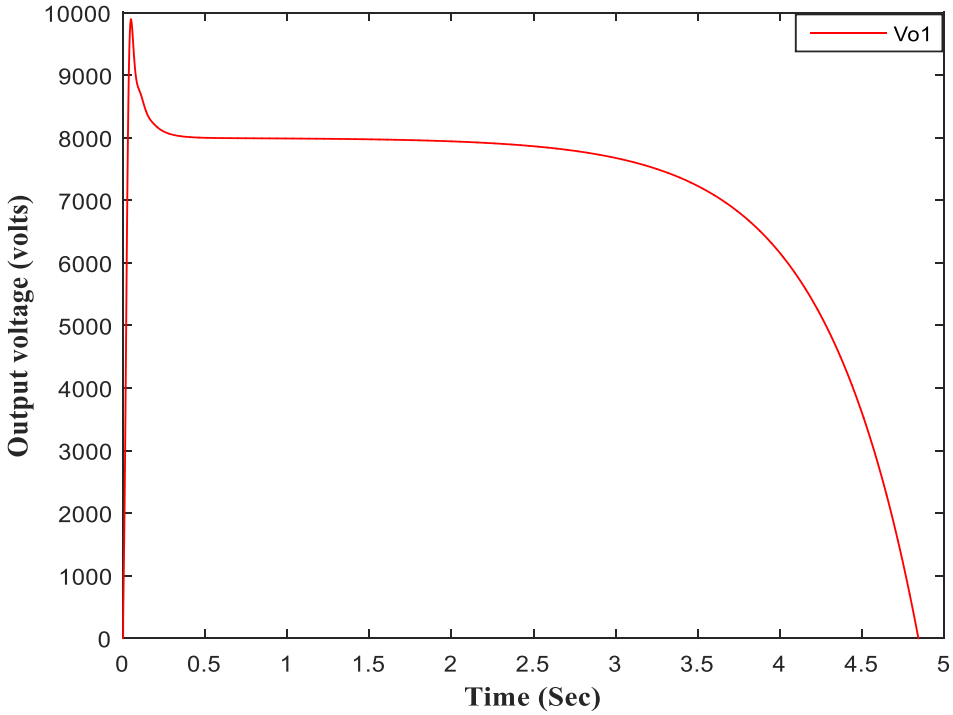


Figure 5.26 the output response curve V_{o1} of the proposed DC transformer due to instability in the third subsystem

In order to find the effect of the pole being in the RHP (see the S-plane of figure 5.27) on the system's stability, table 5.12 is produced to provide unstable gain.

Table 5.12 The stability condition of PID₃ gains (zero error and no overshoot)

Condition (stability rule with zero error) Q_3	**Gain selection**	**Pole/zero analysis**
$\boldsymbol{k_P > 0.003}$ & $\boldsymbol{k_P > 0.353}$	$k_P = 0.0001$	$s_{z1} = 3.21$
$\boldsymbol{k_I > 0}$ & $\boldsymbol{k_I > 0.219}$	$k_I = -1$	$s_{z2} = -3.11$
$\boldsymbol{k_D > 0}$ & $\boldsymbol{k_D > 0.05}$	$k_D = 0.1$	$s_{p1} = 3.14$
		$s_{p2} = -3.18$
		$s_{p3} = -50 + 70.8\,i$
		$s_{p4} = -50 - 70.8\,i$

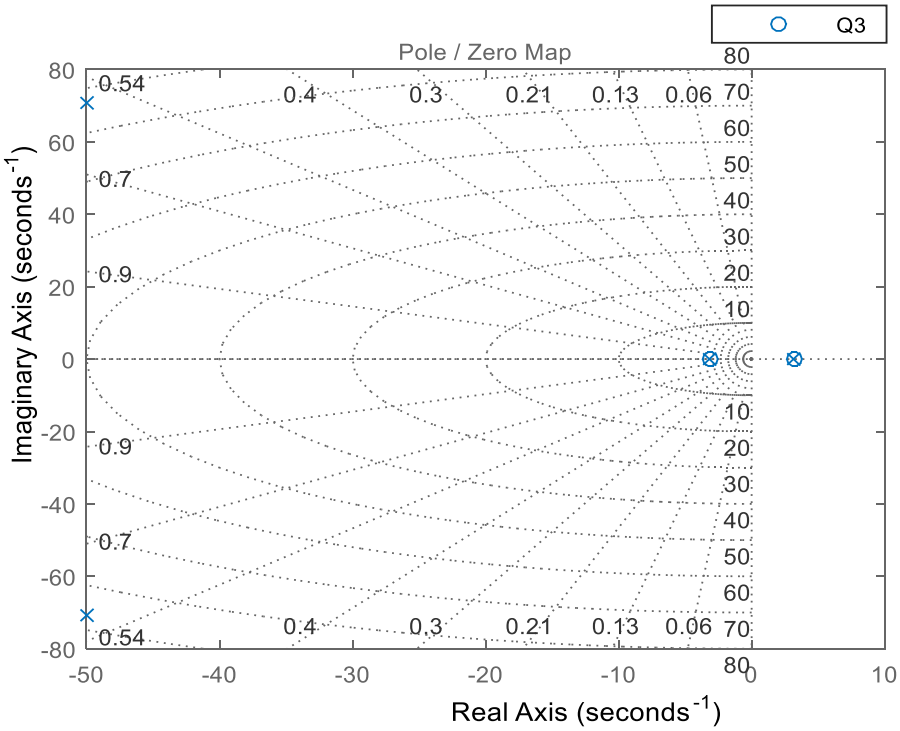


Figure 5.27 the pole-zero map of subsystem Q_3 due to unstable PID_3 gain selection

Figure 5.28 exhibits the effect of the pole and zero in the RHP on the systems' stability in which V_{ci3} and V_{o1} tend towards zero as time increases.

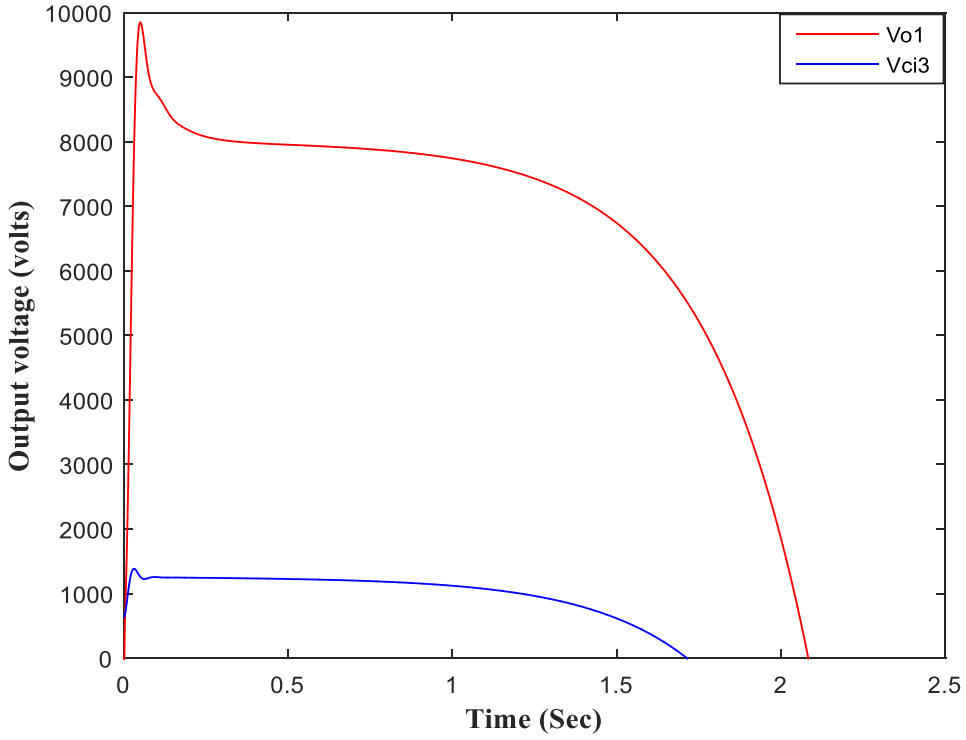


Figure 5.28 the output response curves V_{ci3}, V_{o1} of the considered example of the proposed DC transformer due to RHP pole and zero in the 3rd subsystem

5.5 Study into Flexibility and Robustness of the Designed PID Controller

To study the flexibility and robustness of the designed controller the MATLAB- SIMULINK simulations have been performed on the considered example (three-input two-output) of the proposed DC transformer as shown in figure 5.29 under different scenarios, i.e. different loads and input sources values. The simulation results are presented for three different input DC sources which varied within their corresponding ranges ($V_{i1} = (200 - 500)V$, $V_{i2} = (350 - 875)V$ and $V_{i3} = (250 - 625)V$. The controller has been designed for each scenario in such a way to provide the DC voltages of $V_o = 4\ kV, V_{o1} = 8\ kV$ and $V_{o2} = 11\ kV$. This is achieved through adaptation of PID controllers for the set requirement on the first stage (phase) of the proposed DC transformer when the input sources values changes. And in the case of load variations the PID controllers of the output stage (phase) will be adapted to provide regulating the output DC voltages V_{o1} and V_{o2}.

In the preceding sections, the considered example (three-input two-output) of the proposed MIMO DC transformer will be operated in two different scenarios shown below to reveal the reliability, robustness and flexibility of the devised PID controllers:

a. When all input sources (which is here three sources) are available to feed the loads, V_o is the summation of the three input modules.
b. One source from the three sources will not be available. Then the effects of the voltage change and the load change will be studied.

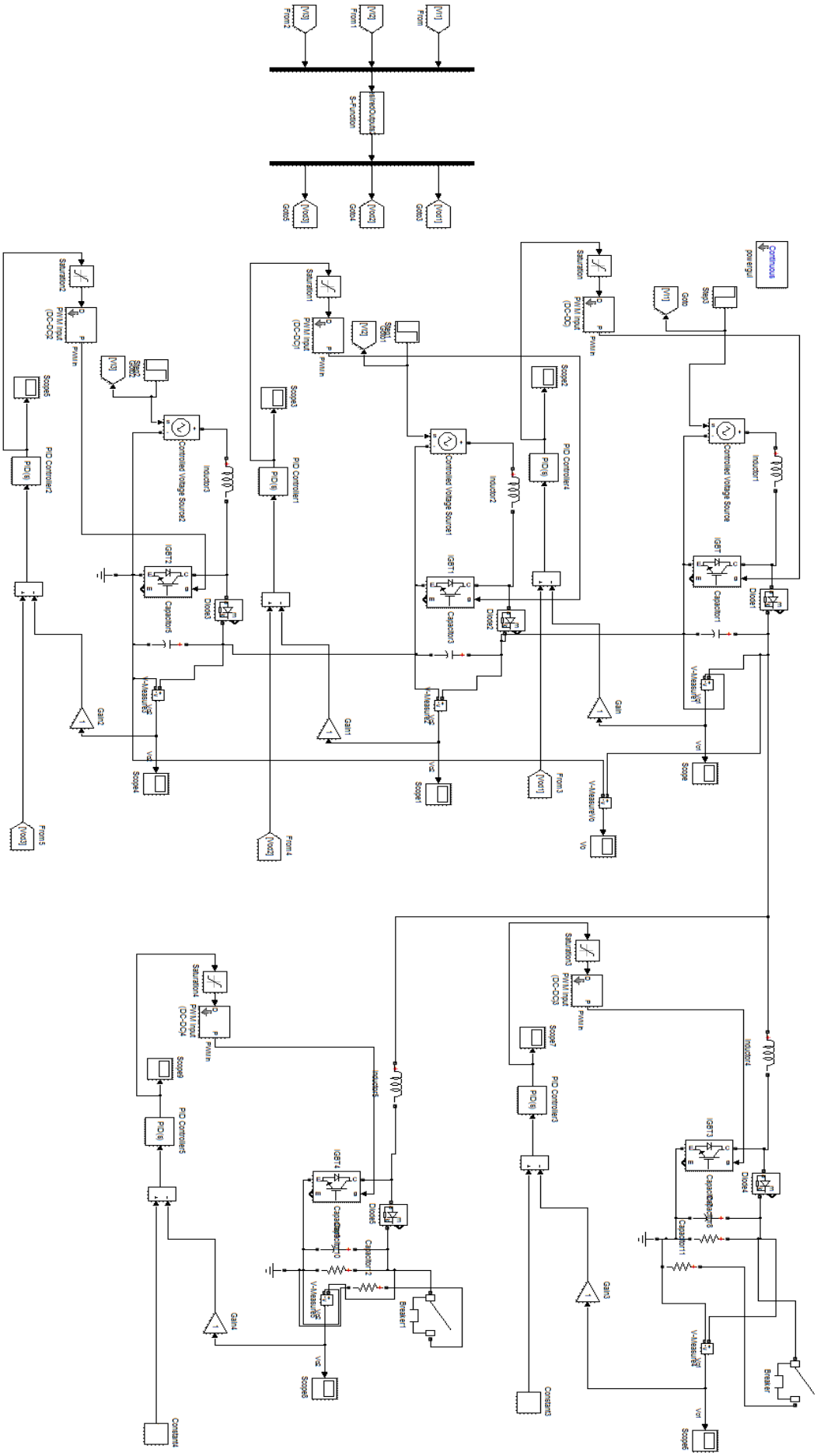


Figure 5.29 the SIMULINK diagram of (three-input double-output) of the proposed DC transformer

5.5.1 First Scenario: All input sources are available in the system to feed the loads

There exist a few possibilities under this scenario which will be discussed in the following sub-sections.

5.5.1.1 Fixed demand and supply

For the considered example of the proposed DC transformer, assuming that all three inputs are available and not varied, and there is no variation on the demand. In this case the DC bus voltage V_o and the output voltages V_{o1}, V_{o2} are fixed to the predefined requirements as follows:

$$(V_{ci1} + V_{ci2} + V_{ci3}) = V_o = 4\ kV, V_{o1} = 8\ kV \text{ and } V_{o2} = 11\ kV$$

The simulation results of the output voltages V_o, V_{o1} and V_{o2} under this scenario are shown in figures 5.30.a, 5.30.b and 5.30.c.

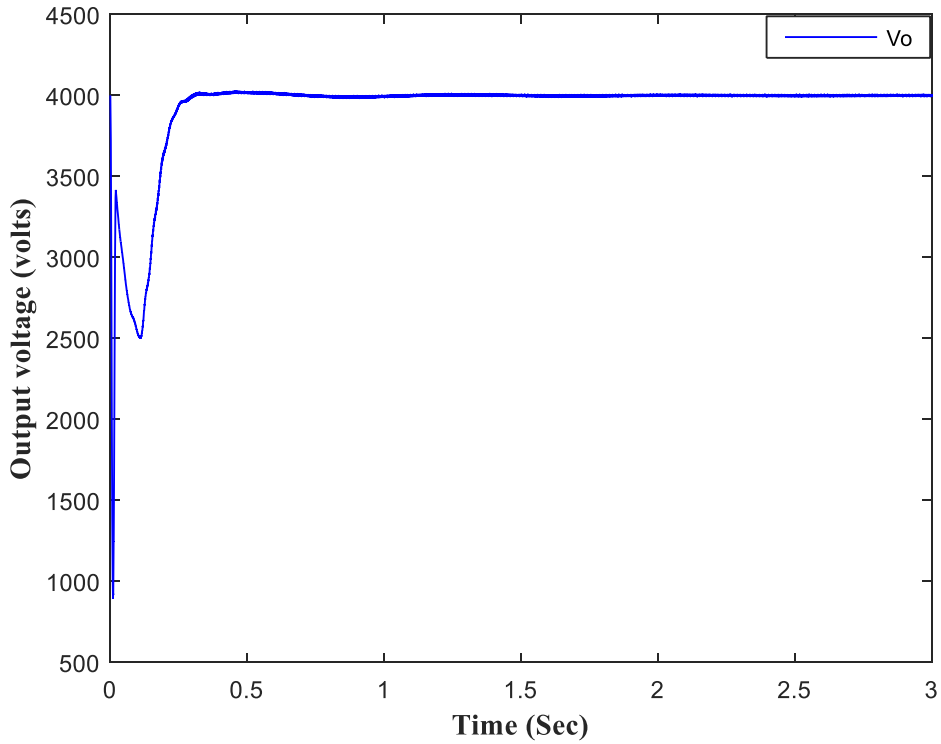


Figure 5.30.a. The bus DC voltage V_o without inputs\loads variation

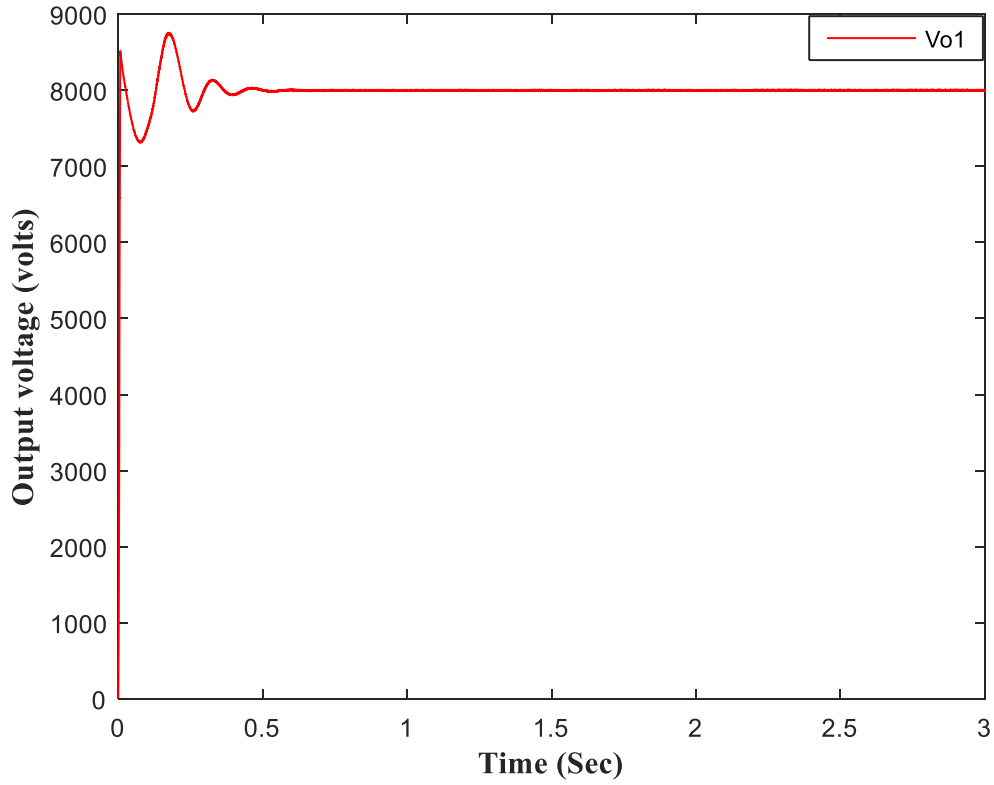


Figure 5.30.b. The output DC voltage V_{o1} without inputs\loads variation

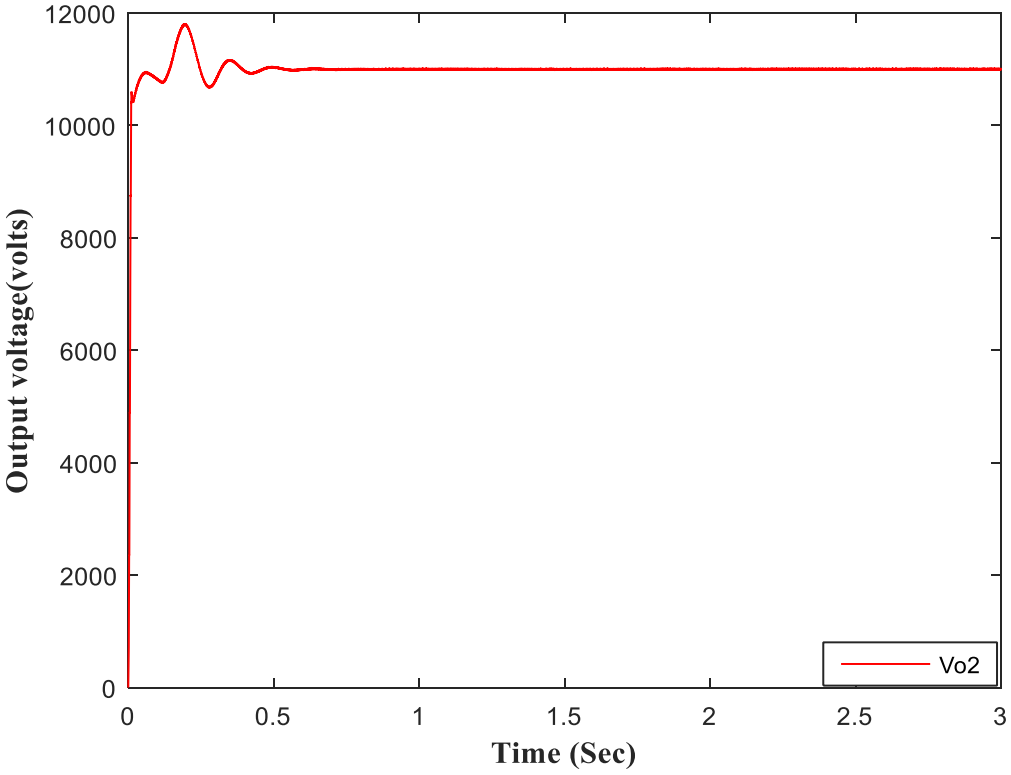


Figure 5.30.c. The output DC voltage V_{o2} without inputs\loads variation

Figure 5.30. The outputs DC voltage V_o, V_{o1} and V_{o2} results without inputs\loads variation

5.5.1.2 Demand and supply variation

In this case the robustness / reliability or integrity of the considered example of the proposed DC transformer with its entire associated PID control algorithm is tested under load or input supply variation cases (load variation at $t = 0.5\ Sec$ where R_L changed form $1\ k\Omega$ to $R_L = 500\ \Omega$ and the input sources varied at $t = 1\ Sec$ as the input values reduced by 20% of the original values). As the considered example is operated by the switches such as $S_{i1}, S_{i2}, S_{i3}, S_{o1}$ and S_{o2}. And each switch has its own specific duty. By proper regulation of switches' duty cycles, the predetermined DC bus voltage and output voltages V_{o1}, V_{o2} are obtained.

Figures 5.31 depict the simulation results of the DC bus voltage V_o and the output voltages V_{o1} and V_{o2} respectively.

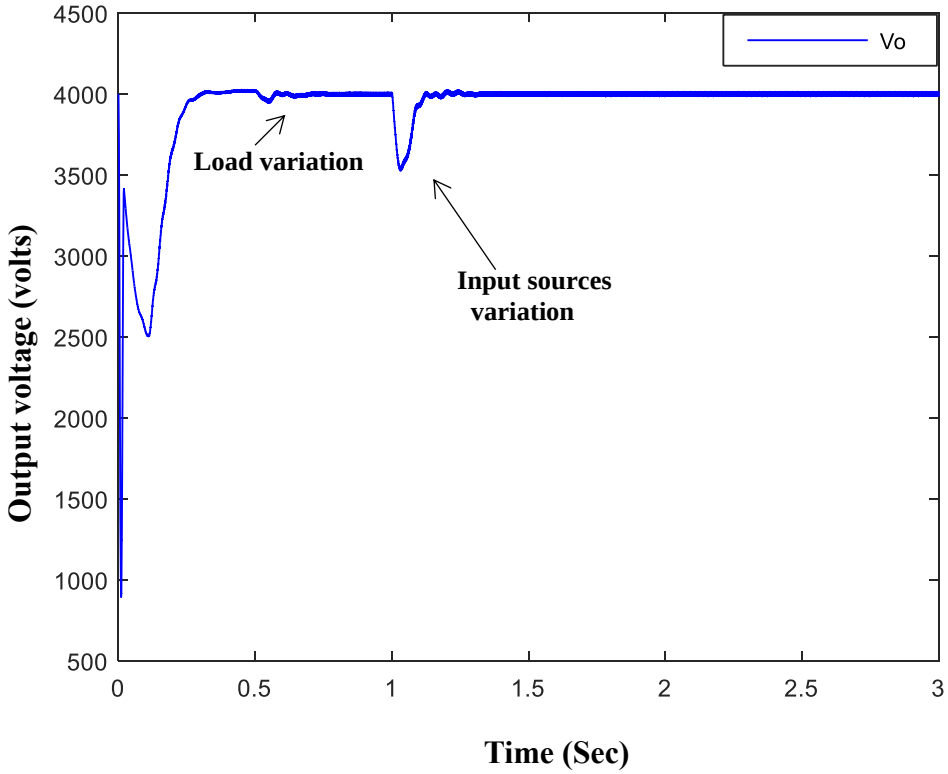


Figure 5.31.a The bus DC voltage V_o with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\ \Omega$ and the input sources varied at t=1s as the input values reduced 20% of the original values.

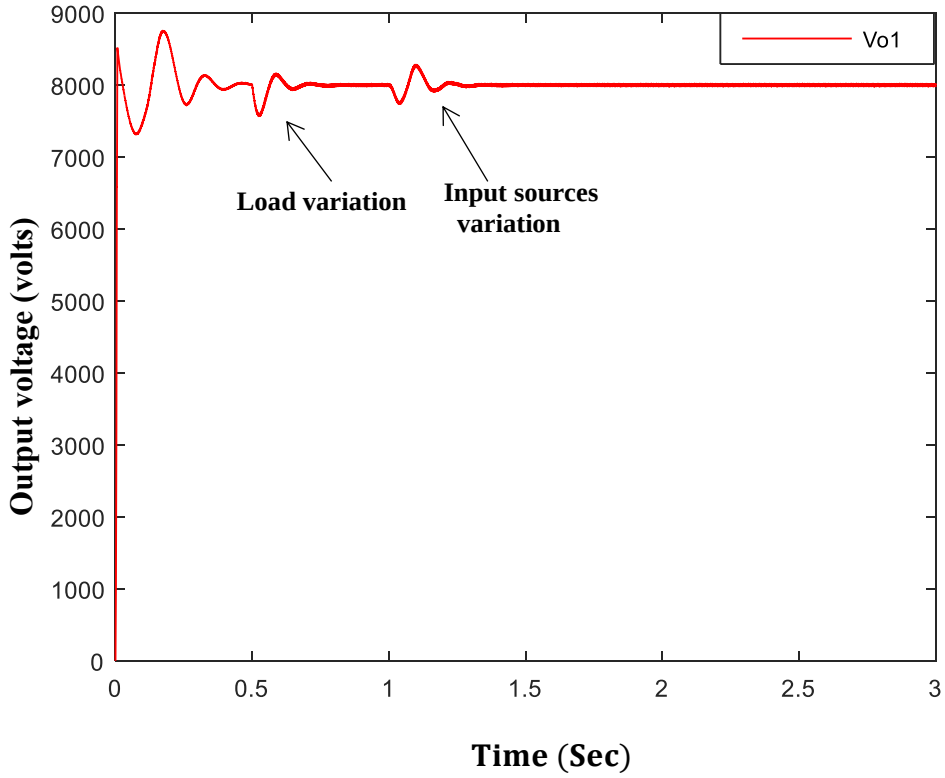


Figure 5.31.b The output DC voltage V_{o1} with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\ \Omega$ and the input sources varied at t=1s as the input values reduced 20% of the original values.

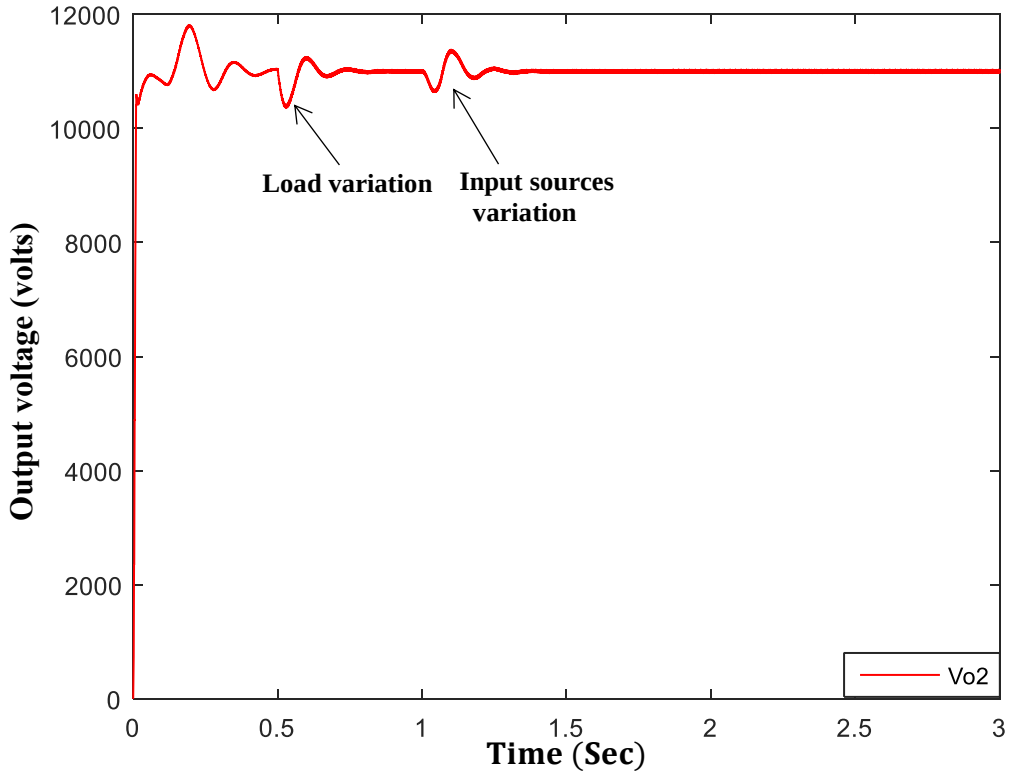


Figure 5.31.c The output DC voltage V_{o2} with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\ \Omega$ and the input sources varied at t=1s as the input values reduced 20% of the original values.

Figure 5.31. The outputs DC voltage V_o, V_{o1} and V_{o2} results with inputs\loads variation

From the results obtained in this scenario, it is noticeable that the DC bus voltage is not affected significantly when the load changes. This is because V_o is load independent. This is further investigated by increasing the loads' resistance values as shown in figure 5.32. Analysis of figure 5.32 suggest that V_o keeps constant as the load resistance changes, while V_{o1}, V_{o2} affected by the load values.

However any variation on the input sources is instantly felt by the DC bus voltage, although the PID controllers adapt and reduce the error voltage by controlling the duty ratios of the input power switches S_{i1},S_{i2} and S_{i3} and the desired voltage with no overshoot and with small peak to peak ripple voltage ($V_{o_{(ripple)(p-p)}} = 20$) volts is obtained within $0.2\ Sec$. The ripple factor in this scenario is:

$$V_{o(ripple)_{rms}} \frac{V_{o(ripple)_p}}{\sqrt{2}} = 7.14\ V \tag{5.85}$$

$$Ripple\ factor = \frac{V_{o(ripple)_{rms}}}{V_{o(DC)}} * 100\% = 0.178\ \% \tag{5.86}$$

where

$V_{o_{(ripple)(p-p)}}$ represents the peak-to-peak ripple value of bus voltage.

$V_{o_{(ripple)(rms)}}$ defined as the root mean square (rms) value of ripple voltage.

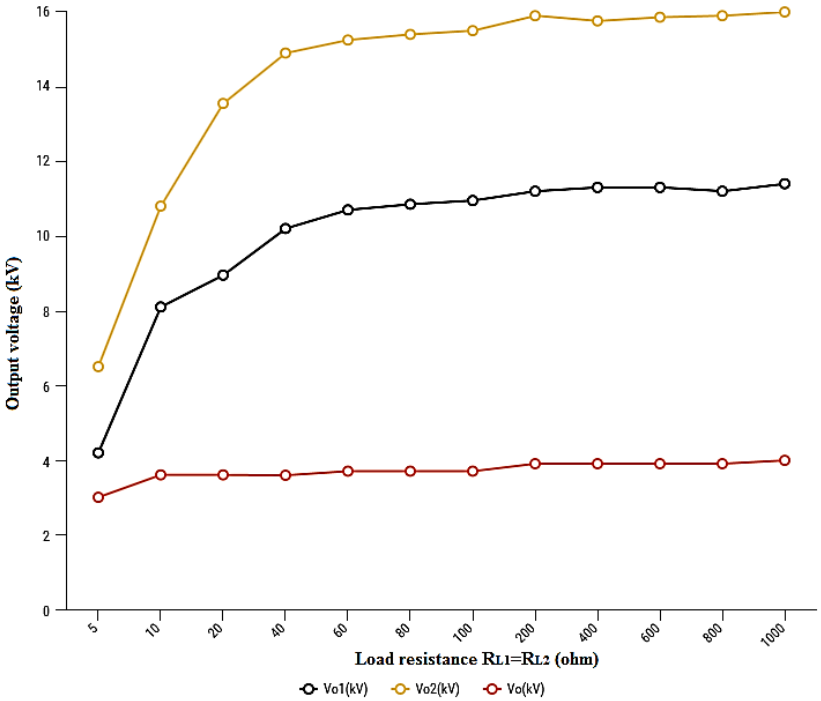


Figure 5.32 The relation between the output voltages V_o, V_{o1} and V_{o2} of three-input two-output of the proposed DC transformer with load resistance values

Similarly, the performance of the designed controller for a predetermined value of the output voltages V_{o1}, V_{o2} has been tested under variation of input sources. The controllers demonstrated their flexibility and robustness as well as their ability to maintain the output voltages V_{o1}, V_{o2} fixed with 9.3% overshoot peak for V_{o1} and 7.2% for the second output V_{o2} as shown in figures 5.31. The peak-to-peak ripple of output voltages and output currents are:

$$V_{o1_{(ripple)(p-p)}} = V_{o2_{(ripple)(p-p)}} = 40\ V$$

And

$$I_{o1_{(ripple)(p-p)}} = I_{o2_{(ripple)(p-p)}} = 200\ mA.$$

Also shown below are the calculated voltage ripple factors of the output voltages:

$$Ripple\ factor(V_{o1}) = \frac{V_{o1(ripple)rms}}{V_{o1(DC)}} * 100\% = 0.178\ \%$$

$$Ripple\ factor(V_{o2}) = \frac{V_{o2(ripple)rms}}{V_{o2(DC)}} * 100\% = 0.129\ \%$$

5.5.2 Second Scenario: One of the input power sources fails to supply the loads

In this scenario one of the input sources is no longer available to participate in feeding the loads. The PID controllers maintain the DC bus voltage V_o constant and increase the

switches' duty ratios of the available input sources to overcome the shortage acquired by the unavailability of one of the input sources. In the considered example (three-input two-output) of the proposed DC transformer three cases are simulated. The criteria for each case is that one of the input voltages is made to be zero and then the DC bus voltage V_o is measured when the load changed at $t = 0.5\ Sec$ from $1\ k\Omega$ to $500\ \Omega$. These are illustrated in figures 5.33.a, 5.33.b and 5.33.c.

The following process show when one of the sources is made zero how the other parameters are calculated. For example, assume that $V_{i1} = 0$ and then there are two inputs to supply the loads. Also let us consider that one of the inputs i.e. the second input has a fixed duty ratio value (80%) which is the maximum duty ratio, then the duty ratio of the third input is calculated as shown below:

$$D_{i2max} = 80\% \text{ then } V_{ci2} = \frac{V_{i2}}{(1 - D_{i2max})} \tag{5.87}$$

$$V_{ci3} = V_o - V_{ci2} \tag{5.88}$$

$$D_{i3} = \frac{V_{ci3} - V_{i3}}{V_{ci3}} \tag{5.89}$$

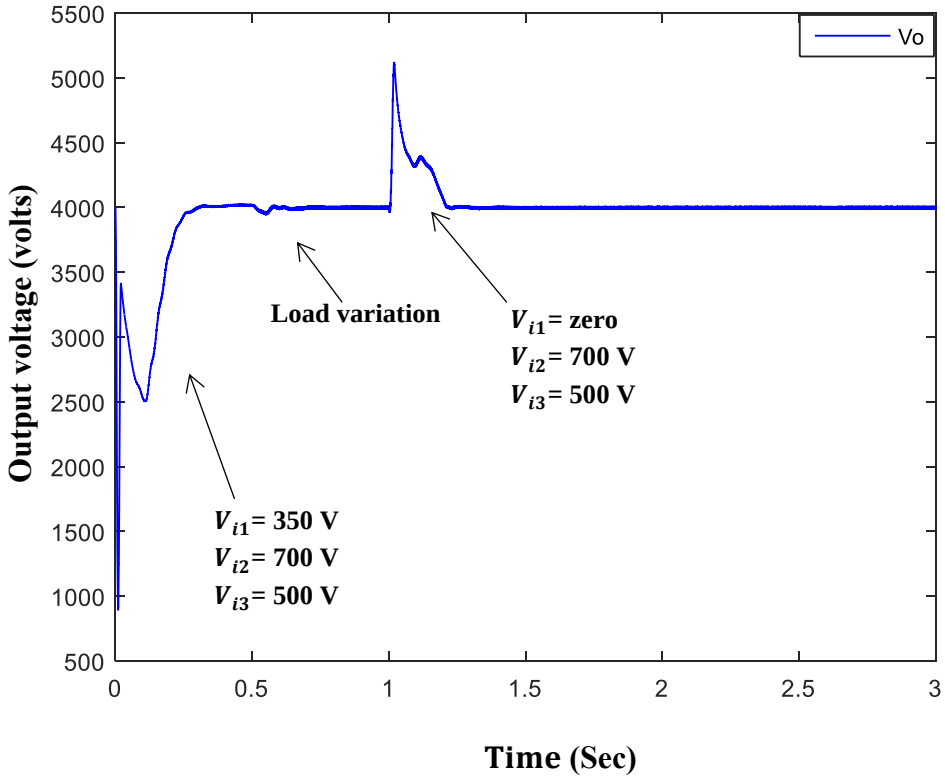


Figure 5.33.a The output DC voltage V_o with Load variation at t=0.5s where$R_L$changed from 1kΩ to R_L = 500 Ω and the input source V_{i1}=0 at t=1s.

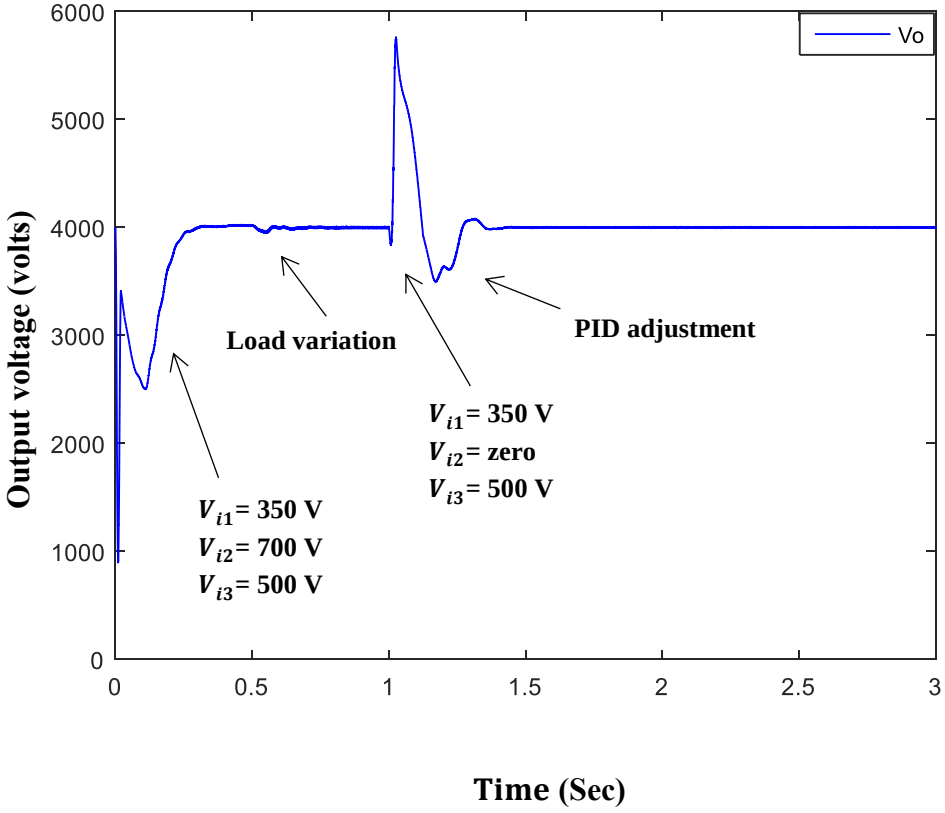


Figure 5.33.b The output DC voltage V_o with Load variation at t=0.5s where$R_L$changed from 1kΩ to R_L = 500 Ω and the input source V_{i2}=0 at t=1s.

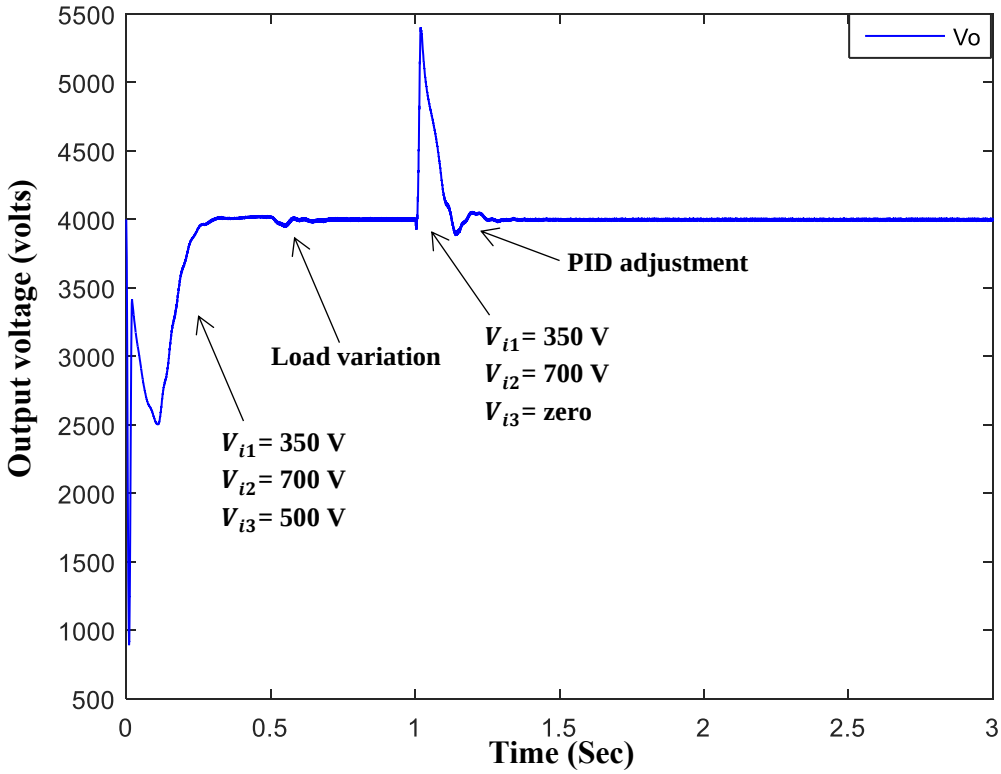


Figure 5.33.c The output DC voltage V_o with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\ \Omega$ and the input source V_{i3}=0 at t=1s.

Figure 5.33 The output DC voltage V_o under the second Scenario when one of the Input power sources fail to supply the Loads

As a whole, according to the results obtained from the simulation of a three-input two-output DC transformer model associated with PID controllers these results demonstrate the flexibility and robustness of the designed controller. The DC bus voltage V_o remains fixed as the input sources changes or when the loads changes. According to that the designed controller automatically adapts and changes the duty ratio of each power switch to get the desired output voltage. Similarly, when one of the input sources is no longer available in the system the controller takes the action to increase the output voltages that generated by the rest of the available sources in order to keep V_o constant.

5.5.2.1 Low Pass Filter (LPF) design

The capacitors C_{i1}, C_{i2}, C_{i3} are fully charged in the system when the three sources are available (during the normal case). When one of the input sources is no longer available, it is noticeable from the output response curves which illustrated in figures 5.33 that at $(t = 1\ Sec)$ one of the input sources becomes zero so immediately the charge dissipated with the same amount of the charged capacitor before being dropped; because of that there is a spike at $(t = 1\ Sec)$ with different amount of charge depends on which source is no longer

available at that time. To keep the system adapted the PID adjustment takes place for the desired voltage V_o.

In addition, in the simulation results the DC bus voltage response curve has an unwanted oscillation at the beginning of the simulation, and this is due to the connection of the input capacitors C_{i1}, C_{i2} and C_{i3} as they are connected in series. At the beginning of the simulation each one has a different charge and voltage and according to the electrical components connected in series must have the same current flow. Hence, the system trying to adjust itself and equalize the current and adding up the capacitors' voltage after 0.1 Sec of the simulation time.

To improve the V_o response curve as noticed in simulation results and to eliminate the unwanted oscillation at the beginning of the simulation as well as reducing the amplitude of the spike in the second scenario discussed in section 5.5.2, a first order Low Pass Filter (LPF) has been designed. This has been added in parallel with the sources stage; as shown in figure 5.34 and the time constant τ_{Filter} has been chosen in order to have faster response in the first stage than the next stage. This is because the first stage is responsible to feed the second stage of the designed DC transformer, thus a different percentage of the load stage time constant have been chosen with respect to the rise time of V_o response curve.

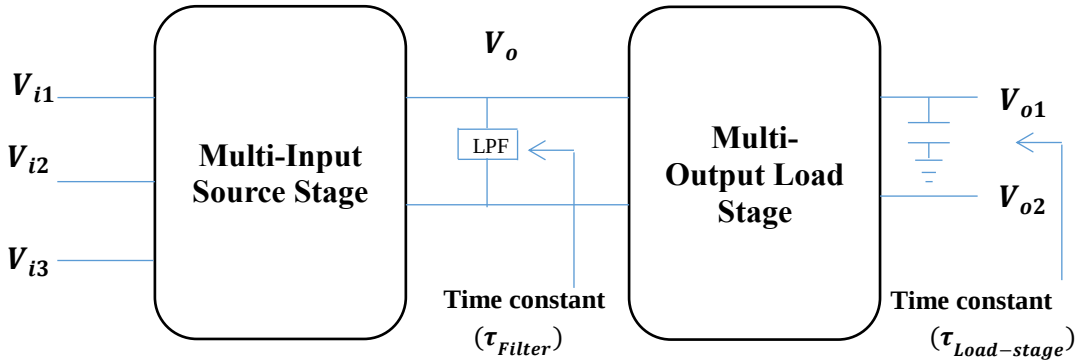


Figure 5.34 Block diagram of the designed three inputs double output DC transformer with LPF

The load stage time constant is calculated as follows:

$$Time\ constant\left(\tau_{Load-stage}\right) = R_{L1} * C_{o1} \tag{5.90}$$

$$Time\ constant\left(\tau_{Load-stage}\right) = 0.2675\ Sec$$

Figure 5.35 shows different percentage of the load stage time constant $(\tau_{Load-stage})$ and its effect on the rise time of V_o response curve in order to choose the proper τ_{Filter} which is necessary to design the $(R_{Filter}C_{Filter})$ LPF.

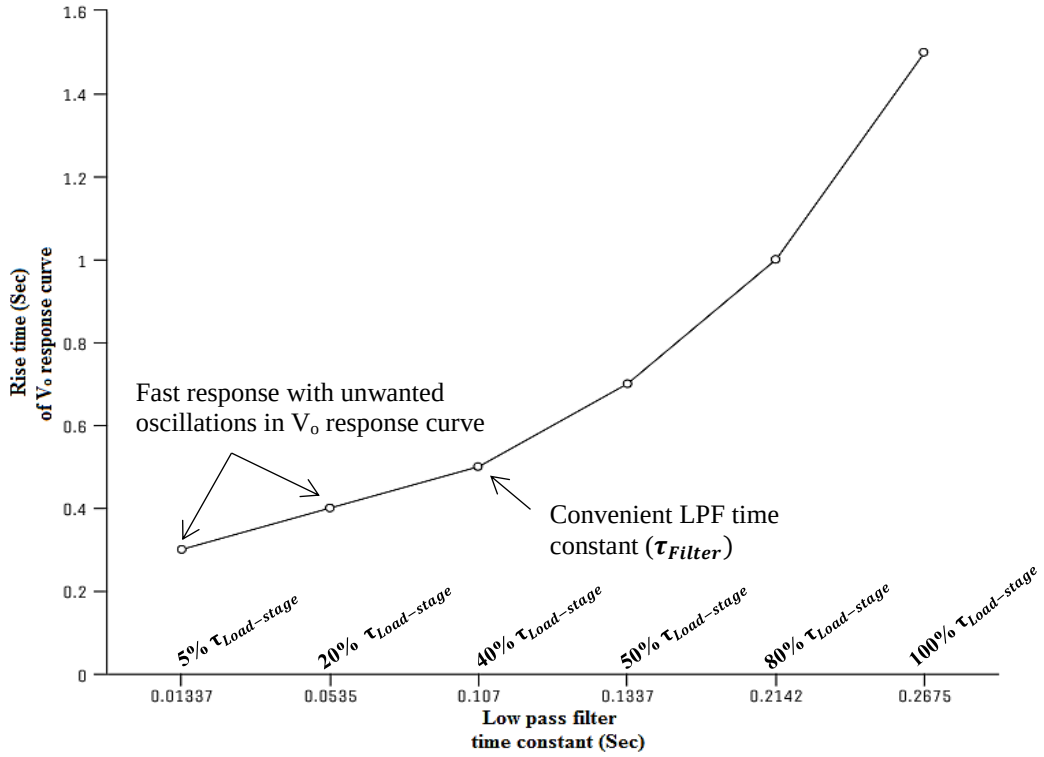


Figure 5.35 The relation between the LPF time constant and the rise time of V_o response curve.

In this study, the LPF time constant has been chosen to be 40% of the load stage time constant. Hence the values of the resistor R_{Filter} and the capacitor C_{Filter} have been calculated as follows:

$$Time\ constant(\tau_{Filter}) = 0.107\ Sec$$

$$0.107 = R_{Filter} * C_{Filter} \tag{5.91}$$

Rearranging equation (5.91):

$$C_{Filter} = \frac{0.107}{R_{Filter}} \tag{5.92}$$

It is worth noting that different values for R_{Filter} could be chosen for the calculation of the time constant. For example, if a larger resistor value is chosen, then a small capacitor is needed or vice versa in order to have the proper time constant as mentioned in equation (5.91).

Assuming that $R_{Filter} = 1\ k\Omega$ and substitute in equation (5.92) yields:

$$C_{Filter} = 107\ \mu F$$

Figure 5.36 depicts the output response curve of the DC bus voltage V_o with and without connecting the LPF.

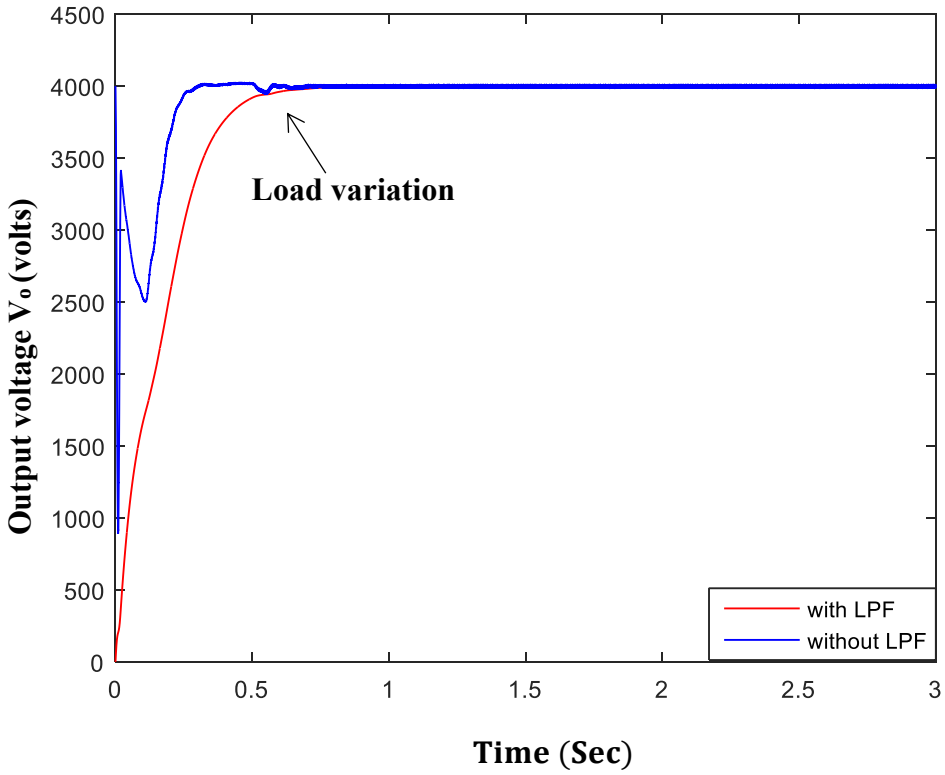


Figure 5.36 the DC bus voltage V_o response curve during the 1^{st} scenario with and without LPF.

Similarly, the LPF will improve the DC bus voltage V_o response curve during the second scenario which discussed in section 5.5.2, as the spike peak has been reduced by 84% as shown in figure 5.37.

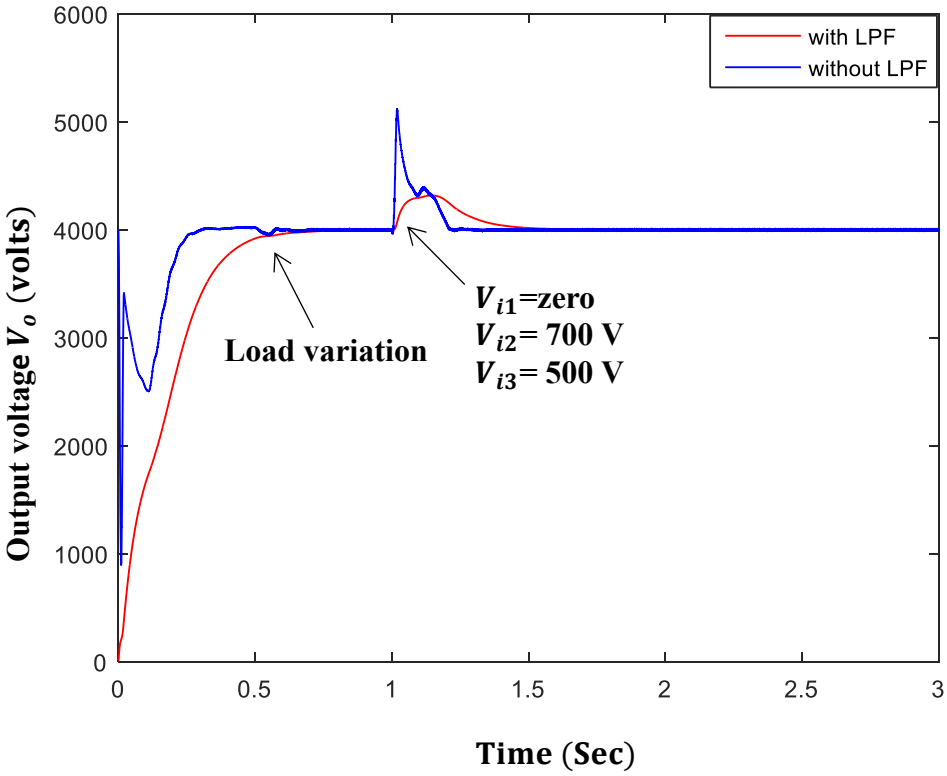


Figure 5.37 the effects of LPF on the DC bus voltage V_o response curve during the 2^{nd}scenario.

5.5.3 Third Scenario: System performance under fault conditions

- **DC transformer's operation without fault**

With reference to figure 5.5 in section 5.2, during the normal operation i.e. without presence of fault, the DC transformer operates through the following switching states: in switching state 1, L_{im} stores energy from the current supplied by its corresponding sources, in switching state 2 L_{im} keeps storing energy and L_{on} stores energy from the same source. However, in switching state 3 the energy stored in L_{on} and L_{im} is transferred through the diodes $Diode_{on}$ to the load side i.e. C_{on} and R_{Ln}. In the last switching state (state 4), the energy stored in the inductors L_{im} is transferred to the output side to be stored in L_{on}.

- **DC transformer's operation under fault conditions**

To examine the performance of the proposed DC transformer under fault conditions, different fault modes have been considered within the simulations. The DC transformers are subjected to various types of fault, where every component in a DC transformer is responsible for creating a fault such as the semiconductors, capacitors, inductors and the loads [151]. Here the response of the semiconductors devices (transistors and diodes) under different possible faults were obtained using MATLAB\Simulink model. Two types of line-to-ground faults namely Short Circuit (SC) and Open Circuit (OC) fault modes have been

analysed. SC or OC faults could be acquired in the switches (transistors) which used in the DC transformer. In this study, the fault modes have been analysed for each switch of the considered example (three-input double-output) of the proposed DC transformer. Initially, in the OC switches' fault modes the output voltage of the module (subsystem) which has the fault drops only by few volts, but the only problem of these fault modes is that there will not be any path for the inductor through the switch then the total supply is given to the load. The inductor charging and discharging decides the output voltage, as there will not be any boosting action taking place in the DC transformer and only the input is fed to the output without any switching operation after the fault. Therefore, the SC switches' fault modes have been analysed for each switch as illustrated in table 5.13.A. During each simulation only occurrence of one fault is considered.

In the case of diodes fault modes, the fault analysed for each diode of the considered example (three-input two-output) of the proposed DC transformer. The diodes' SC faults cause a very high inductors' current drawn from the sources which may damage the DC transformer's components. The performance of the DC transformer under SC diodes' faults is similar to its performance under SC transistors' faults. Then the OC diodes' fault modes have been analysed for each diode of the proposed DC transformer as shown in table 5.13.B. During each simulation only occurrence of one fault is considered.

Table 5.13 the considered example (three-input two-output) of the proposed DC transformer's fault operation modes

(A) Transistors Fault Modes

Fault / **Mode**	**Switching Transistors of Figure 5.4**				
	S_{i1}	S_{i2}	S_{i3}	S_{o1}	S_{o2}
1	SC	Normal	Normal	Normal	Normal
2	Normal	SC	Normal	Normal	Normal
3	Normal	Normal	SC	Normal	Normal
4	Normal	Normal	Normal	SC	Normal
5	Normal	Normal	Normal	Normal	SC

(B) Diodes Fault Modes

Fault / Mode	Switching Diodes of Figure 5.4				
	$Diode_{i1}$	$Diode_{i2}$	$Diode_{i3}$	$Diode_{o1}$	$Diode_{o2}$
6	OC	Normal	Normal	Normal	Normal
7	Normal	OC	Normal	Normal	Normal
8	Normal	Normal	OC	Normal	Normal
9	Normal	Normal	Normal	OC	Normal
10	Normal	Normal	Normal	Normal	OC

5.5.3.1 Short Circuit (SC) fault across the transistors

SC transistors faults have been analysed as a line-to-ground fault occurs across the transistors for short period of time where the fault time $t_F = 0.5\ m\ Sec$. As shown in table 5.13.A in each simulation only occurrence of one fault is considered which causes a high current pass through the inductors L_{im} or L_{on} when short circuit happens on transistor S_{im} or S_{on} respectively. For each fault the respective currents are:

$$I_{Lim} = I_{Sim} = \frac{V_{im}}{R_{s_{im}} + R_{ind_{im}}} \tag{5.93}$$

Or

$$I_{Lon} = I_{Son} = \frac{V_o}{R_{ind_{on}}} \tag{5.94}$$

Where

$R_{ind_{im,on}}$ represents the inductors resistance in ohms.

$R_{s_{im}}$ represents the input sources resistance in ohms.

From the above expressions it could be noticed that the SC fault modes cause a high current which increases linearly with time and this could damage the power DC transformer. In these fault modes, no current will pass through the DC capacitors (C_{im}) from the input module which has a fault.

As the performance of the system during the SC faults depend on the SC fault location (location of the switch) and the fault resistance (R_F), hence different locations with different fault resistance values have been analysed as follows:

5.5.3.1.1. Short Circuit (SC) transistor with solid fault ($R_F = 0$) on the input side of the proposed DC transformer

If a solid fault (i.e. fault resistance $R_F = 0$) happens across S_{i1} , then a high current passes through the inductor L_{i1} and the IGBT switch S_{i1} and this current increases linearly with the time as shown in figure 5.38 and this current could damage the power DC transformer. This will cause a disturbance in the output voltages as shown in figure 5.39.a, also will cause a drop in the voltage of the next input modules (i.e. $V_{ci2} = 0$). This is because the input modules are connected like a string. Then this fault mode will disturb the rest of the connected inputs. However, if the location of the SC fault (S_{im}) be for example in the middle of the string, then the effect of the fault on the output voltages will be reduced and the system recovers in a short period of time. Where in the fault modes 2 and 3 the recovery of the system is after $t = 0.19\ Sec$ when the fault has been cleared as shown in figures 5.39.b and 5.39.c.

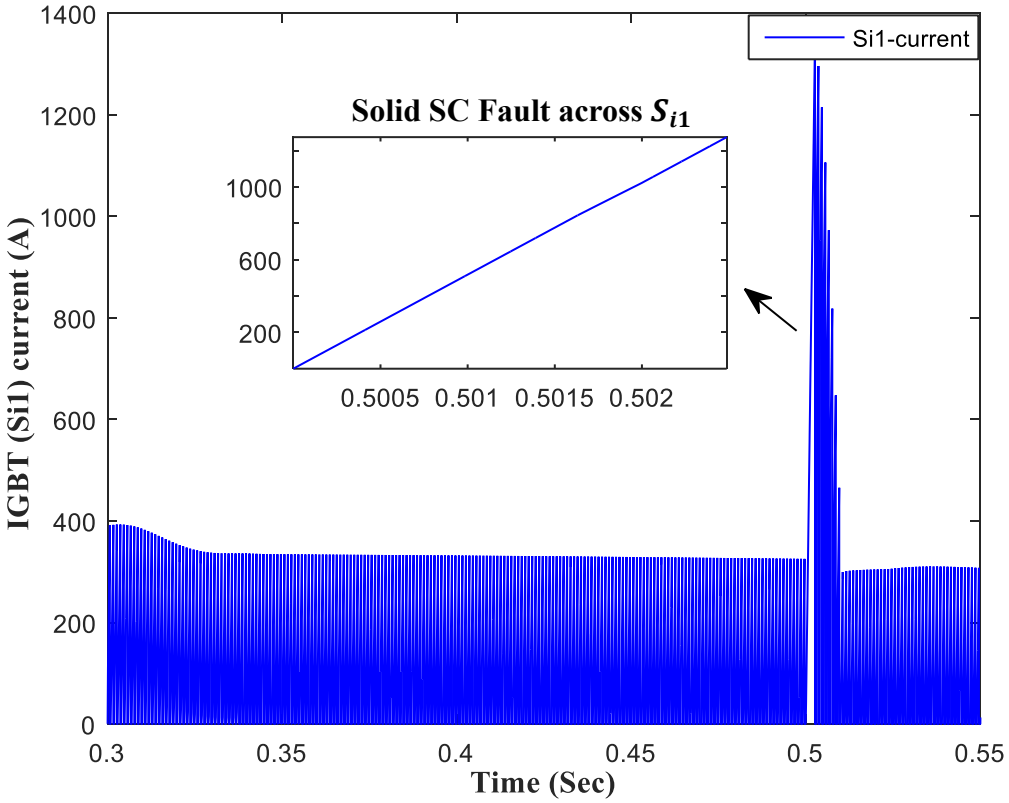


Figure 5.38 the current response curve of the power switch (S_{i1}) due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i1})

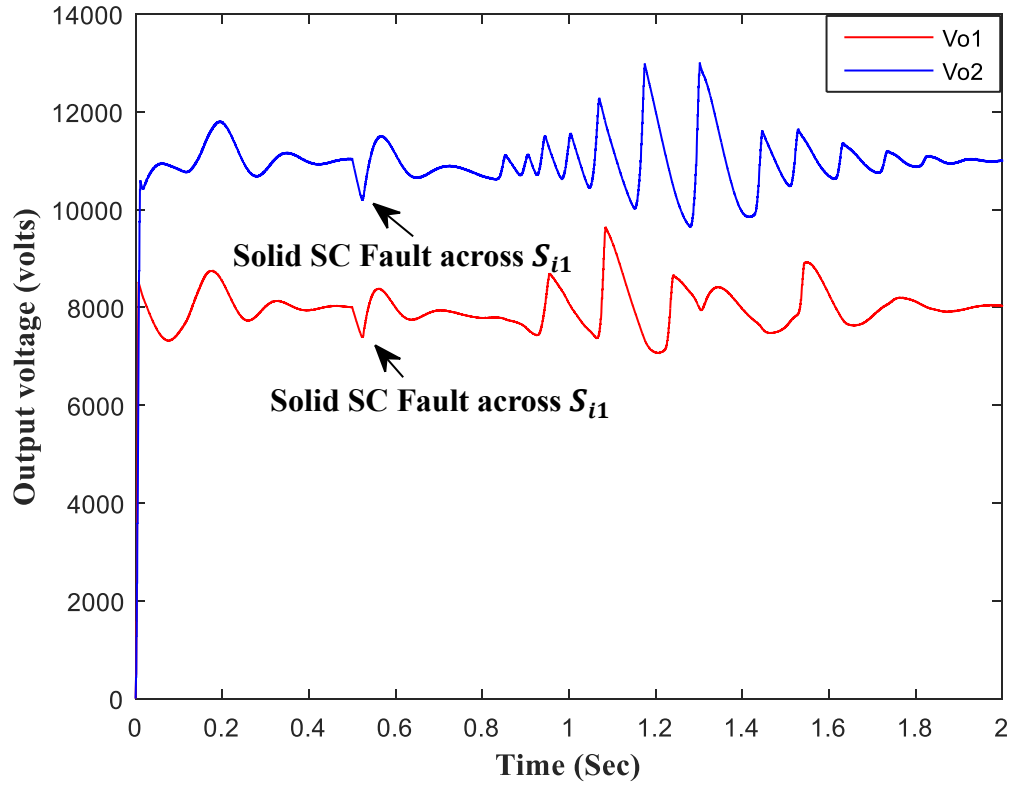


Figure 5.39.a. the output voltages response curves V_{o1}, V_{o2} due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i1})

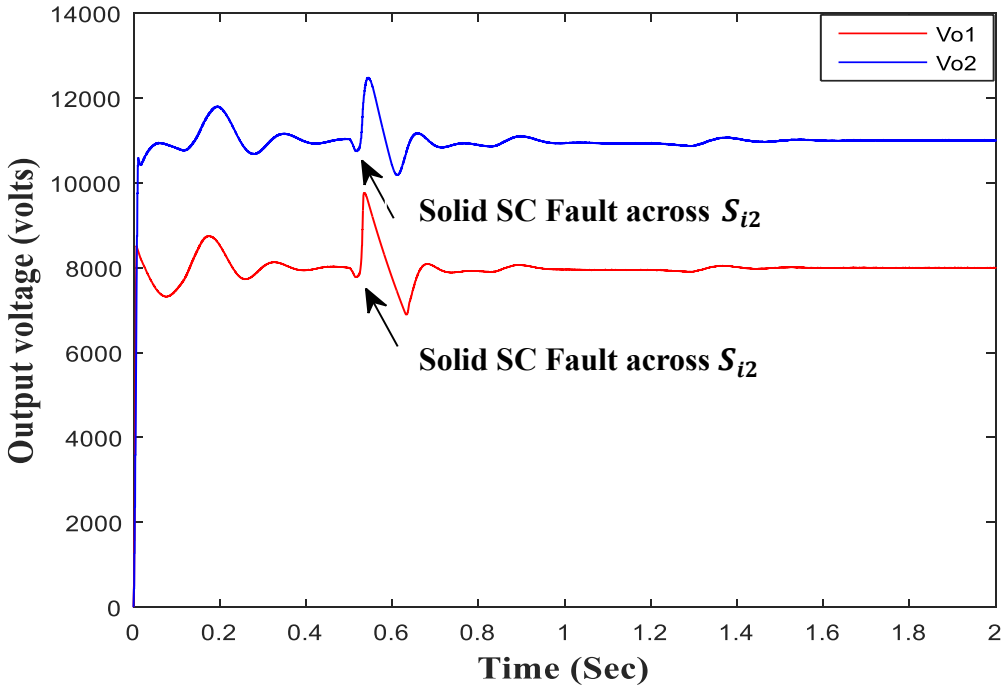


Figure 5.39.b. the output voltages response curves V_{o1}, V_{o2} due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i2})

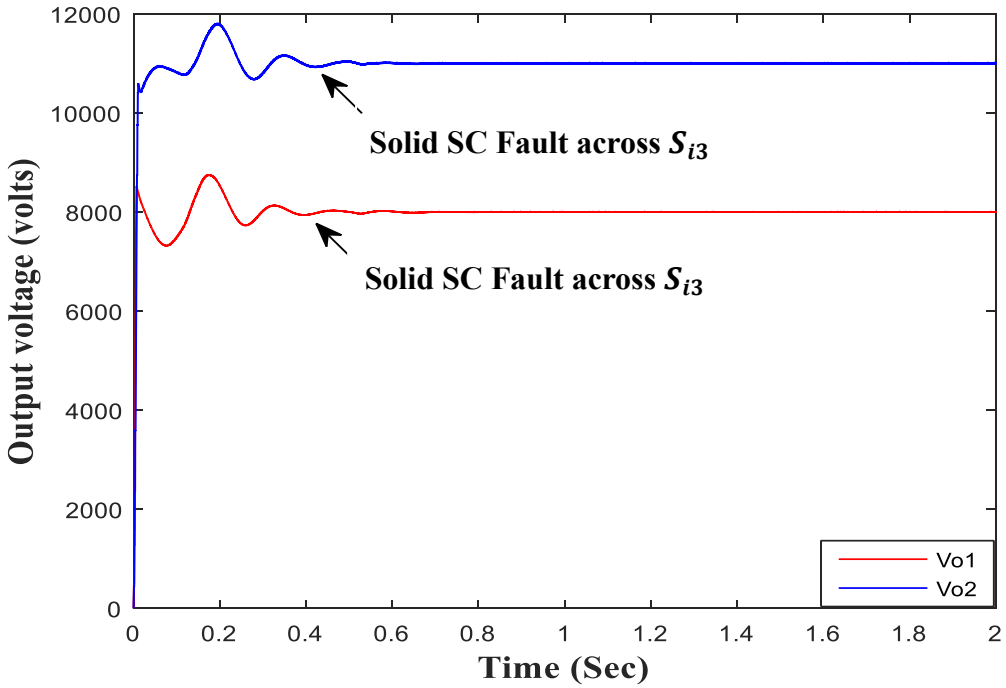


Figure 5.39.c. the output voltages response curves V_{o1}, V_{o2} due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i3})

Analysis of figure 5.39.b suggest that if the solid SC fault occurs across S_{i2}, this contributes to spikes on V_{ci1} and V_{ci2} response curves and their corresponding closed loop controllers adapt and recover. For example, V_{ci1} recovers after 0.6 Sec and for V_{ci2} recovers after 0.4 Sec . However, V_{ci3} will attain the input source value " V_{i3}" i.e. behaves as a source without stepping up the voltage.

Figure 5.39.c represents the result of simulation when the solid SC fault occurred across S_{i3}. In this fault mode the only output voltage response curve V_{ci3} will be affected where a high spike voltage has been detected which is recovered after 0.099 Sec.

5.5.3.1.2. Short Circuit (SC) transistor with solid fault ($R_F = 0$) on the output side of the proposed DC transformer

In the considered example (three-input two-output), if the solid fault occurs across S_{o1} or S_{o2} (output side switches) the whole system will shut down ($V_{ci1} = V_{ci2} = V_{ci3} = 0$) as the outputs of the system are connected in parallel. These are shown in the simulation results of figures 5.40.a and 5.40.b.

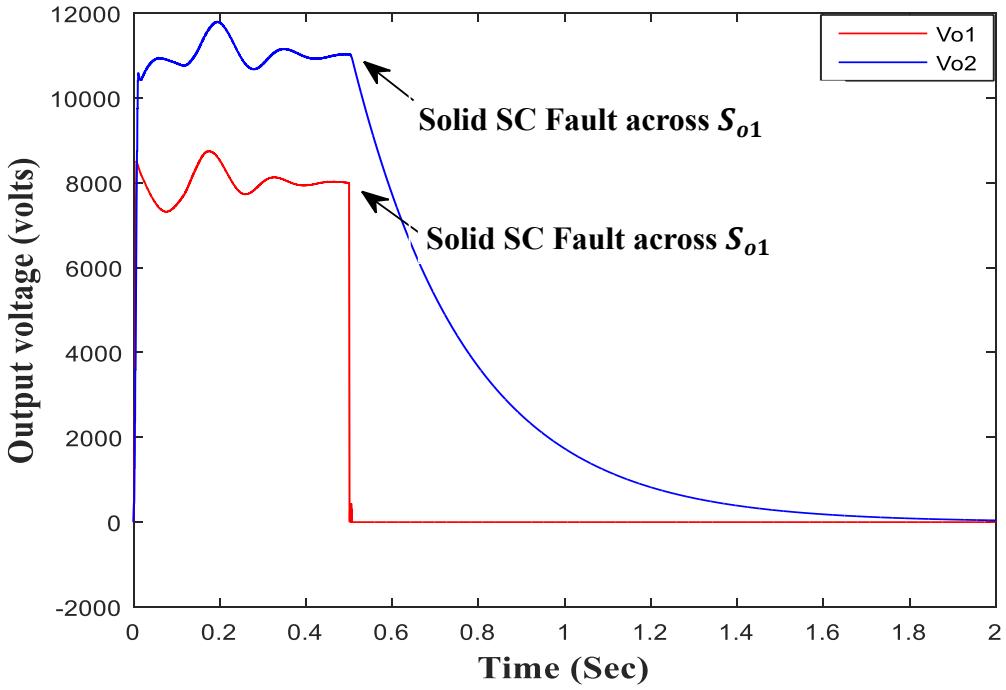


Figure 5.40.a. the output voltages response curves V_{o1}, V_{o2} due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o1})

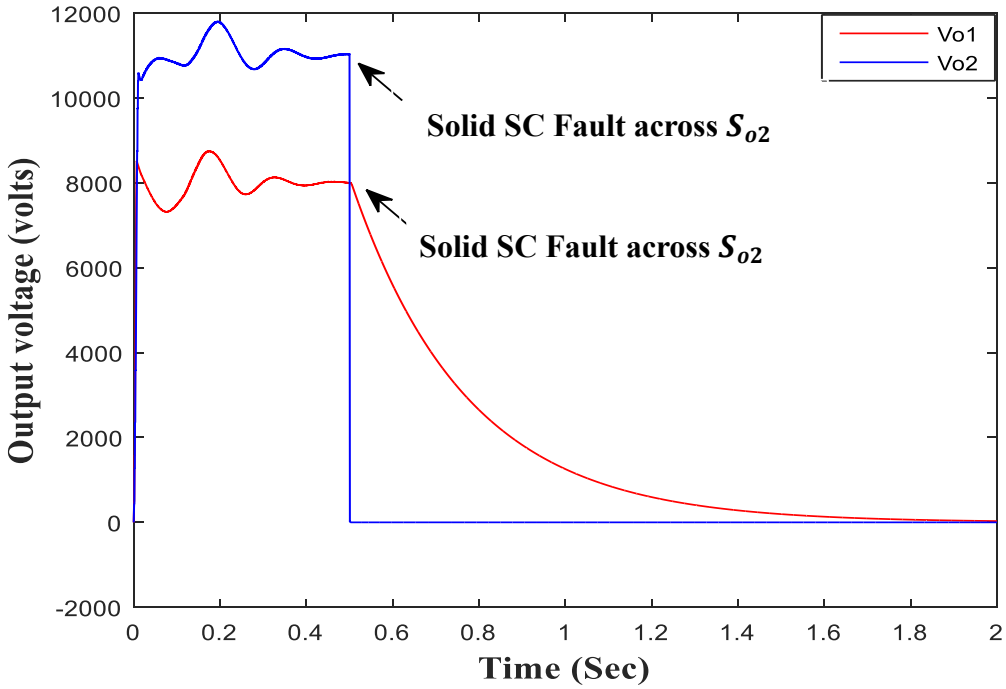


Figure 5.40.b. the output voltages response curves V_{o1}, V_{o2} due to a SC solid fault ($R_F = 0$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o2})

5.5.3.1.3. Short Circuit (SC) transistor with non-solid fault ($R_F > 0$) on the input side of the proposed DC transformer

The performance of the considered example (three-input two-output) of the proposed DC transformer has been tested under non-solid faults where the fault resistance has a value within the range $(0 < R_F < 10)\ \Omega$. As before, the SC non-solid fault occurs across the switching transistors but through a resistance.

The simulations of SC non-solid fault across S_{i1} with fault resistance $R_F < 3\ \Omega$ have revealed that it has the same characteristic as a solid fault mode. But as mentioned before the SC solid fault mode 1 causes a drop in the output voltage of the next input module where $V_{ci2} = 0$. This is true when the fault resistance value across the switch S_{i1} is less than $7\ \Omega$. However, as the fault resistance increases the ripple peak-to-peak voltages decreases. Therefore, the simulation of the outputs response curve of V_{o1} and V_{o2} under SC non-solid fault with $R_F = 10\ \Omega$ across S_{i1} is performed as shown in figure 5.41.a

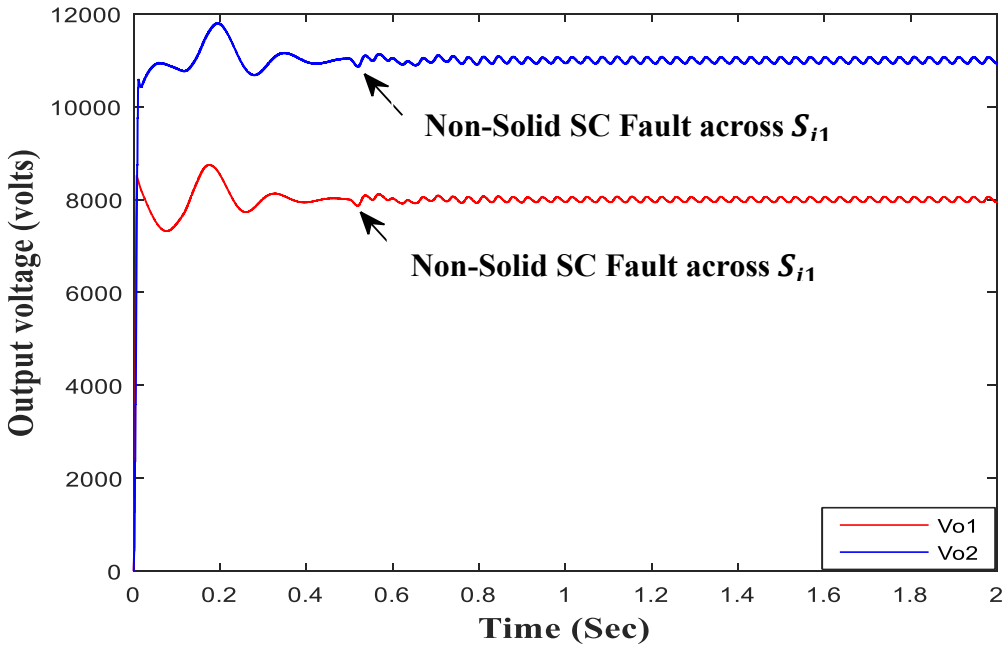


Figure 5.41.a. the output voltages response curves V_{o1}, V_{o2} due to a SC non-solid fault ($R_F = 10\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i1})

As shown in figure 5.41.b when non-solid fault with $R_F = 10\ \Omega$ occurs across S_{i2}, the amplitude of the peak-to-peak spike on the outputs voltage V_{o1}, V_{o2} are $40\ V, 50\ V$ respectively which is less in comparison to the solid faults $R_F = 0$. However, if the non-solid fault occurs across S_{i3} the system has the same performance as with the solid faults as shown in figure 5.41.c.

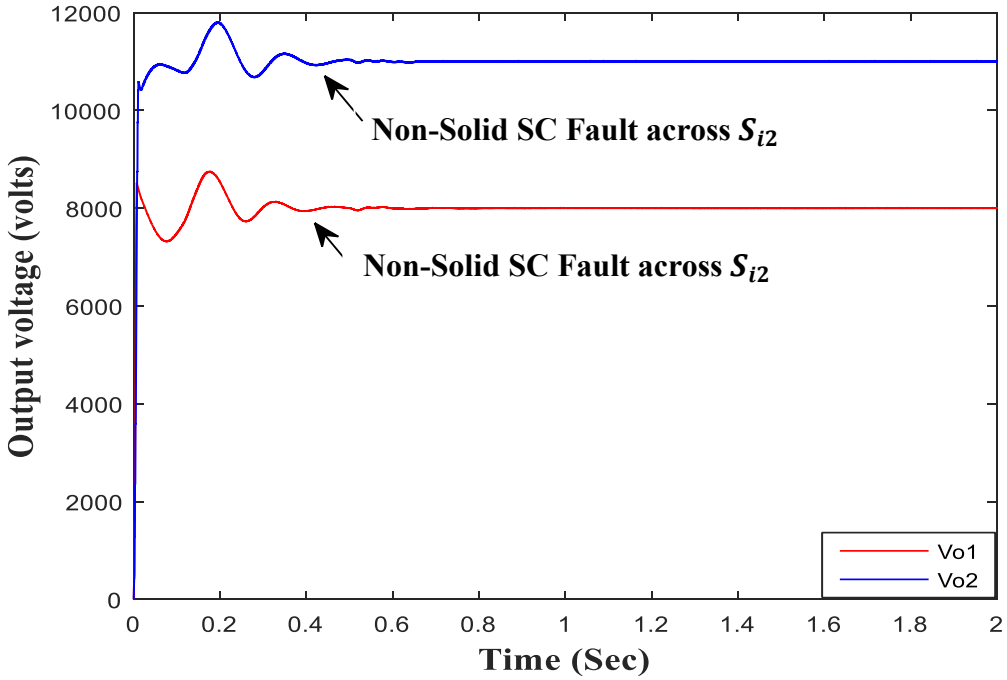


Figure 5.41.b. the output voltages response curves V_{o1}, V_{o2} due to a SC non-solid fault ($R_F = 10\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i2})

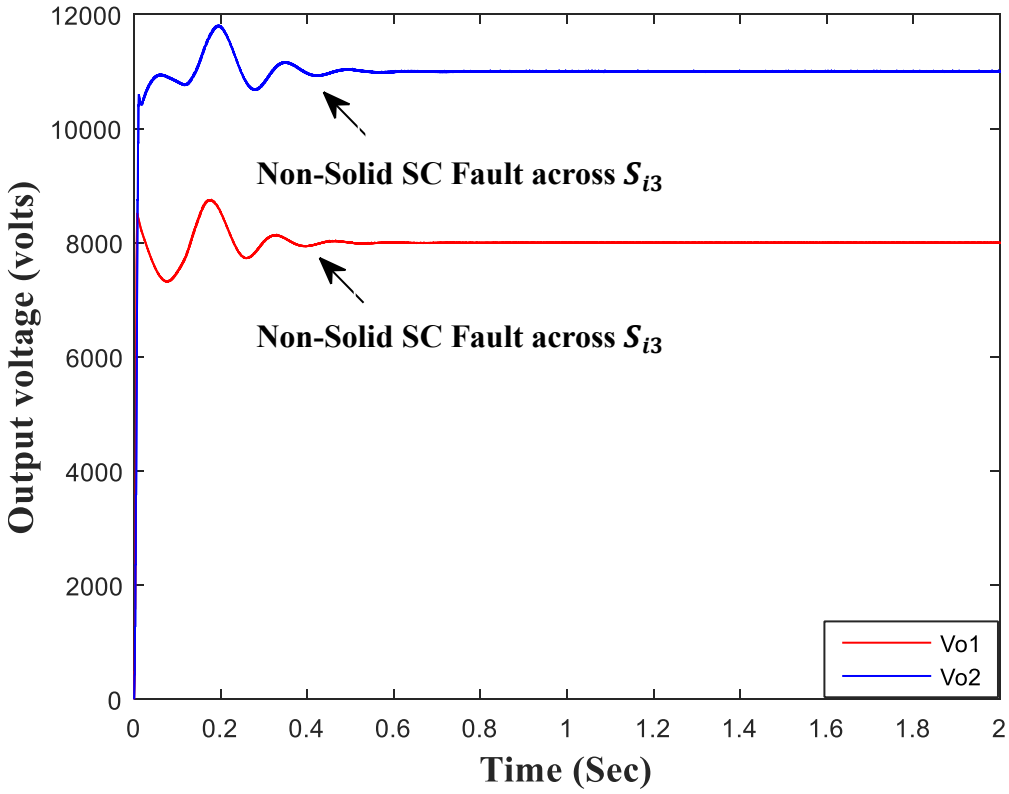


Figure 5.41.c. the output voltages response curves V_{o1}, V_{o2} due to a SC non-solid fault ($R_F = 10\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{i3})

5.5.3.1.4. Short Circuit (SC) transistor with non-solid fault ($R_F > 0$) on the output side of the proposed DC transformer

Figure 5.42 shows the effect of fault resistance (across transistors S_{o1} or S_{o2}) on the output voltage values V_{o1}, V_{o2}. Analysis of figure 5.42 suggest that for operation without failure i.e. V_{o1}, V_{o2} not tending towards zero and to protect the system, the fault resistance across S_{o1} or S_{o2} must be greater or equal to 30 Ω.

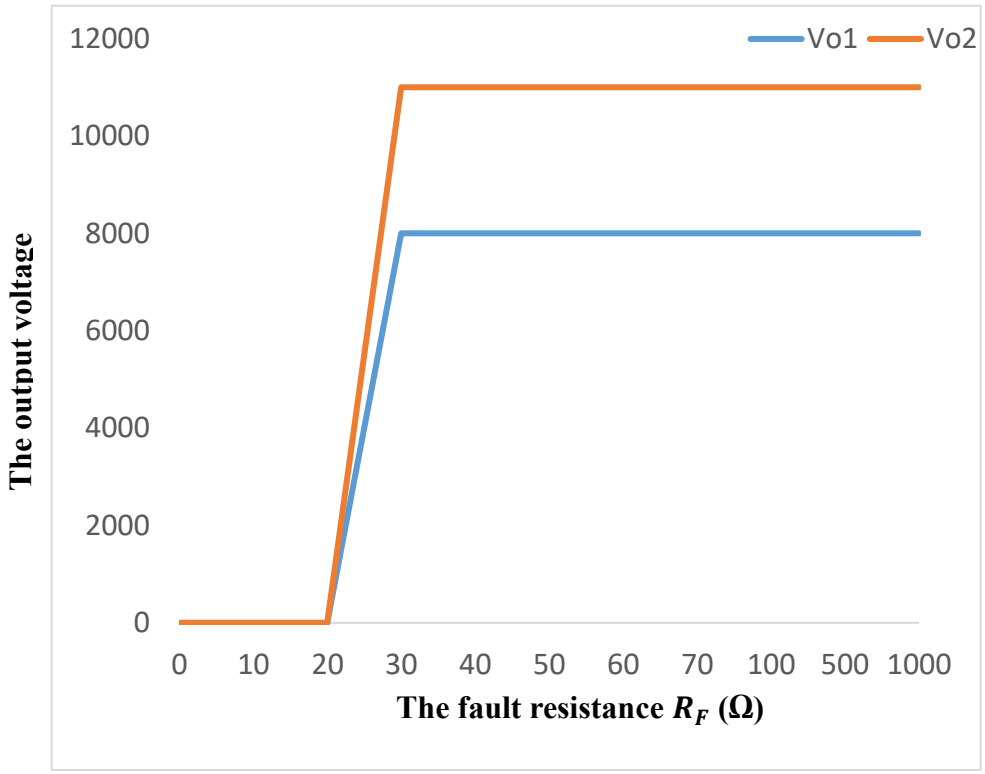


Figure 5.42 the relation between the SC non-solid fault resistance $R_F$across S_{o1} or S_{o2} and its corresponding output voltages V_{o1} and V_{o2}

The effect of fault resistance values on the amplitude of the output voltages of the considered example (three-input two-output) of the proposed DC transformer are summarised in tables 5.14.

Table 5.14 Short Circuit (SC) non-solid fault resistance ($R_F > 0$)across the transistors $S_{o1}$and S_{o2}

Table 5.14.A. SC non-solid fault resistance across the transistor S_{o1}

Fault resistance across S_{o1} (R_F) (Ω)	**Output voltage V_{o1} (Volts)**	**V_{o1} Peak-to-peak ripple voltage (Volts)**	**Output voltage V_{o2} (Volts)**	**V_{o2} Peak-to-peak ripple voltage (Volts)**
zero	zero	Zero	zero	zero
10	zero	Zero	zero	zero
20	zero	Zero	zero	zero
30	8000	360	11000	55
40	8000	40	11000	40
50	8000	35	11000	40
60	8000	30	11000	40
.				
.				
.				
.				
1000	8000	30	11000	40

Table 5.14.B. SC non-solid fault resistance across the transistor S_{o2}

Fault resistance across S_{o2} (R_F) (Ω)	**Output voltage V_{o1} (Volts)**	**V_{o1} Peak-to-peak ripple voltage (Volts)**	**Output voltage V_{o2} (Volts)**	**V_{o2} Peak-to-peak ripple voltage (Volts)**
zero	zero	Zero	zero	zero
10	zero	Zero	zero	zero
20	zero	Zero	zero	zero
30	8000	180	11000	1400
40	8000	100	11000	400
50	8000	24	11000	40
60	8000	24	11000	40
.				
.				
.				
.				
1000	8000	24	11000	40

Study of tables 5.14 indicate that the magnitude of output voltages i.e. V_{o1}, V_{o2} depend on the value of the fault resistance. This in turn will change the error of the closed loop PID controller from its normal operation. Furthermore, the 30Ω is the minimum value of the fault resistance that the closed loop PID controller can handle the error and adapts its normal operation. It has been reported in [150] that the control action becomes more unstable as the process output deviates from the set point further.

The simulation results of the output voltages V_{o1}, V_{o2} under SC non-solid fault with $R_F = 30\Omega$ across the output transistors S_{o1}, S_{o2} are shown in figures 5.43.a, 5.43.b, 5.44.a and 5.44.b.

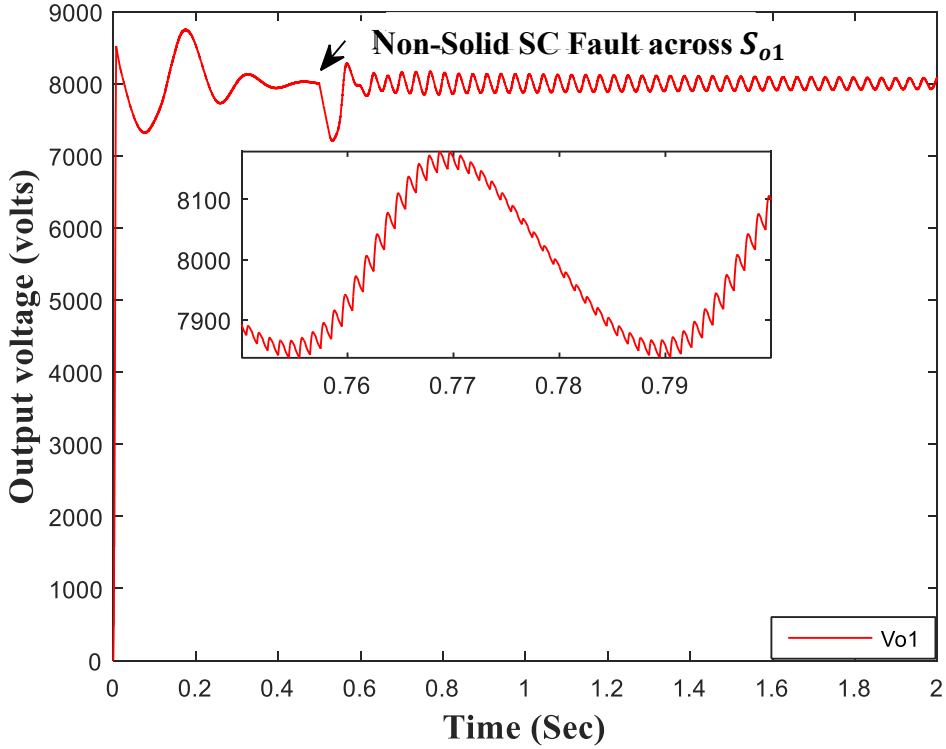


Figure 5.43.a. the output voltage response curve V_{o1} due to a SC non-solid fault ($R_F = 30\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o1})

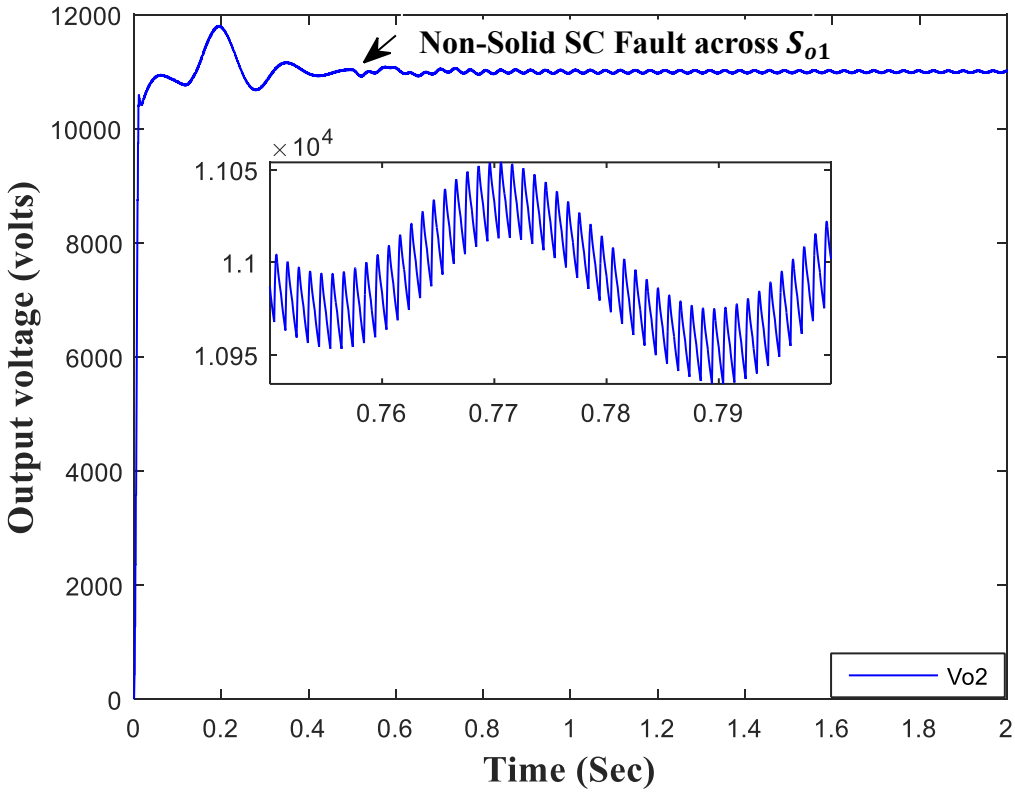


Figure 5.43.b. the output voltage response curve V_{o2} due to a SC non-solid fault ($R_F = 30\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o1})

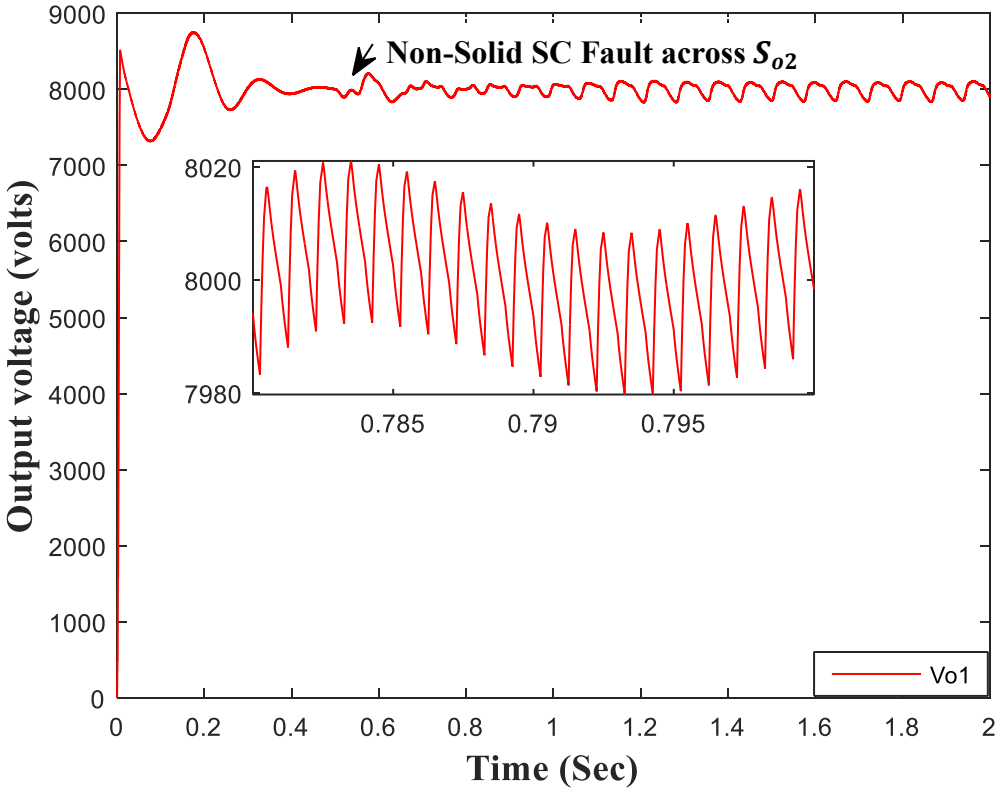


Figure 5.44.a. the output voltage response curve V_{o1} due to a SC non-solid fault ($R_F = 30\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o2})

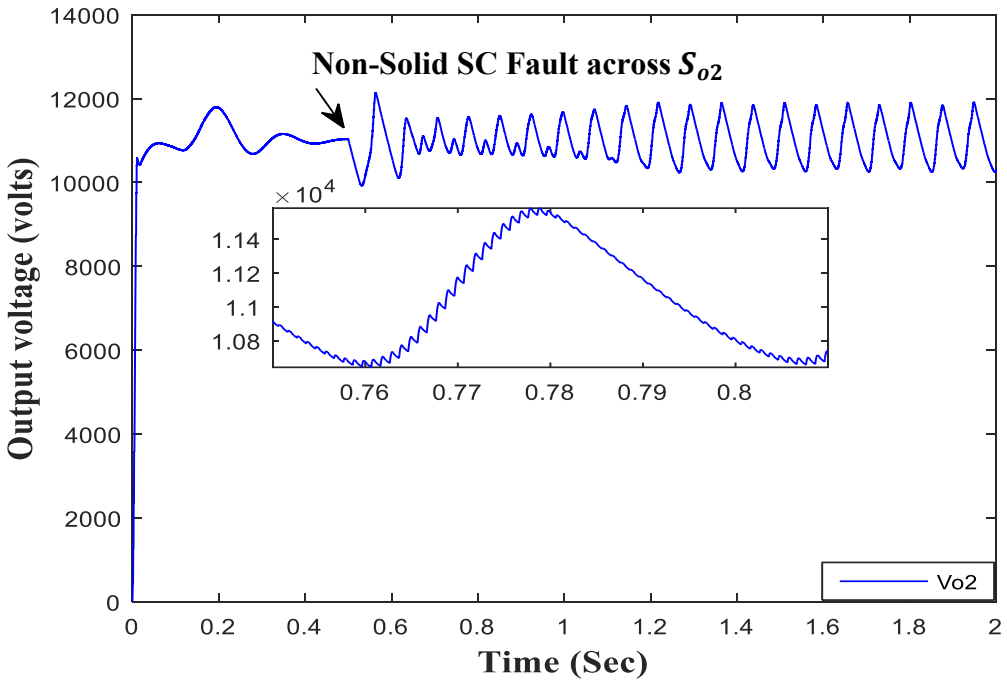


Figure 5.44.b. the output voltage response curve V_{o2} due to a SC non-solid fault ($R_F = 30\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o2})

- **Short Circuit (SC) transistor with non-solid fault ($R_F > 100\Omega$) on the output side of the proposed DC transformer**

Here the short circuit non-solid fault simulations are carried out for fault resistance between the following ranges.

$$100\ \Omega < R_{F-High} < 1000\ \Omega$$

Where $R_{F-High}$is the high fault resistance.

To demonstrate the effect of the above ranges as illustrated in table 5.14, the results (outputs voltage V_{o1}, V_{o2}) obtained with two fault resistances i.e. ($100\ \Omega$ across S_{o1} and $140\ \Omega$ across S_{o2}) are shown in figures 5.45 and 5.46. As these resistances are the minimum fault resistance values where their corresponding closed loop controller starts to be more stable during the occurrence of their switches SC faults. In this case the fault duration is $0.5\ mSec$ and the system recovers within 0.179 after the fault cleared.

It is known that if the fault occurs across the output transistors e.g. S_{o1} when the transistor is ON, R_{ON} is much smaller than the fault resistance (R_F) and hence the current will pass through the transistor branch and the output will be disconnected from the source side. However, if the fault occurs across the output transistors e.g. S_{o1} when the transistor is OFF, due to high resistance of the transistor, the voltage across the transistor will depend on the fault resistance value since it is connected in parallel with the transistor. It is found that at higher fault resistance value, error in the closed loop is lower and the PID controller could adapt and reduce the steady state error.

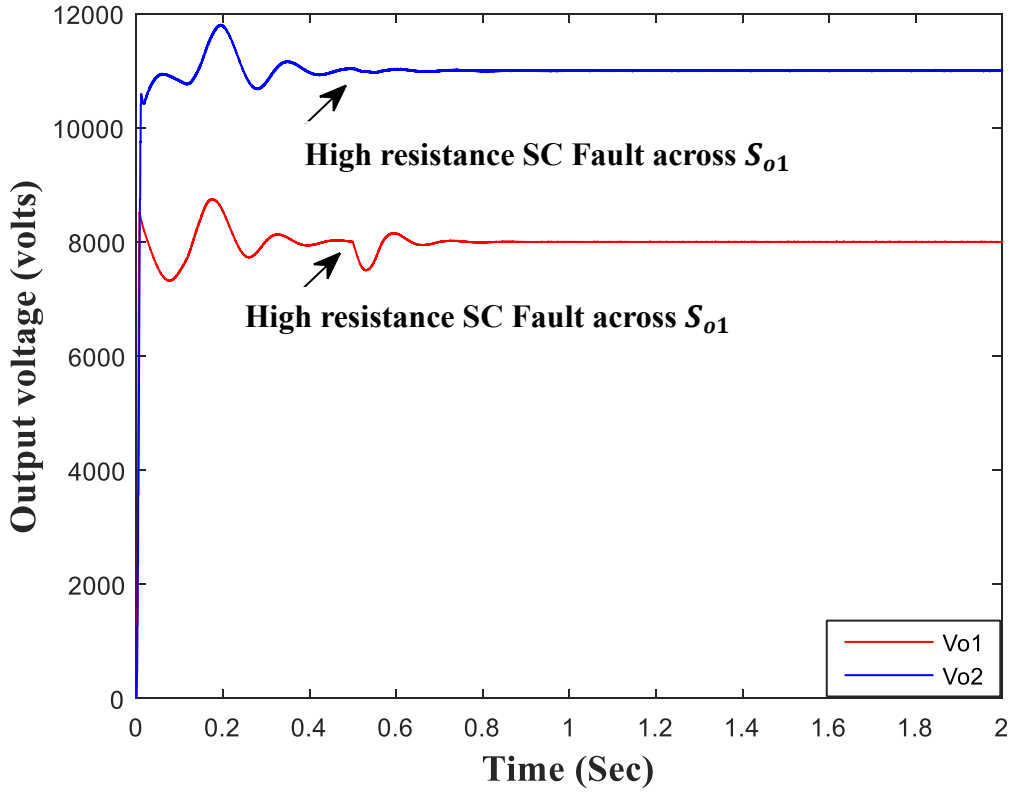


Figure 5.44 the output voltages response curves V_{o1}, V_{o2} due to a SC non-solid high fault ($R_F = 100\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o1})

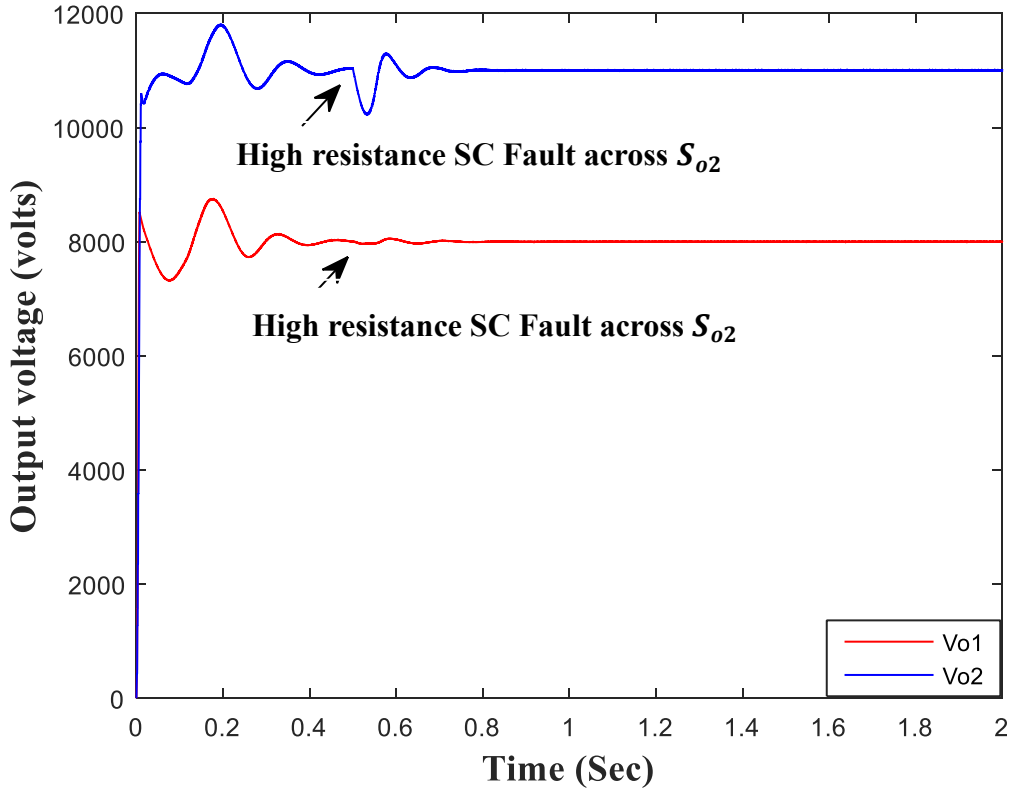


Figure 5.45 the output voltages response curves V_{o1}, V_{o2} due to a SC non-solid high fault ($R_F = 140\ \Omega$) at $t = 0.5\ Sec$ for duration of $5m\ Sec$ acquired on switching power (S_{o2})

5.5.3.2.Open Circuit (OC) faults across the Diodes

The Open Circuit (OC) faults are carried out on the considered example (three-input two-output) of the proposed DC transformer. Since the considered example has five diodes as illustrated in table 5.13.B, hence five tests are simulated and in each test the characteristics of the output voltages are monitored. In general, when the input stage diodes are OC the DC output voltage is isolated from the source. Hence, a significant decrease in the inductor current is observed. When the transistor is ON, the source current cycles through the transistor, once the transistor turns OFF the current drawn from the source collapses to nearly to zero. Then a high voltage spike is observed across the transistor and the OC diode. And these high voltage spikes could damage the power switching components in the DC transformer. Figure 5.46 shows the voltage across the transistor (S_{o1}) when OC fault occurred across $Diode_{o1}$ at $t = 0.8\,Sec$.

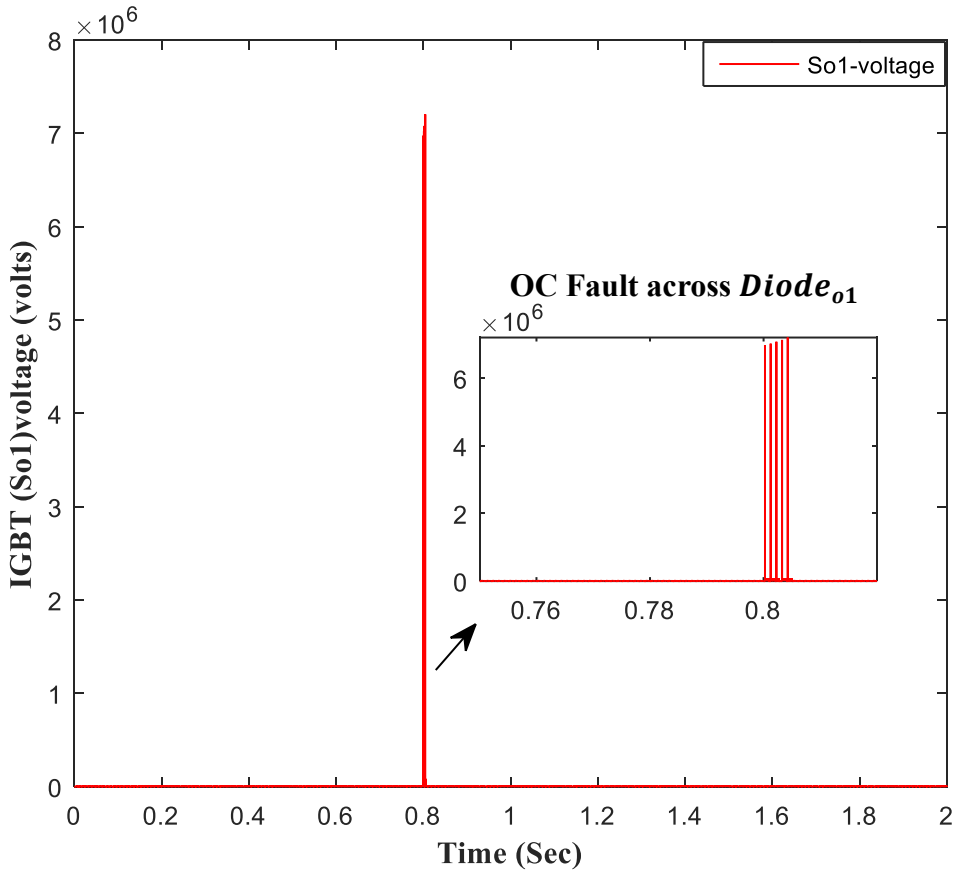


Figure 5.46 the IGBT switch (S_{o1}) voltage response curve due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{o1}$

These faults occur across the diodes at $t = 0.8\,Sec$ for short period of time where the fault time $t_F = 0.5\,m\,Sec$. The simulation results are shown graphically in figures 5.47 to 5.56.

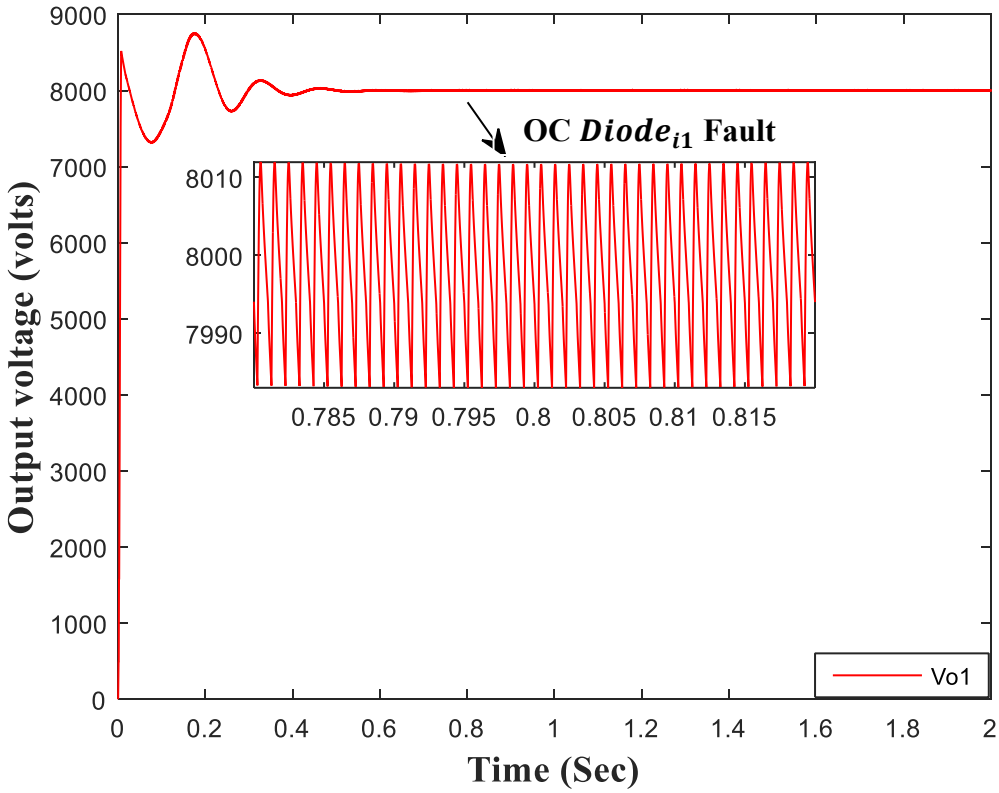


Figure 5.47 the output voltage response curve V_{o1} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i1}$

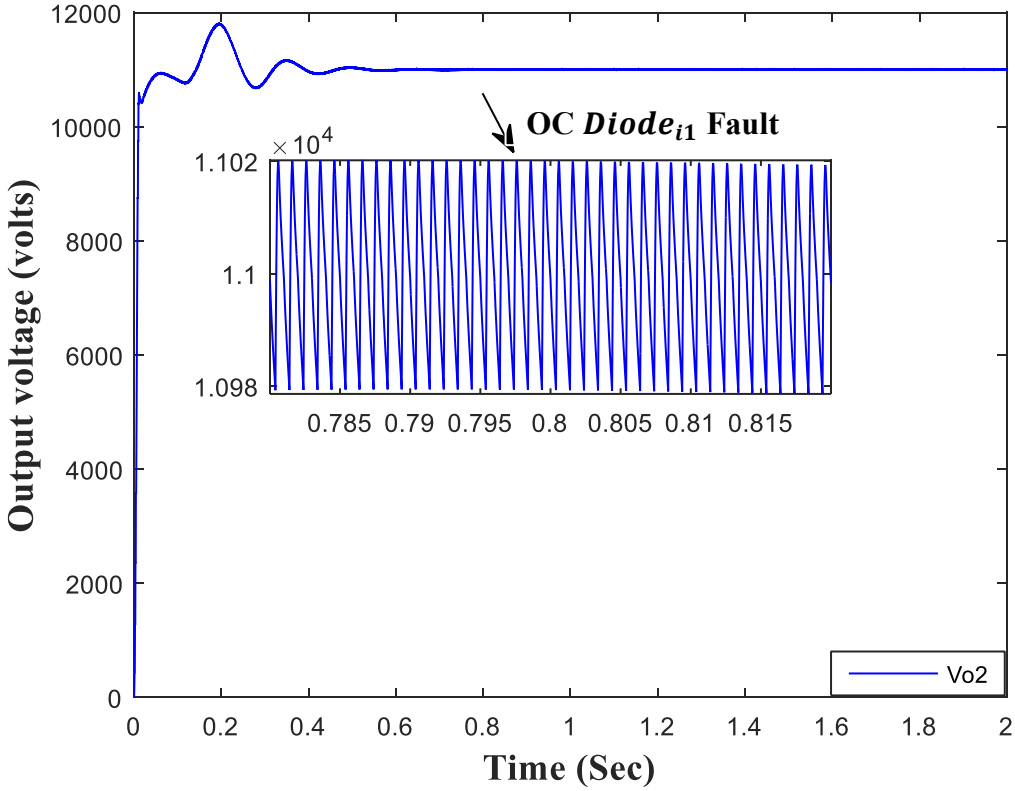


Figure 5.48 the output voltage response curve V_{o2} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i1}$

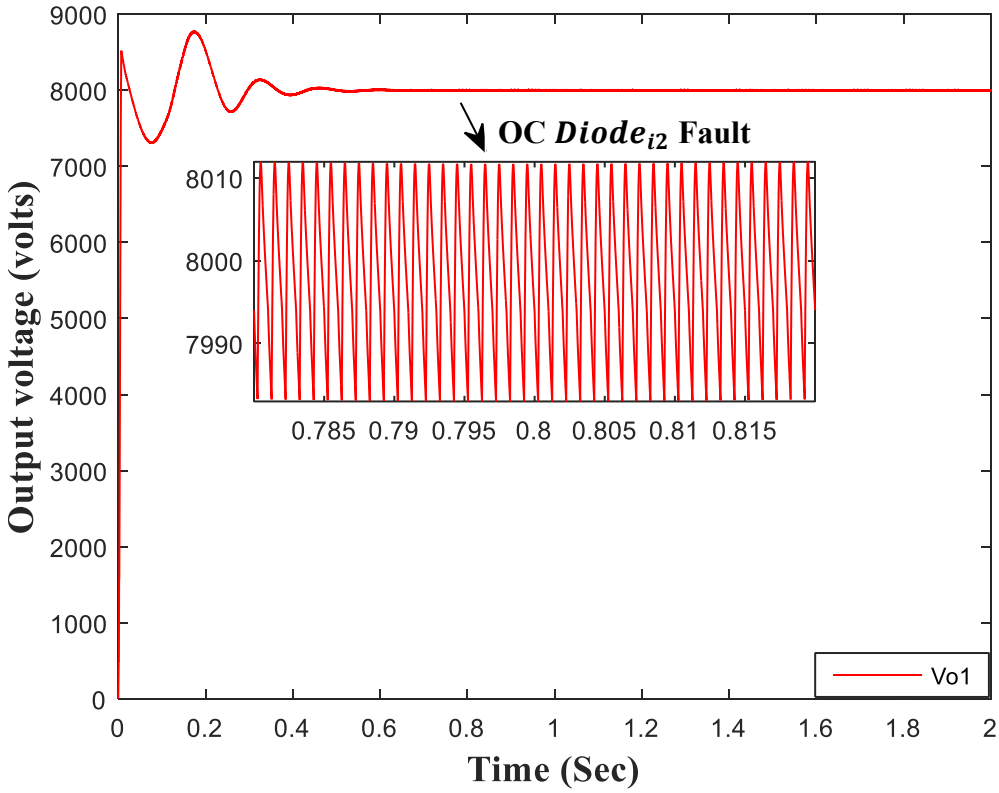


Figure 5.49 the output voltage response cure V_{o1} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i2}$

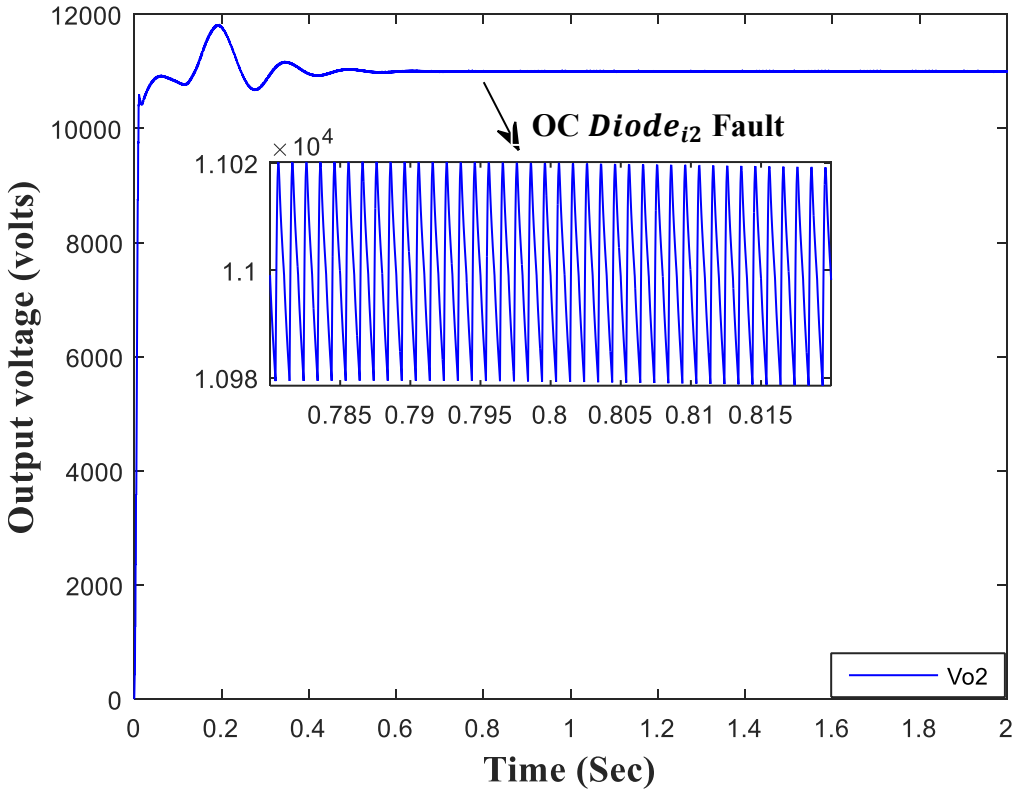


Figure 5.50 the output voltage response curve V_{o2} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i2}$

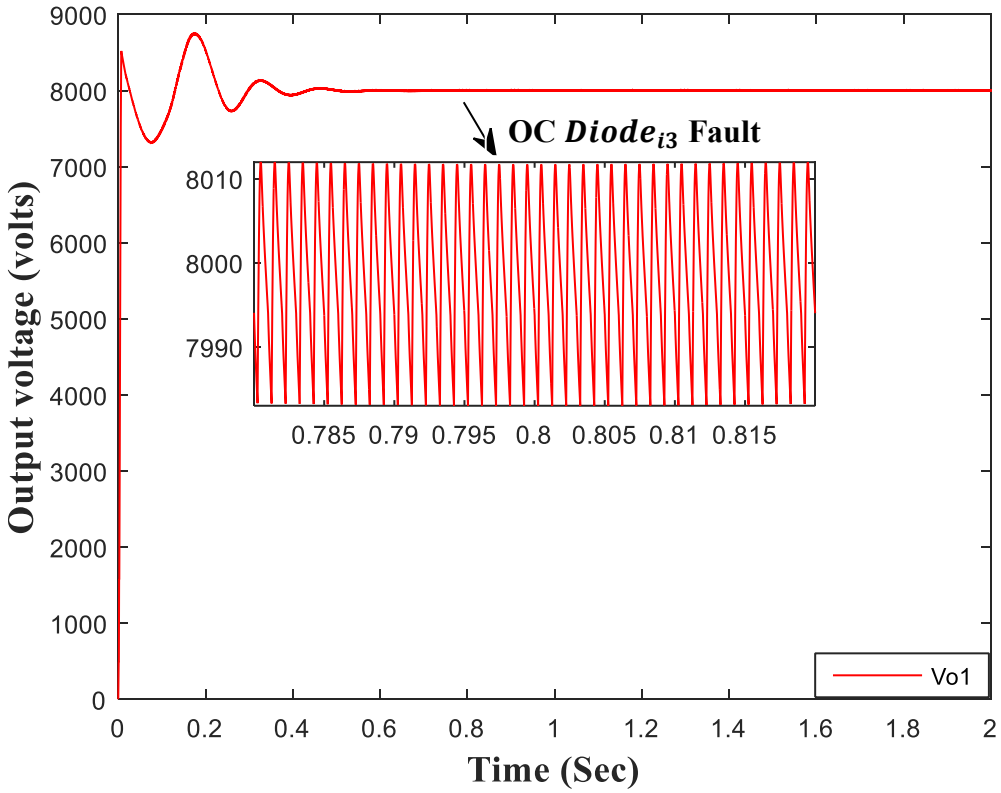


Figure 5.51 the output voltage response curve V_{o1} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i3}$

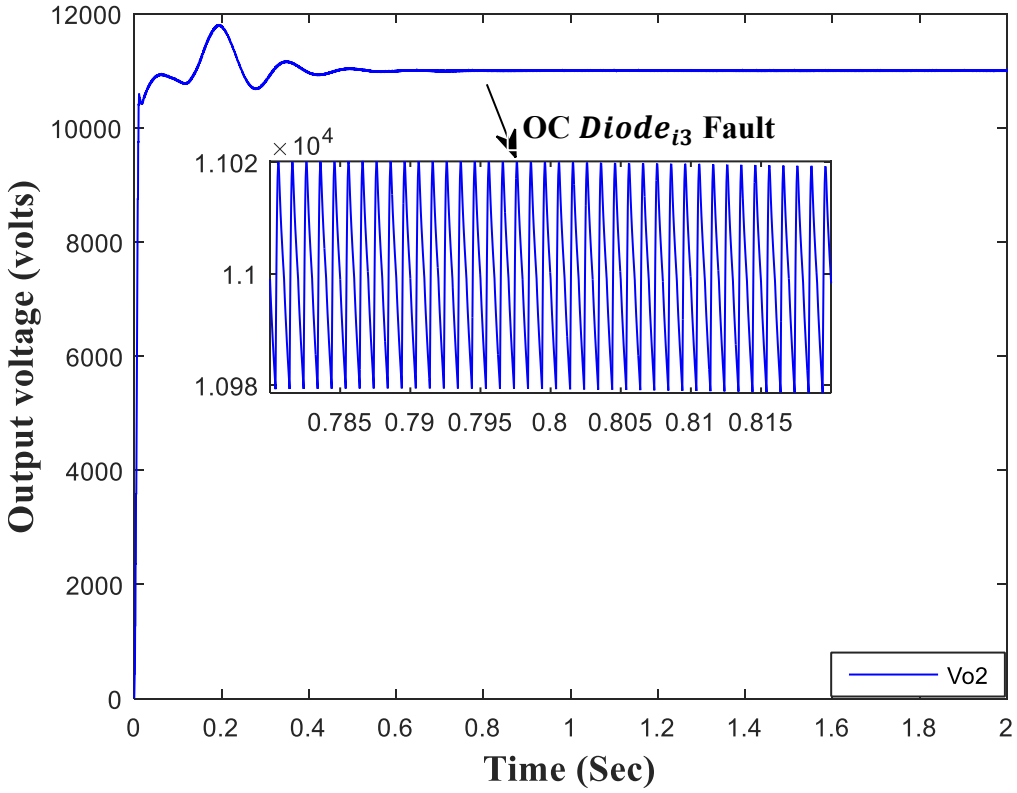


Figure 5.52 the output voltage response curve V_{o2} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{i3}$

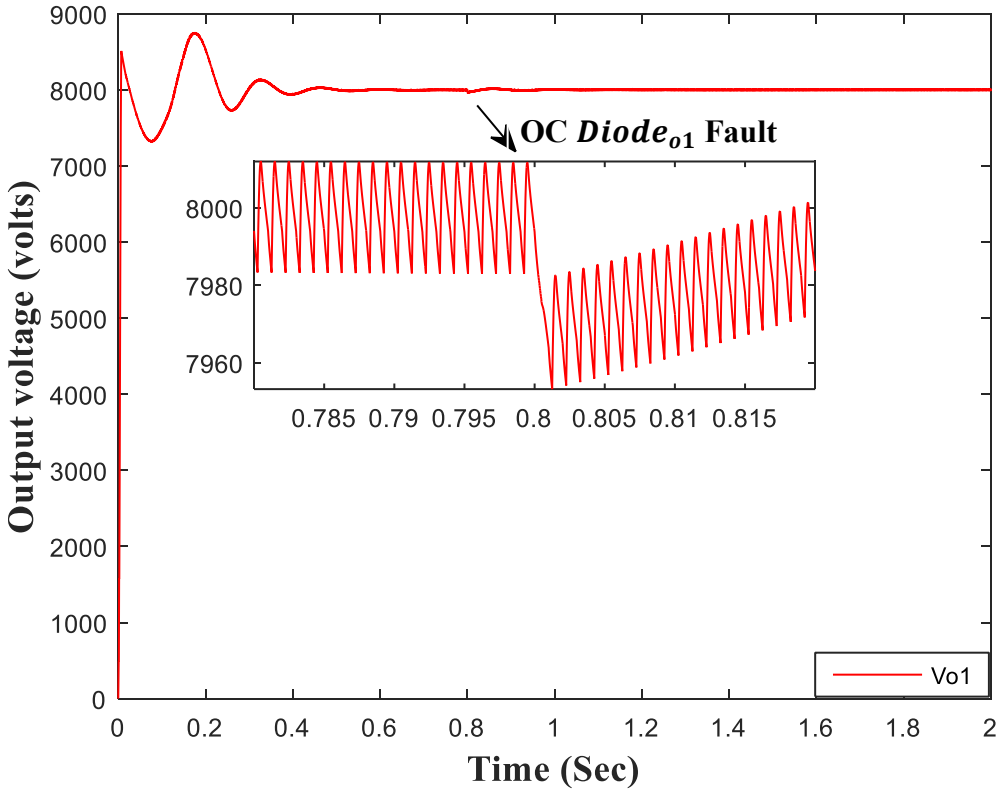


Figure 5.53 the output voltage response curve V_{o1} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{o1}$

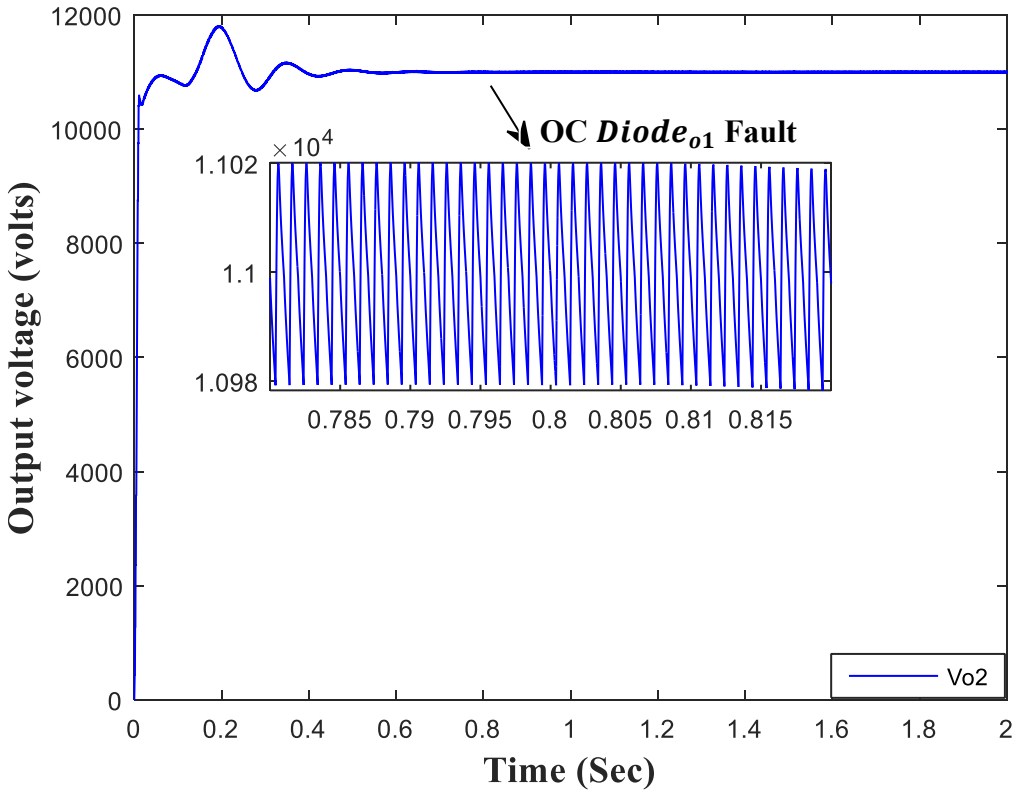


Figure 5.54 the output voltage response curve V_{o2} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{o1}$

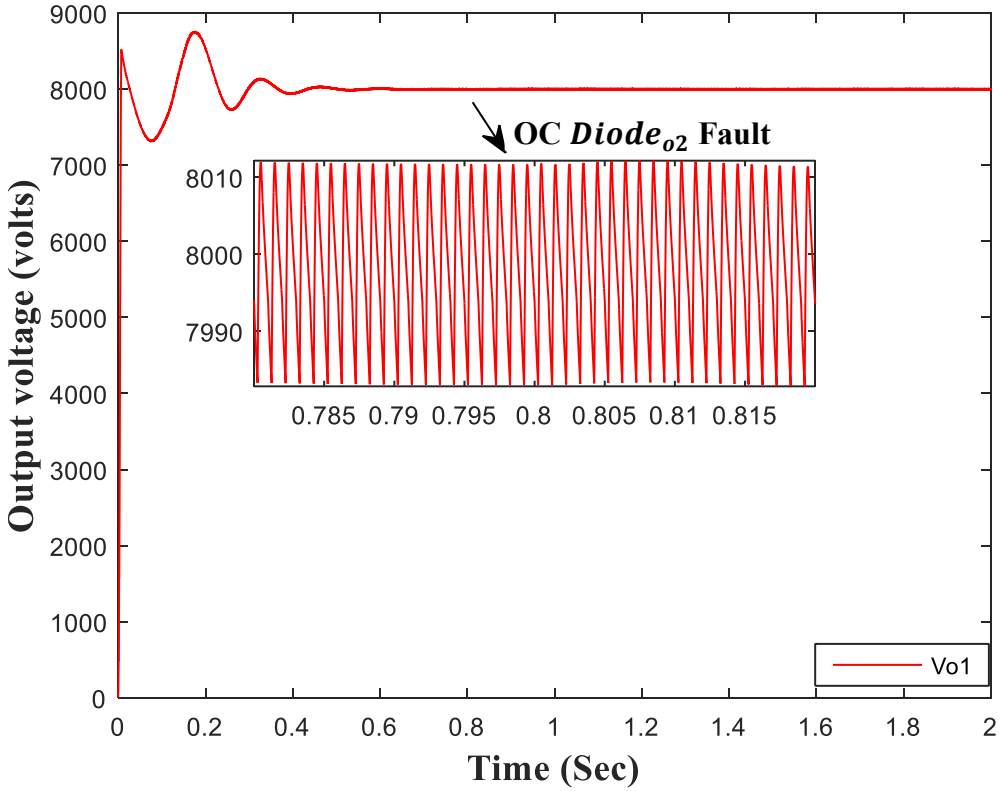


Figure 5.55 the output voltage response curve V_{o1} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{o2}$

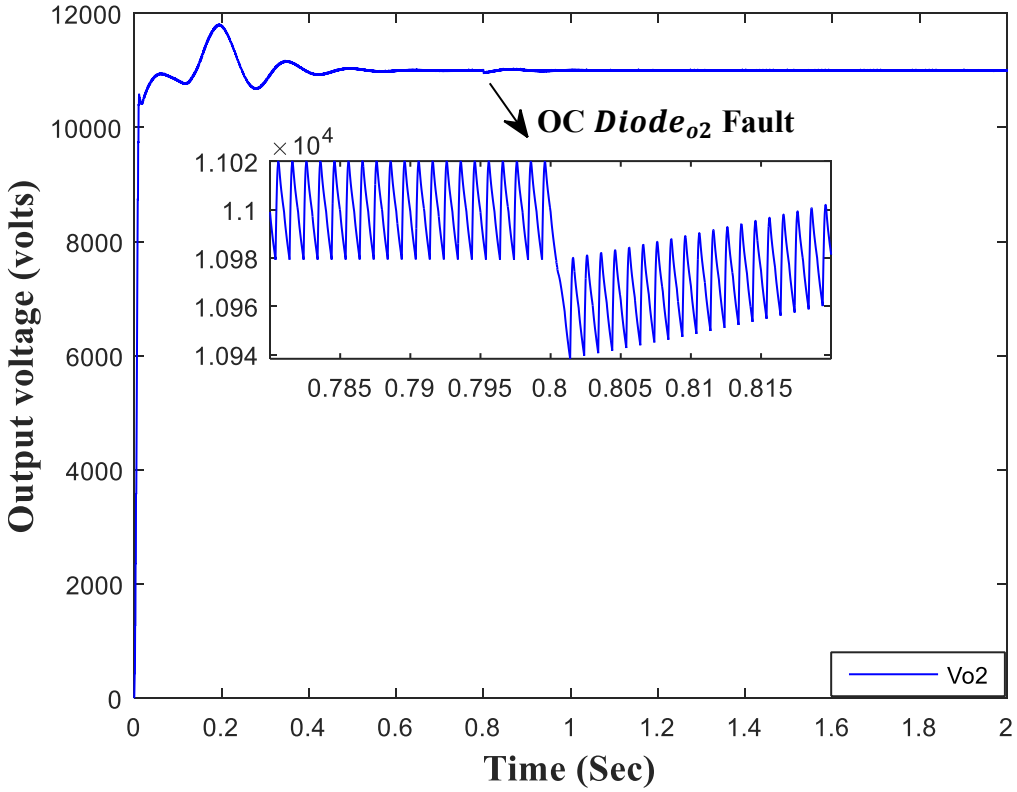


Figure 5.56 the output voltage response curve V_{o2} due to OC fault at $t = 0.8\,Sec$ for duration of $5m\,Sec$ acquired across $Diode_{o2}$

Analysis of figures 5.47 to 5.56 reveal that if the OC fault occurs on the input side diodes, V_{o1}, V_{o2} perform well without any changes. However, ripple could be observed within $V_{o1}$and V_{o2} waveforms if the OC fault occurs on diodes situated on the output side of the proposed DC transformer and the system recovers after a short period of time($i.e. 0.015\ Sec$). For example, if OC fault occurs in $Diode_{o1}$, the peak-to-peak ripple voltage in V_{o1} is $27\ V$ and in V_{o2} is slightly lower (i.e. $25\ V$) . But, if OC fault occurs in $Diode_{o2}$, then the peak-to-peak ripple voltage in V_{o1} is $40\ V$ and in $V_{o2} = 50\ V$.

5.6 Summary

In this chapter, the modelling and control algorithm of the proposed Multi-Input Multi-Output (MIMO) step-up DC transformer have been discussed. Where Proportional Integral Derivative (PID) controllers have been designed and integrated to control and operate the proposed DC transformer in Continuous Conduction Mode (CCM) utilising the concept of closed loop Voltage Mode Control (VMC). The DC transformer can integrate different energy sources for provision of different output voltage levels. The advantage of energy sources integration is that the required output voltage levels could be made up from a range of sources based on the availability and choice.

As the proposed MIMO DC transformer is a non-linear plant, hence Small Signal Modelling (SSM) and linearization of the plant is required to obtain a linear model for ease of analyse and to achieve a more stable and regulated output voltage. A comprehensive design of the proposed transformer control system requires a comprehensive knowledge of the transformer structure and its operational principles. In order to obtain the SSM of the plant to be controlled, the mathematical modelling and the state space representation in a matrix form of the proposed DC transformer have been derived within the transformer's switching states. This yields to the transfer functions presentation of the designed transformer. High order transfer functions that are needed for the proposed DC transformer will further complicate the analysis of the designed controller, as the number of the transformer's inputs\outputs increases the complexity of controller increases too. Thus, integration of the PID controllers is introduced in order to simplify the controller design as well as the possibility to add more inputs\outputs without redesigning the whole control. And also, PID controller is a well proven controller.

To determine the stability of the system consisting of identical or semi identical subsystems it is necessary to analyse the stability of each subsystem. Then the system will be stable if

all subsystems are stable and if any subsystem is unstable this leads the whole system to instability. As the proposed transformer is constructed from connected number of modules (subsystems) the stability analysis has been carried out for each module.

The stability analysis of the proposed MIMO DC transformer is done through transfer function approach. Phase margin and gain margin are obtained by plotting the bode plot of each subsystem's transfer function which defines the stability of the system. To maintain a balance between the stability and transient behaviour a stable rule design for PID controller tuning is proposed using Routh-Hurwitz stability criterion. The effectiveness of this approach has been examined via simulations with different cases. The bode plot and the pole-zero map have been used as a tool to define the system's stability.

The validity of the DC transformer's control performance is demonstrated through MATLAB\SIMULINK software simulation under different scenarios depending on the utilisation of the input sources. When one of the input sources is not available or when the demand changes in the system the controller automatically adapts and changes the duty ratio of the power switch in order to get the desired output voltage. The results verify the flexibility and robustness of the designed controller under demand and supply variations. It also proves the controller's adaptive ability to adjust so as to ensure the system produces the desired output voltage level and to adjust when any changes are required by the system in order to have the desired output voltage level by controlling the ON and OFF time of the power switches.

Improvement in the output response curve V_o has been acquired by designing (RC) LPF. The convenient time constant value has been selected and the values of R and C have been sized in order to remove the unwanted oscillations as well as to reduce the effect of the high peak spike when one of the input sources is not available in the system by almost 84%.

The performance of the proposed DC transformer under faulty conditions has been examined. Different fault modes have been considered within the simulations. Here fault conditions are classified as the Short Circuit (SC) and the Open Circuit (OC) faults of transistors and diodes consequently. During each simulation only occurrence of one fault is considered with different fault resistance values.

To conclude, the controlled DC transformer achieves a constant $8\,kV, 11\,kV$ for the two outputs from three different DC input sources at an operating frequency of $1\,kHz$ and the results prove the effective integrated operation of input sources which will provide a reliable

and flexible system, as well as the simplicity of designing the adaptive and robust controller to achieve a constant DC output voltage in different scenarios when the inputs or the load change.

CHAPTER SIX

EVALUATION OF THE DESIGNED MIMO DC TRANSFORMER

6.1 Evaluation and comparison of existing published MIMO DC transformers

The step-up DC transformers can be categorized into two main groups, namely: isolated and non-isolated [154], [155]. Isolated DC transformers present galvanic isolation and high voltage gain, but due to the application of a transformer, they have low efficiency, bulky and costly [156]. On the other hand, the non-isolated ones have simpler structure and higher efficiency, with lower size and cost. But these types usually have lower voltage gains [157].

The literature has reported on various non-isolated step-up DC transformer topologies with deferent voltage boosting techniques, in which the passive components incorporated with the semiconductors (switches and diodes) are connected and utilised in the circuit.

In order to evaluate the designed MIMO DC transformer a comprehensive review to classify various step-up DC transformers based on the number of inputs\outputs, number of components, application of the design, and their conversion gain will be presented and summarised in this section.

As yet little work has been carried out on the design of MIMO DC transformer. However, the review of the published topologies to date has led the author to categorise the existing designs into four main groups based on the number of inputs\outputs as presented in the tables from 6.1 to 6.4.

Table 6.1 SISO step-up DC transformer topologies

The reference of the presented topology	Title	Year	Number of inputs and outputs	Number of components	Relation between the input and the output	Applications
[160]	Novel High efficiency DC-DC Boost Converter for using in Photovoltaic systems	2015	(1) Input and (1) output	Internal transformer, (3) Inductors, (4) Capacitors, (1) Switches and (2) Diodes	$V_o = \frac{nV_{i1}}{(1-D)}$ Where $n = \frac{N_2}{N_1}$ n is the transformer's turns ratio	For Photovoltaic Systems
[163]	A Novel Transformer-less Adaptable Voltage Quadrupler DC Converter with low switch Voltage stress	2014	(1) Input and (1) output	(2) Inductors, (4) Capacitors, (2) Switches and (4) Diodes	$\frac{V_o}{V_i} = \frac{4}{(1-D)}$	For applications requiring high Step-Up voltage gain
[52]	Ultra-step-up DC-DC converter with reduced switch stress	2010	(1) Input and (1) output	(2) Inductors, (4) Capacitors, (1) Switch and (5) Diodes	$\frac{V_o}{V_i} = \frac{(3+D)}{(1-D)}$	For providing a high voltage gain
[165]	Hybrid switched inductor converters for high step-up conversion	2015	(1) Input and (1) output	(3) Inductors, (1) Capacitor, (2) Switches and (4) Diodes	$\frac{V_o}{V_i} = \frac{(1+2D)}{(1-D)}$	Fuel cell applications
[166]	High voltage gain interleaved DC boost converter application for photovoltaic generation system	2013	(1) Input and (1) output	(4) Inductors, (2) Capacitors, (4) Switches and (4) Diodes	$\frac{V_o}{V_i} = \frac{(1+D)}{(1-D)}$	photovoltaic generation system
[167]	A high voltage ratio and low stress DC/DC converter with reduced input current ripple for fuel cell source	2014	(1) Input and (1) output	(2) Inductors, (4) Capacitors, (1) Switch and (3) Diodes	$\frac{V_o}{V_i} = \frac{2}{(1-D)}$	Renewable energy systems and fuel cell applications

Table 6.2 DIDO step-up DC transformer topologies

The reference of the presented topology	Title	Year	Number of inputs and outputs	Number of components	Relation between the input and the output	Applications
[156]	A non-isolated Multi-Input Multi-Output DC-DC Boost Converter for different voltage requirements	2016	(2) Input and (2) output	(1) Inductor, (2) Capacitors, (4) Switches and (4) Diodes	The general relation is not considered but via simulation the conversion ratio: $\frac{V_{o1}}{V_1} = 2.28$ And $\frac{V_{oT}}{V_2} = 2.5$	Renewable energy sources
[157]	Dual Input Dual Output Single switch DC-DC Converter for renewable energy Applications	2016	(2) Input and (2) output	(3) Inductors, (2) Capacitors, (1) Switches and (3) Diodes	Symmetrical outputs (1) switch $V_{o1} = V_{o2}$ $V_o = \frac{2D}{(1-D)} V_i$	Renewable energy applications
[162]	A Transformer-less Multi-Input Multi-Output DC-DC Boost Converter using Fuzzy logic Controller for Electric Vehicle applications	2015	(2) Input and (2) output	(1) Inductors, (2) Capacitors, (4) Switches and (4) Diodes	The general relation is not considered	Low voltage applications and Electric vehicles

Table 6.3 MISO and SIMO step-up DC transformer topologies

The reference of the presented topology	Title	Year	Number of inputs and outputs	Number of components	Relation between the input and the output	Applications
[1]	An Improved Structure for Multi-Input high Step-Up DC-DC Converters	2017	(n) Input and (1) output	$(n+1)$ Inductors, $(n+1)$ Capacitors, $(n+1)$ Switches and $(n+1)$ Diodes	$V_o = \frac{V_1}{(1-D_1)^2} + \sum_{i=2}^{n} \frac{V_i}{(1-D_i)}$	For high voltage gain applications
[152]	A new Multi-Input Step-Up Converter for Hybrid energy Systems	2017	(n) Input and (1) output	(n) Inductors, $(2n-1)$ Capacitors, (n) Switches and $(2n-1)$ Diodes	$V_o = \sum_{j=1}^{n} \frac{V_j}{(1-D_j)}$	For hybrid energy systems
[158]	Single Stage Multi-Input DC-DC/AC Boost Converter with Sliding Mode Control	2016	(2) Input and (1) output	(4) Inductors, (4) Capacitors, (4) Switches and (2) Diodes	$V_o = \frac{V_1}{(1-D_1)} - \frac{V_2}{(1-D_2)}$	Renewable energy sources
[89]	A Bidirectional Multiple-Input Multiple-Output Modular Multilevel DC-DC Converter and its Control Design	2016	(1) Input and (3) output	(3) Inductors, (4) Capacitors, (6) Switches and No Diodes	The general relation is not considered with respect to the duty cycle but the conversion ratio: $\frac{V_{c1}}{V_1} = 2.5$ $\frac{V_{c2}}{V_1} = 3.75$ And $\frac{V_{c3}}{V_1} = 5$	Utilised in both low and high power applications
[11]	Multi-Input Step-Up Converters based on the Switched-Diode-Capacitor Voltage Accumulator	2016	(2) Input and (1) output	(2) Inductors, (5) Capacitors, (2) Switches and (5) Diodes	Parallel configuration: $V_o = \frac{3V_{i1}}{(1-D)} = \frac{3V_{i2}}{(1-D)}$ Series configuration: $V_o = \frac{2V_{i1} + 2V_{i2}}{(1-D)}$	High voltage gain applications

[42]	Modelling of multi-input DC/DC converter for renewable energy sources	2014	(2) Input and (1) output	(2) Inductors, (1) Capacitor, (4) Switches and (4) Diodes	$V_o = \frac{1}{(1-D)}(V_{i1} + V_{i2})$	Renewable energy sources (wind, solar)
[29]	Testing of a new DC/DC converter topology for integrated wind-photovoltaic generating system	1993	(2) Input and (1) output	(2) Inductors, (2) Capacitors, (2) Switches and (3) Diodes	The general relation is not considered	PV-wind generating system
[34]	New DC/DC converter for energy storage system interfacing in fuel cell hybrid electric vehicles	2007	(2) Input and (1) output	(2) Inductors, (1) Capacitor, (3) Switches and (3) Diodes	$V_o = \frac{1}{(1-D_1)}V_1 + \frac{1}{(1-D_2)}V_2) + \frac{1}{(D_1+D_2)-1}V_3$	Fuel cell vehicles
[62]	Multi- output DC/DC converters based on diode-clamped converters configuration: topology and control strategy	2010	(1) Input and (n) output	(1) Inductor, (n) Capacitors, $(n+1)$ Switches and (n) Diodes	The general relation is not considered	Low and high power applications
[153]	Principle and Topology Synthesis of Integrated Single-Input Dual-Output and Dual-Input Single-Output DC-DC Converters	2017	(1) Input and (2) output	(2) Inductors, (2) Capacitors, (2) Switches and (1) Diode	$\frac{V_{o1}}{V_1} = \frac{1}{(1-D_1)}$ And, $\frac{V_{o2}}{V_1} = \frac{D_1+D_2-1}{(1-D_1)}$	For applications required integrated inputs or outputs

Table 6.4 MIMO step-up DC transformer topologies

The reference of the presented topology	Title	Year	Number of inputs and outputs	Number of components	Relation between the input and the output	Applications
[155]	Modelling and Simulation of Photovoltaic system Fed two Input two Output DC-DC Boost Converter Interfaced with asymmetric Cascaded H-Bridge Multilevel Inverter	2017	(m) Input and (m) output	(1) Inductor, (m) Capacitors, $(2m-1)$ Switches and $(2m-1)$ Diodes	The general relation is not considered but via simulation for two inputs two output the conversion ratio: $\frac{V_{o1}}{V_1}=3.3$ And $\frac{V_{o2}}{V_2}=1.11$	Renewable power systems, Aerospace power systems and Hybrid energy vehicle
[159]	Structure for Multi-Input Multi-Output DC-DC Boost Converter	2016	(n) Input and (m) output	(1) Inductor, $(2m)$ Capacitors, $(n+1)$ Switches and $(n+1+2m)$ Diodes	$\frac{V_o}{V_i}=\frac{m}{(1-D_{n+1})}$ where V_o and V_i are the average values of the output and input voltages, respectively	Renewable energy sources
[164]	Innovative DC-DC Converter for Hybrid energy sources using Multi-Inputs	2015	(m) inputs and (n) outputs	(1) Inductor, (n) Capacitors, $(m+n)$ Switches and $(m+n)$ Diodes	The general relation is not considered with respect to the duty cycle but the conversion ratio via simulation for two inputs two output: $\frac{V_{o1}}{V_1}=2.28$ $\frac{V_{oT}}{V_2}=2.5$	Renewable energy sources

[90]	A Non-isolated multi-input multi-output DC/DC boost converter for electric vehicle applications	2014	(m) inputs and (n) outputs	(1) Inductor, (n) Capacitors, $(m+n)$ Switches and $(m+n)$ Diodes	The general relation is not considered with respect to the duty cycle but the conversion ratio via simulation for two inputs two output: $\frac{V_{o1}}{V_1} = 2.28$ $\frac{V_{oT}}{V_2} = 2.5$	Electric Vehicle applications

As the proposed topology designed for medium to high voltage application then the transformer's voltage conversion gain is the main characteristic of the design. Hence among the topologies shown in the aforementioned tables only, the topology presented in [11] that uses a switched-diode-capacitor as a boosting technique and the topology presented in [1] that uses a multi-stage or multi-level as a boosting technique are selected for the comparative analysis with the proposed step-up MIMO DC transformer design; as these topologies have high step-up conversion gain in comparison with the other topologies mentioned in the previous tables. The in-depth analysis is discussed in the next section of this chapter.

6.2 Evaluation and comparison of the proposed MIMO DC transformer with the selected published DC transformers

In this section, a comparison of required devices, performance, manufacturing cost and flexibility of the proposed design and those presented in [1] and [11] have been discussed.

6.2.1 Comparative analysis of the proposed topology with the selected published topologies

For the purpose of simplicity in comparison, it is assumed that the selected topologies of [1], [11] and the proposed topology have a double input single output. Hence, three models will be constructed for simulation. Figure 6.1 shows the block diagram of the chosen topologies to be analysed using MATLAB\SIMULINK software.

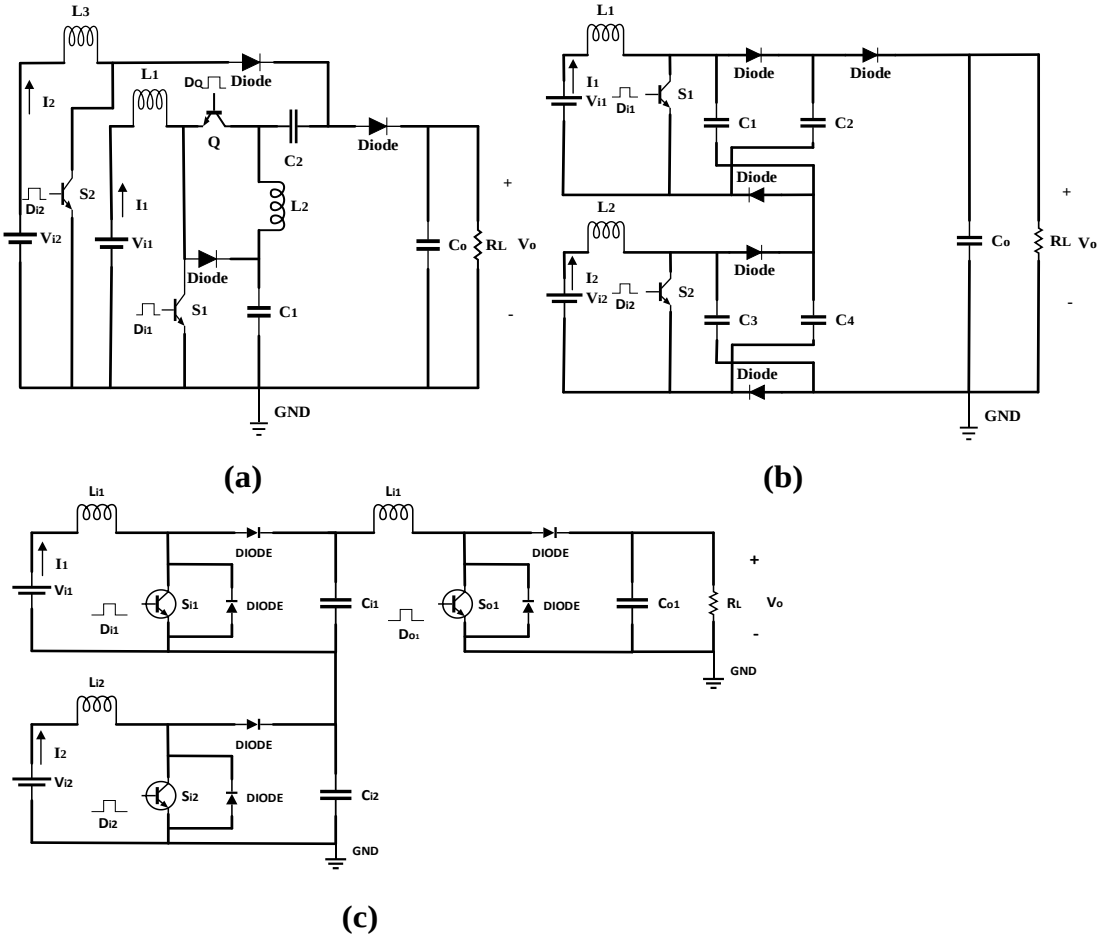


Figure 6.1 the block diagram of the proposed topology and those presented in [1] and [11].

For the three models, the passive components have been sized based on the following requirements:

$$V_{i1} = V_{i2} = 330\ V$$

$$V_o = 11\ kV$$

$$f_s = 1\ kHz$$

$$R_L = 1\ k\Omega$$

According to this $L\ and\ C$ of the selected topologies could be found as follows:

- **Topology presented in [11]**

$$V_{c1} = V_{c2} = 2750\ V$$

$$V_{c3} = V_{c4} = 2750\ V$$

$$V_o = 2 * V_{c1} + 2 * V_{c3} \tag{6.1}$$

$$V_o = 2 * V_{c1} + 2 * V_{c3} = 11\ kV$$

For $D_{i1} = D_{i1} = D$

$$V_o = \frac{2}{(1-D)}(V_{i1} + V_{i2}) \tag{6.2}$$

Then the duty ratio D will be

$$D = 0.88$$

To find the inductors values:

$$L_1 = \frac{V_{i1} * D_{i1}}{2\Delta i_{L1} * f_s} \tag{6.3}$$

From the data provided in the published paper [11] the ripple and the average current will be:

$$I_1 = I_2 = \frac{2 * V_o}{(1-D)R_L} \tag{6.4}$$

$$I_1 = I_2 = \frac{2 * V_o}{(1-D)R_L} = 183.3\ A$$

$$\Delta i_{L1,2} = 0.2\frac{V_o}{V_{i1,2}} I_o \tag{6.5}$$

Where $I_o = (1-D)I_{1,2} = 22\ A$

$$\Delta i_{L1,2} = 0.146\ kA$$

Then

$$L_1 = L_2 = \frac{V_{i1} * D_{i1}}{2\Delta i_{L1} * f_s} \tag{6.6}$$

$$L_1 = L_2 = \frac{V_{i1} * D_{i1}}{2\Delta i_{L1} * f_s} = \frac{330 * 0.88}{2 * 10^3 * 0.146 * 10^3}$$

$$L_1 = L_2 = 994.5 * 10^{-6}\ H$$

The capacitors selection:

Based on

$$\Delta V_{C1,2} < 0.05 * V_o$$

$$\Delta V_{C1,2} = 137.5\ V$$

Then C_1 and C_2 will be:

$$C_1 = \frac{V_{C1,2}}{2 * R_L * f_s * \Delta V_{C1,2}} \tag{6.7}$$

$$C_1 = \frac{V_{C1,2}}{2 * R_L * f_s * \Delta V_{C1,2}} = \frac{2750}{2 * 10^3 * 10^3 * 137.5}$$

Due to symmetry in the two inputs then:

$$C_1 = C_2 = C_3 = C_4 = 10\ mF$$

And the output capacitor will be:

$$\Delta V_{Co} = 0.05 * 11000 = 550\ V$$

$$C_o = \frac{V_o}{2 * R_L * f_s * \Delta V_{Co}} \tag{6.8}$$

$$C_o = \frac{V_o}{2 * R_L * f_s * \Delta V_{Co}} = \frac{11 * 10^3}{2 * 10^3 * 10^3 * 550} = 10\ \mu F$$

- **Topology presented in [1]**

For $V_{i1} = V_{i2} = V_i$ and $D_{i1} = D_{i2} = D_Q = D$ the output voltage will be

$$V_o = \frac{(2 - D)}{(1 - D)^2} V_i \tag{6.9}$$

$$V_o = \frac{(2 - D)}{(1 - D)^2} V_i = 11\ kV$$

Then the duty ratio D

$$D = 0.81$$

And

$$V_{C1} = \frac{V_i}{(1-D)} + V_{C2} = 3.46\ kV$$

$$V_{C2} = \frac{V_i}{(1-D)} = 1.73\ kV$$

Hence, C_1 and C_2 will be

$$C_1 = \frac{V_{C1}}{2 * R_L * f_s * \Delta V_{C1}} \tag{6.10}$$

And the capacitor ripple voltage ΔV_{C1}

$$\Delta V_{C1} = 0.05 * 3.46 * 10^3 = 173\ V$$

Then

$$C_1 = 10.5\ \mu F$$

$$C_2 = 5\ \mu F$$

To find the output capacitor C_o

$$C_o = \frac{V_{Co}}{2 * R_L * f_s * \Delta V_{Co}} \tag{6.11}$$

$$C_o = 31.8\ \mu F$$

In order to size the inductors, the following relation will be used

$$L_1 = L_2 = L_3 = \frac{V_i * D}{2\Delta i_L * f_s} \tag{6.12}$$

The inductor ripple current as presented in [1] considered to be $\Delta i_L = 4.95\ A$, this yields to:

$$L_1 = L_2 = L_3 = 27\ mH$$

- **The Proposed Topology**

The DC analysis of the proposed topology have been presented in chapter four, hence the value of L and C have been found as follows:

For $D_{i1} = D_{i2} = D_{o1} = D$ the output voltage will be

$$V_o = \frac{2}{(1-D)^2} V_i \tag{6.13}$$

And

$$V_o = 11\ kV$$

Then through data substitution the duty ratio D will be 0.75 or 75% .

Given the average input inductor current equation as:

$$I_1 = I_2 = \frac{V_{i1} + V_{i2}}{(1-D)^2(1-D_{o1})^2 R_L} \tag{6.14}$$

So, the inductors' value

$$L_{i1} = L_{i2} = 1.92\ mH$$

$$L_{o1} = 91\ mH$$

Similarly, for the voltage expression across C_{i1} or C_{i2} as shown below:

$$V_{Ci1} = V_{Ci2} = \frac{V_i}{(1-D)} = 1.38\ kV$$

Then the capacitors' value is:

$$C_{i1} = C_{i2} = 2.5\ \text{mF}$$

And the output capacitor as previously can be found as:

$$C_{o1} = 25.1\ \mu\text{F}$$

After computation of the passive components for the three models, attempts have been made to construct and simulate the models within MATLAB\SIMULINK. Figure 6.2 displays the voltage conversion gain of the simulated models which reveals that the step-up conversion gain of the proposed topology is higher than those presented in [1] and [11] for duty ratios

greater than 0.5. As the gain of the topology presented in [11] is higher than the proposed topology for duty ratios less than 0.5, hence topology of [11] is not convenient for high voltage applications.

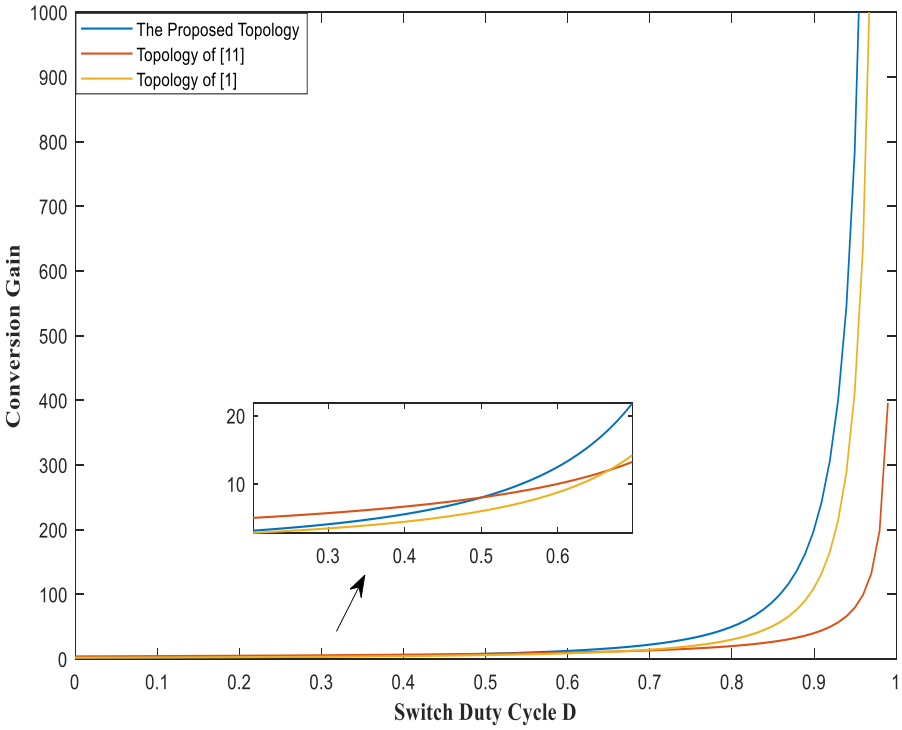


Figure 6.2 the step-up conversion gain of the proposed topology and those presented in [1] and [11] with the switches' duty cycle (ratio)

The comparative analysis of the pre-mentioned topologies based on the required devices and the DC analysis have been summarised in table 6.5.

Table 6.5 Comparison between the proposed topology and those presented in [1] and [11] for two input one output at these requirements: $V_o = 11\ kV, V_{i1} = V_{i2} = 330\ V\ and\ D_{i1} = D_{i2} = D_{i3} = D$ with 1 kHz switching frequency

	The proposed topology	**The topology presented in [1]**	**The topology presented in [11]**
Voltage gain ratio: V_o/V_i	$\frac{2}{(1-D)^2}$	$\frac{(2-D)}{(1-D)^2}$	$\frac{4}{(1-D)}$
Number of semiconductors	Diode: $(m+1)$ Switch: $(m+1)$	Diode: $(m+1)$ Switch: $(m+1)$	Diode: $(2m+1)$ Switch: (m)
Number of passive elements (m is the number of inputs)	Inductor:$(m+1)$ Capacitor:$(m+1)$	Inductor: $(m+1)$ Capacitor: $(m+1)$	Inductor: (m) Capacitor: $(2m+1)$
Extra components	(1) $Inductor$ (1) $Switch$	(1) $Inductor$ (1) $Switch$	(2) $Capacitors$ (2) $Diodes$
Output Diode voltage stress	(V_o)	$(V_o - V_{c2})$	$\frac{V_o}{2}$
Output current equation	$\frac{(V_{i1}+V_{i2})}{(1-D)^2 R_L}$	$\frac{V_o}{(1-D)R_L} + \frac{D(1-D)V_{i1}}{2Lf_s}$	$\frac{4*(V_{i1}+V_{i2})}{(1-D)R_L}$
Average current equation of Input Inductor	$\frac{(V_{i1}+V_{i2})}{(1-D)^4 R_L}$	$\frac{V_o}{(1-D)^2 R_L} + \frac{DV_{i1}}{2Lf_s}$	$\frac{4*(V_{i1}+V_{i2})}{(1-D)^2 R_L}$
Magnetic size (mH)	$L_{i1} = L_{i2} = 1.9$ $L_{o1} = 91$	$L_1 = L_2 = \cdots$ $L_3 = 27$	$L_1 = L_2 = 0.99$
Capacitance size (mF)	$C_{i1} = C_{i2} = 2.5$ $C_{o1} = 0.025$	$C_1 = 0.0105$ $C_2 = 0.005$ $C_o = 0.0318$	$C_1 = C_2 = C_3 = \cdots$ $C_4 = 10$ $C_o = 0.01$
The power switches' duty cycle D (%)	$D = 75$	$D = 81$	$D = 88$
The required switching signal for switching devices	Voltage controlled	Voltage controlled	Voltage controlled

It is noticeable that the topology presented in [11] requires two extra capacitors and two extra diodes compared with the proposed and reference [1] topologies. On the other hand, the number of the utilised inductors and switches in the topology presented in [11] are fewer. As the number of components will affect the size, weight and the cost of the design, thus,

the topology of [11] could be bulky and costly. However, the design of [11] requires a smaller number of inductors with much smaller size than those used in [1] and the proposed topology. In addition, the topology presented in [11] requires high switch's duty cycle i.e. $D = 0.88$ to meet the pre-determined requirements compared with the proposed topology. Thus, the latter is impractical as reported in [1].

In order to analyse the performance of the proposed and selected topologies, MATLAB\SIMULINK simulations have been performed. Here performance is related to the characteristics of the input current (I_1) and the output voltage (V_o). Figures 6.3 to 6.5 show the simulation results of the output voltage and the input current of the three models.

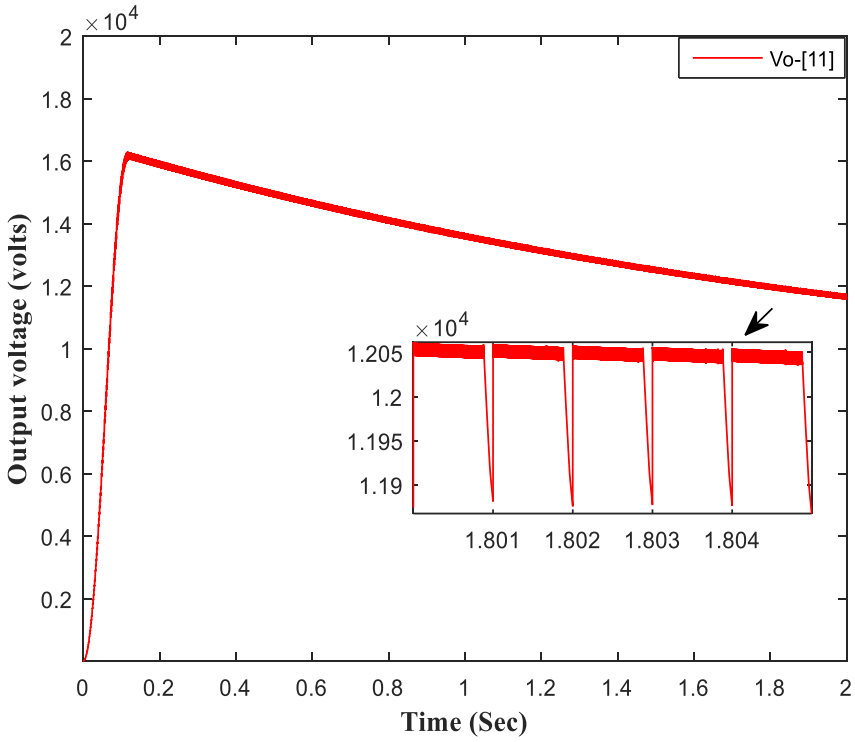


Figure 6.3.a. the output voltage response curve (V_o) of the topology presented in [11]

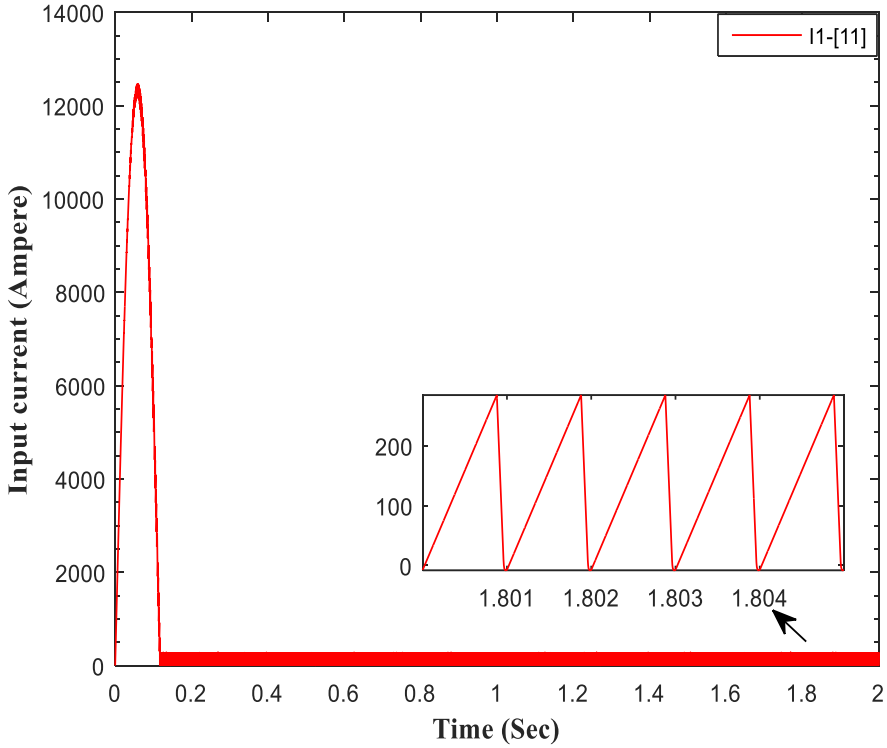


Figure 6.3.b. the input current response curve (I_1) of the topology presented in [11]

Figure 6.3 the output voltage and input current response curves of the topology presented in [11]

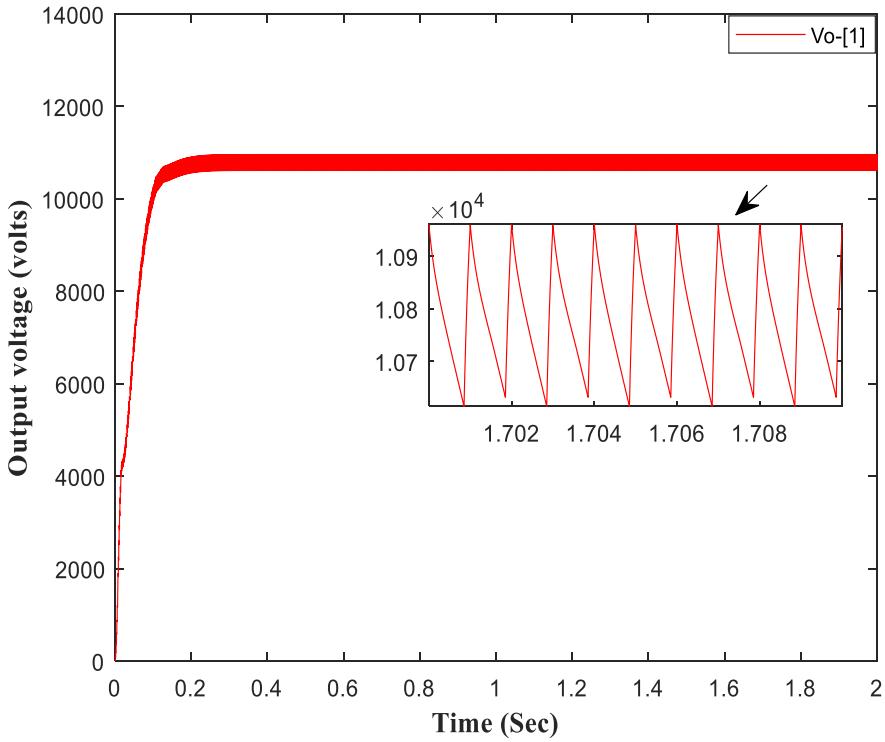


Figure 6.4.a. the output voltage response curve (V_o) of the topology presented in [1]

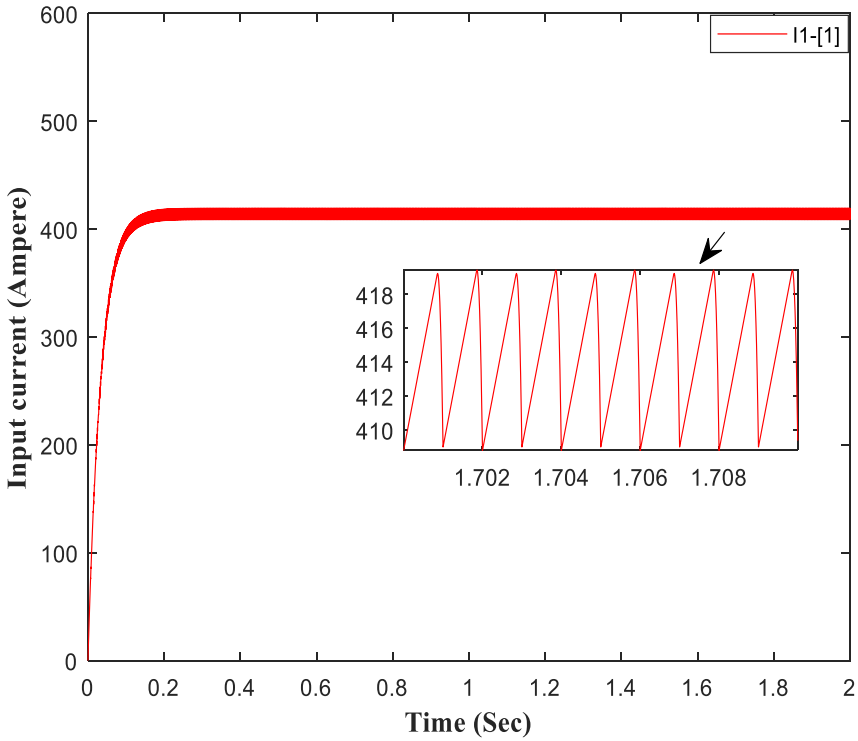


Figure 6.4.b. the input current response curve (I_1) of the topology presented in [1]

Figure 6.4 the output voltage and input current response curves of the topology presented in [1]

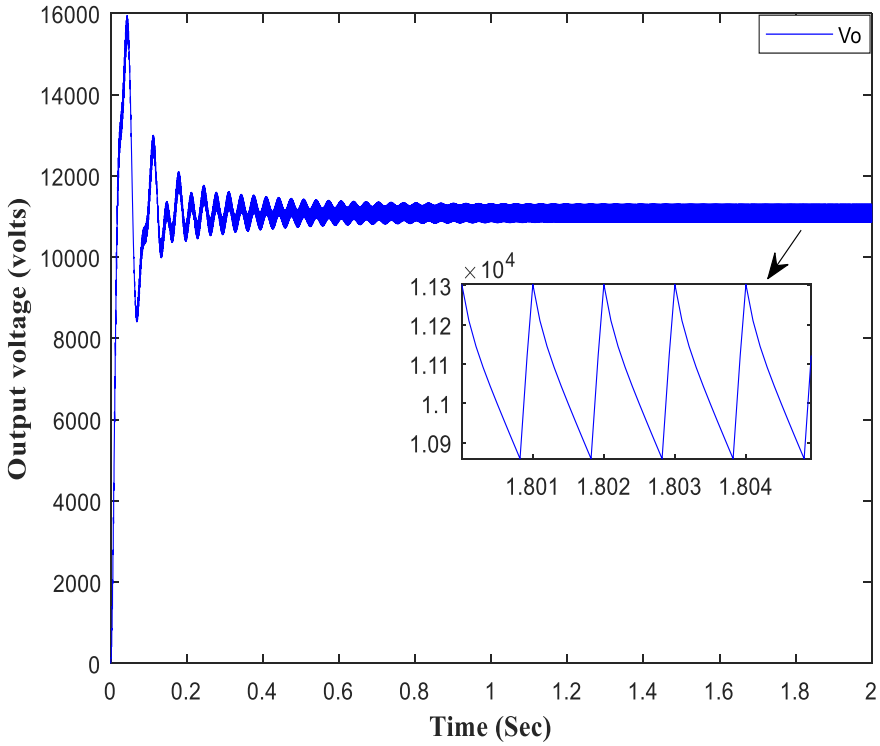


Figure 6.5.a. the output voltage response curve (V_o) of the proposed topology

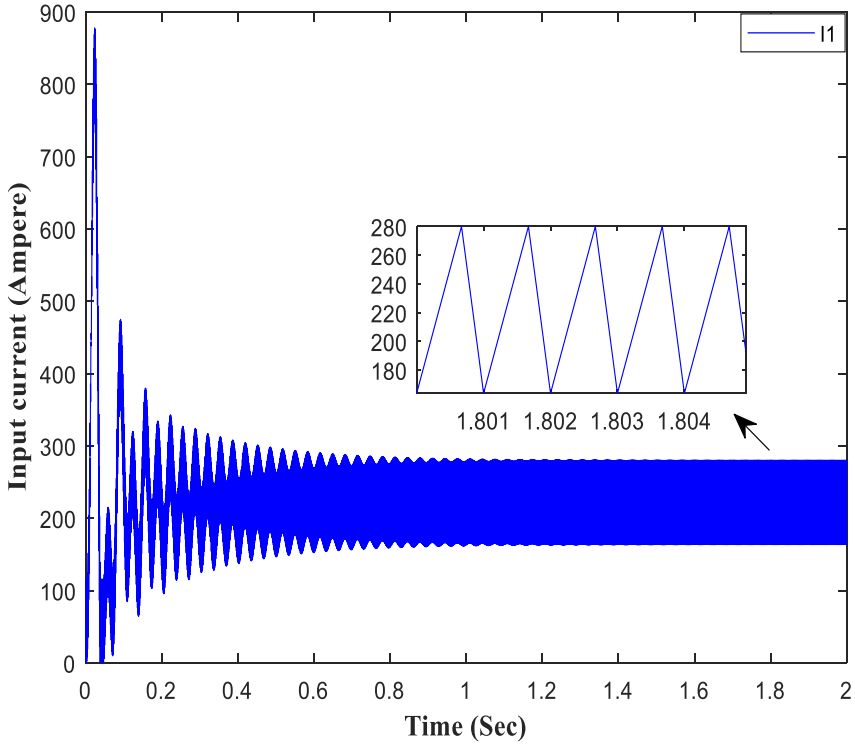


Figure 6.5.b. the input current response curve (I_1) of the proposed topology

Figure 6.5 the output voltage and input current response curves of the proposed topology

From the simulation results, it is found that the output voltage level of the topology presented in [11] does not correlate with the results obtained through theoretical analysis. However, a good agreement is observed between the simulation result of the output voltage of the

proposed topology and the theoretical output voltage level. Furthermore, the input inductor current ripple of the topology in [11] is higher than the other topologies. For example, in [11] is $150\ A$ and in the proposed design is $55\ A$, while in [1] is $6\ A$. However, the peak ripple output voltage of [11] is less than the others' designs by almost 50%. Table 6.6 summarises the simulation results of the three models for the purpose of comparison.

Table 6.6 Comparison between the proposed topology and those presented in [1] and [11] for two input one output at these requirements: $V_o = 11\ kV, V_{i1} = V_{i2} = 330\ V\ and\ D_{i1} = D_{i2} = D_{i3} = D$ with $1\ kHz$ switching frequency based on the MATLAB simulation results

	The proposed topology	**The topology presented in [1]**	**The topology presented in [11]**
Peak output voltage ripple (V)	(200)	(200)	(100)
Peak input inductor current ripple (A)	(55)	(6)	(150)
Response curve settling time (Sec)	0.4	0.2	4.3
Percentage of total power $loss^*$ (%)	15.1	39.4	30.3
Efficiency (%)	97.2	81.8	94.1
MATLAB solver time (Sec)	21.06	44.1	56.4

Tentative inspection of table 6.6 shows that the percentage loss of the topologies presented in [1] and [11] is high due to the switching loss, which depends on the switches' duty ratio value. In addition, the losses of the topology presented in [11] is higher because of the extra capacitors and diodes that used in the design.

In order to analyse the power capability of the evaluated models a comparison has been performed with respect to the switches' duty cycle value D as shown in figure 6.6.

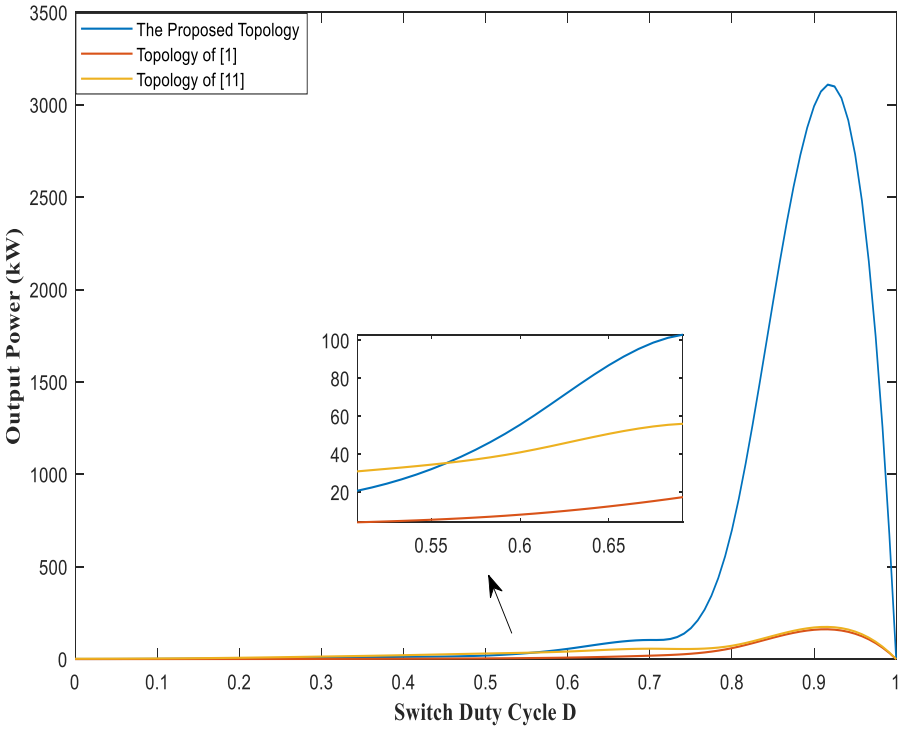


Figure 6.6 the output power of the proposed topology and those presented in [1] and [11] with the switches' duty cycle

It is clear, that the proposed design delivers higher power when the duty cycle "D" is greater than 0.55 compared with the other designs. While the topology of [11] deliver more power when $D < 0.55$ which suggests that the topology of [11] is more suitable for low power applications.

Efficiency is another essential characteristic in design of MIMO DC transformers. Efficiency is the ratio between the output power and the input power of the design. In the proposed and selected topologies, the total input power is expressed as:

$$P_{in_{Total}} = I_1 * V_{i1} + I_2 * V_{i2} \tag{6.15}$$

And the generic output power as:

$$P_o = \frac{{V_o}^2}{R_L} \tag{6.16}$$

For the proposed design

$$Po_{Proposed} = \frac{4{V_i}^2}{(1-D)^4 R_L} \tag{6.17}$$

And for the topology presented in [11] is:

$$Po_{[11]} = \frac{16{V_i}^2}{(1-D)^2 R_L} \tag{6.18}$$

While the output power of [1] expressed as:

$$Po_{[1]} = \frac{(D^2 - 4D + 4){V_i}^2}{(1-D)^4 R_L} \tag{6.19}$$

From these equations the efficiency could be found from the following relation:

$$\eta = \frac{P_o}{P_{in_{Total}}} * 100\% \tag{6.20}$$

Figure 6.7 shows the efficiency of each model vs. the switch duty cycle.

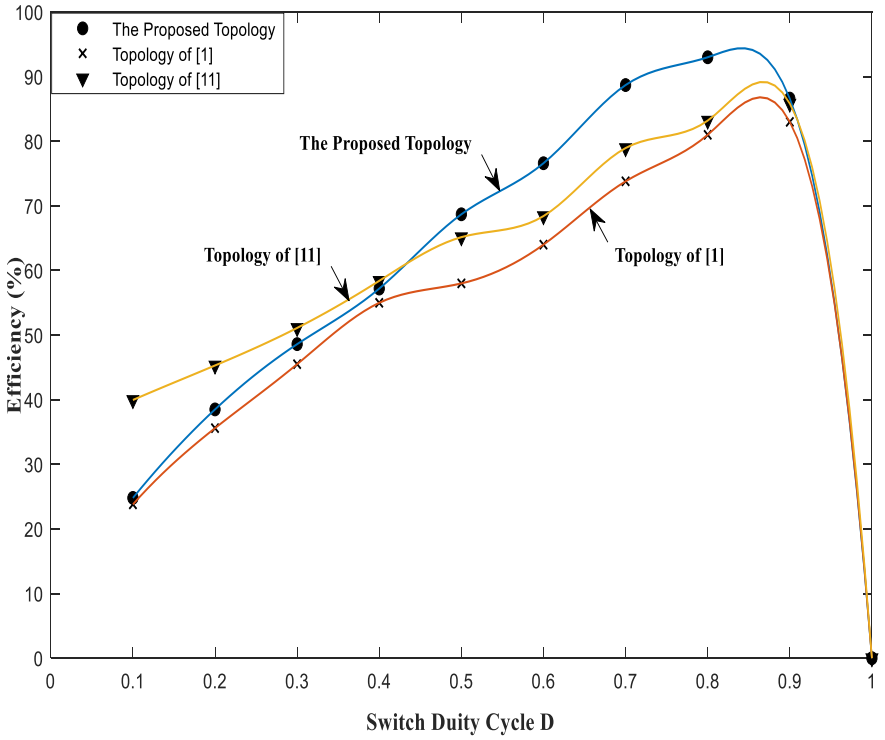


Figure 6.7 the simulated efficiency of the proposed topology and those presented in [1] and [11] with the switches' duty cycle

The other important parameters in design are the flexibility and reliability. Here the flexibility and reliability of the three models have been investigated under various scenarios. The scenarios are created by not making one of the input sources available to supply the load for an abnormal reason or due to occurrence of a fault. In each scenario, the transformer's controller must adjust to keep the output DC voltage level constant by increasing or decreasing the power switch's duty cycle. However, one must bear in mind that operation for duty cycles greater than 0.85 is almost impractical as reported in [1].

To have 11 kV at the output side, for each design the action of the controller in terms of the duty cycle value will be as follows:

For the proposed topology:

$$\begin{Bmatrix} V_{i1} = 0, & D_{NEW_{[proposed]}} = 0.83 \\ V_{i2} = 0, & D_{NEW_{[proposed]}} = 0.83 \end{Bmatrix}$$

The topology presented in [1]:

$$\begin{Bmatrix} V_{i1} = 0, & D_{NEW_{[1]}} = 0.97 \\ V_{i2} = 0, & D_{NEW_{[1]}} = 0.83 \end{Bmatrix}$$

The topology presented in [11]:

$$\begin{Bmatrix} V_{i1} = 0, & D_{NEW_{[11]}} = 0.94 \\ V_{i2} = 0, & D_{NEW_{[11]}} = 0.94 \end{Bmatrix}$$

Simulations have revealed that the power switch of the topology presented in [11] needs a high duty cycle value ($D_{NEW_{[11]}} = 0.94$), which is impractical in order to achieve the predefined requirements of the design. While in the topology presented in [1], the controller will be able to adjust ONLY if the first input source is always active to supply the load. However, the proposed topology is flexible and reliable in terms of the availability of the power sources with acceptable duty cycle value ($D_{NEW_{[proposed]}} = 0.83$).

In addition, increasing the duty cycle will increase the conduction and switching losses of the power switch. Thus, a higher duty cycle means more current conducts through the device if one considers $R_{CE_{ON}} = 0.01\ \Omega$ and $V_{CE_{ON}} = 3\ V$ for all the power switches. Also increases is the losses through the parasitic element that store and dissipate energy during each switching cycle.

6.2.2 Manufacturing cost of the proposed topology and the selected published topologies

The biggest challenges facing any design are the manufacturing cost, reliability and flexibility. In this section attempt is being made to estimate the manufacturing cost of ($330\ V/11\ kV$) DC transformers' components. As the prices tend to fluctuate, the quotation has been received from a number of companies with the following specifications and constraints as listed in table 6.7.

Table 6.7 the high voltage DC components' constraints of the proposed topology and those presented in [1] and [11] for pricing requirements

Capacitors		**Inductors**		**IGBTs power switch** $(\boldsymbol{f_s = 1\ kHz})$		**Diodes**	
Capacitance $(\boldsymbol{F})$	DC Voltage rating (kV)	Inductance (H)	DC Current rating (A)	Maximum operating voltage $V_{CE}\ (kV)$	Maximum operating power $(\ kW)$	Maximum forward voltage (kV)	Maximum forward current $(\ A)$
2.5 *m*	1.4	27 *m*	414	1	180	3.6	63
25 µ	11	995 µ	140	11	880	11	11
10.5 µ	3.6	2 *m*	180	3.6	1490	9	11
5 µ	2	91 *m*	80	2	1490	1	60
32 µ	11	-	-	2.75	385	2.75	17
10 *m*	2.75	-	-	-	-	5.5	11
10 µ	11	-	-	-	-	-	-

A company (High Voltage) from India on the 28th of April 2018 has forwarded the total price of the needed capacitors as shown below:

For the proposed topology

$$Total\ cost\ of\ C_{proposed} = £\ 1{,}302$$

And for the topology presented in [11]

$$Total\ cost\ of\ C_{[11]} = £\ 1{,}288$$

While the topology of [1]

$$Total\ cost\ of\ C_{[1]} = £\ 1{,}708$$

Also, a company in Jordan (Saluos for Supply) on 20/05/2018 has provided the following quotations for other components of the three models "two-input one-output DC transformer" topologies namely of reference [1], of reference [11] and the proposed design.

The power inductors:

For the proposed topology

$$Total\ cost\ of\ L_{proposed} = £\ 6{,}433$$

And for the topology presented in [11]

$$Total\ cost\ of\ L_{[11]} = £\ 4{,}575.2$$

While for the topology presented in [1]

$$Total\ cost\ of\ L_{[1]} = £\ 8{,}085$$

The power switches:

For the proposed topology

$$Total\ cost\ of\ Switches_{proposed} = £\ 67{,}795$$

And for the topology presented in [11]

$$Total\ cost\ of\ Switches_{[11]} = £\ 23{,}450$$

While for the topology presented in [1]

$$Total\ cost\ of\ Switches_{[1]} = £\ 86{,}275$$

The power Diodes:

For the proposed topology

$$Total\ cost\ of\ Diodes_{proposed} = £\ 4{,}022.2$$

And for the topology presented in [11]

$$Total\ cost\ of\ Diodes_{[11]} = £\ 2{,}587.2$$

While for the topology presented in [1]

$$Total\ cost\ of\ Diodes_{[1]} = £\ 7{,}591.5$$

Thus, the total cost of the DC transformer is:

For the proposed topology

$$Cost\ of\ DC\ Transformer_{proposed} = £\ 79{,}552.2$$

And for the topology presented in [1]

$$Cost\ of\ DC\ Transformer_{[1]} = £\ 103{,}659.5$$

While for the topology presented in [11]

$$Cost\ of\ DC\ Transformer_{[11]} = £\ 31{,}900.4$$

As shown in figure 6.8 the topology presented in [1] requires a high cost compared with the other topologies. While the cost of the topology presented in [11] is almost 50% less than the proposed topology due to the high cost of the $11\ kV$ power switches. Finally, it is worth noting that as the IGBTs rating voltage is almost $V_{CE} = 3.3\ kV$, therefore in practice a number IGBTs are connected in series to meet the predefined voltage level.

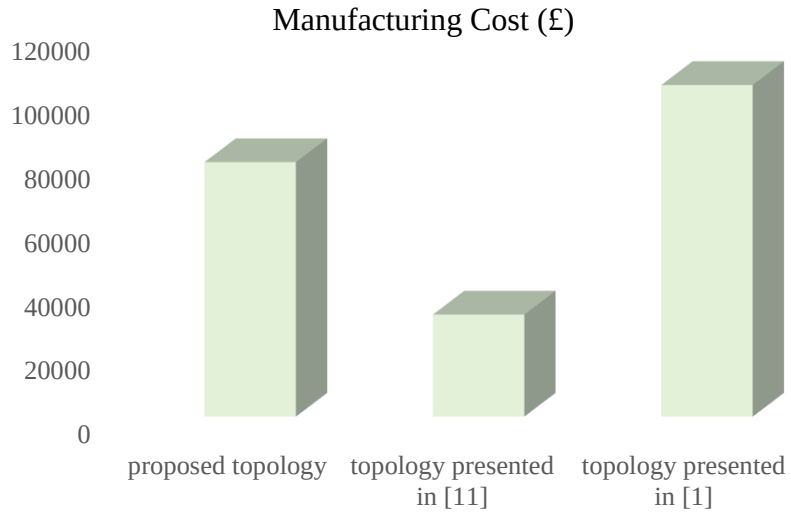


Figure 6.8 the manufacturing cost of the required passive components and semiconductors of the proposed and the selected topologies

6.3 Summary

It is hard to provide an efficient and financially viable design with a smaller size and weight. Thus, in designing DC transformers the trade-offs between the design key variables such as the switching frequency, performance, efficiency, weight and cost should be made. As the optimal selection of components, switching frequency and topology are dependent on operating specification such as voltage conversion gain, output voltage and output power [168].

In order to design a DC transformer for high voltage applications; higher conversion gain is needed. Hence topologies presented in [1] and [11] have been selected to compare their behaviour and characteristics with the proposed topology; as these topologies provide a high step-up conversion gain in comparison with the reviewed topologies. However, [1] and [11] possess different boosting techniques.

The performance characteristics of the proposed DC transformer and the selected topologies are analysed. The main parameters considered are, number of employed components, voltage conversion gain, duty cycle, output diode's voltage stress and the efficiency. The comparison has been summarised in table 6.5.

Inspection of table 6.5 suggests that the step-up conversion gain of the proposed topology is higher than the gain of the topology presented in [1] and also the gain of the topology presented in [11] is higher than the proposed topology for duty ratios less than 0.5 . The latter indicates that the topology of [11] is not convenient for high voltage applications.

Furthermore, in terms of the designs' size the topology presented in [11] requires two extra capacitors and two extra diodes compared with the topology in [1] and the proposed one. Also, the utilised capacitors in the topology presented in [11] with a large capacity leads to have a larger size and weight. As the number of components will affect the size, weight and the cost of the design, thus, the topology of [11] is expected to be bulky. In addition, the topology presented in [11] requires high switch's duty cycle to meet the predefined requirements compared with the proposed topology. For example, the topology of [11] requires a duty ratio of $D = 0.88$ that is impractical as reported in [1]. Also increasing the duty cycle as in [1] will increase the conduction and switching losses of the power switch. The losses acquired of the components in the topologies of [1] and [11] are high. This is mainly related to utilisation of a higher number of capacitors and diodes in [11] and passage of high current through the input cell in [1]. Thus, the proposed topology is more efficient compared with the selected topologies.

In addition, the proposed design delivers higher power when the duty cycle is greater than 0.55 ($D > 0.55$) compared with the other designs. While the topology of [11] deliver more power when $D < 0.55$ which again means that the topology of [11] is more convenient for low power applications.

On the other hand, the cost of the passive components and semiconductors that utilised in the proposed topology is high compared with the topology presented in [11]. Also, the cost of the topology presented in [11] is almost 50% less than the proposed topology due to the high cost of the $11\ kV$ power switches. While the topology presented in [1] requires a high cost compared with the proposed topology.

In conclusion, the designed DC transformer for high voltage applications has the advantages of simple configuration, fewer components, high conversion gain and high efficiency. In

addition, the manufacturing cost of the proposed design is less compared with the cost of the topology presented in [1]. While the cost of the topology presented in [11] is less than the cost of the proposed design however the topology of [11] is not practical for high voltage applications.

CHAPTER SEVEN

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The purpose of this research is achieved through development of an optimal Multi-Input Multi-Output (MIMO) step-up DC transformer for medium to high DC voltage applications particularly for high voltage renewable energy sources. The proposed design integrated several renewable energy sources to supply different locations with different voltage levels. MIMO DC transformers provide flexibility in terms of the choice and the availability of the power source, reduction in the number of power lines to transfer power to pre-specified locations as well as enhancement in system reliability. The proposed MIMO DC transformer has the advantages of simple configuration, fewer components, and high efficiency which reaches almost 98% in the case of ideal components. However, the efficiency of the proposed design depends on the number of inputs and outputs, therefore based on the pre-defined number of inputs, the number of outputs will be limited in order to have an efficient DC transformer. Also, the designed DC transformer has a significant advantage over the existing DC transformer designs where a high conversion gain is obtained without using an internal AC transformer. The general mathematical derivation which describes inputs with outputs in terms of the ideal and non-ideal design's components have been presented. The power losses of the designed DC transformer, considering the effect of the parasitic resistances of the components have been discussed in detail. Also considered is the effect of the resistance of the inductors on the DC transformer's performance. In this study with the view of the proposed DC transformer to be connected to high voltage renewable energy sources for which high efficiency and high conversion gain are needed, hence, $1\ kHz$ is chosen as the switching frequency. From the studies performed on the proposed DC transformer design, it is found that the proposed design components could become smaller in size by increasing the switching frequency. This is also true for the ripple current. But higher frequency means more losses, thus the efficiency of the designed DC transformer will be reduced. It is concluded from the simulation results for the considered example, the three-input two-output step-up DC transformer achieves the predetermined $8\ kV, 11\ kV$ (V_{o1}, V_{o2}) in steady state condition with peak-to-peak ripple voltage of $250\ V, 400\ V$ respectively. And with low ripple on the DC bus voltage V_o is acquired where the peak ripple voltage is $6\ V$ and the peak current is $10\ A$.

The modelling and control algorithm of the proposed MIMO step-up DC transformer have been carried out successfully. The Proportional Integral Derivative (PID) controllers have been designed and integrated to control and operate the proposed DC transformer in continuous conduction mode utilising the concept of closed loop voltage mode control. As the proposed MIMO DC transformer is a non-linear plant, hence Small Signal Modelling (SSM) and linearization of the plant is required to obtain a linear model for ease of analyse and to achieve a more stable and regulated output voltage. In order to obtain the SSM of the plant to be controlled, the mathematical modelling and the state space representation in a matrix form of the proposed DC transformer have been derived within the transformer's switching states. Also, the general mathematical representation of the proposed MIMO step-up DC transformer's state variables has been derived for m inputs and n outputs of the DC transformer. This yields to the transfer functions presentation of the designed transformer. The stability analysis of the proposed MIMO DC transformer is done through the transfer function approach using a Bode plot and pole-zero map for each input and output in order to guarantee the stability of the whole system. To maintain a balance between the stability and the transient behaviour a stable rule design for PID controllers tuning is proposed using the Routh-Hurwitz stability criterion. The effectiveness of this approach has been examined via simulations with different cases of disturbance.

The validity of the DC transformer's control performance is demonstrated through MATLAB-SIMULINK software simulation under different scenarios depending on the utilisation of the input sources. When one of the input sources is not available or when the demand changes in the system the controller automatically adapts and changes the duty ratio of the power switch in order to get the desired output voltage. The results verify the flexibility and robustness of the designed controller under demand and supply variations. It also proves the controllers' adaptive ability to adjust so as to ensure the system produces the desired output voltage level and to adjust when any changes are required by the system in order to have the desired output voltage level by controlling the ON and OFF time of the power switches. Furthermore, results prove the ability of the controller to keep the output voltages V_{o1}, V_{o2} fixed whatever the loads or the inputs changes with a good performance where 9.3% is the overshoot peak of V_{o1} and 7.2% for the second output V_{o2}. As well as there is a small peak-to-peak ripple voltage which is $40\ V$ for the two outputs.

In the case of the input sources availability, high voltage spikes have been detected via simulations when one of the input sources is no longer available in the system. Therefore, a first order low pass filter has been designed to provide an overvoltage protection for the

proposed DC transformer where the unwanted high voltage spikes have been reduced by almost 84%.

The performance of the proposed DC transformer under various fault conditions has been examined. The fault conditions are the short circuit of transistors and the open circuit of diodes. To verify the performance of the designed MIMO DC transformer faults are performed at different locations with different fault resistance values. With reference to table 5.13, it could be summarised that, the solid fault modes $1, 4$ and 5 can damage the proposed DC transformer, while this is not the case for the non-solid fault modes 1 and 2 if the fault resistance value $R_F > 7\ \Omega$. Furthermore, for non-solid fault modes 4 and 5 the proposed DC transformer will be damaged if $R_F < 30\ \Omega$. The open circuit fault modes $6, 7, 8, 9$ and 10 do not damage the proposed DC transformer.

Finally, the proposed MIMO step-up DC transformer is designed for medium to high voltage applications; then a higher conversion gain is needed. Hence topologies presented in [1] and [11] have been selected to compare their behaviour and characteristics with the proposed topology. However, [1] and [11] possess different boosting techniques. The performance characteristics of the proposed DC transformer and the selected topologies are analysed. The main parameters considered are, number of employed components, voltage conversion gain, duty cycle, efficiency and the utilised semiconductors and passive components cost. The MATLAB-SIMULINK simulations have been performed and the results have been presented. From the simulation results, it is found that the output voltage level of the topology presented in [11] does not correlate with the results obtained through theoretical analysis. However, a good agreement is observed between the simulation result of the output voltage of the proposed topology and the theoretical output voltage level. Furthermore, the input inductor current ripple of the topology in [11] is higher than the other topologies. For example, in [11] is $150\ A$ and in the proposed design is $55\ A$, while in [1] is $6\ A$. However, the peak ripple output voltage of [11] is less than the others' designs by almost 50%.

Furthermore, the settling time of the output voltage response curve of the topology presented in [11] is much higher than the other topologies which equals to $4.3\ Sec$ while in the proposed topology it is $0.4\ Sec$ thus the response of the proposed topology is faster than the topology of [11].

From the comparative analysis one could be concluded that, that the step-up conversion gain of the proposed topology is higher than the gain of the topology presented in [1] and also the gain of the topology presented in [11] is higher than the proposed topology for duty ratios less than 0.5. The latter indicates that the topology of [11] is not convenient for high voltage

applications. In addition, the proposed design delivers higher power when the duty cycle is more than 55% compared with the topologies described in [1] and [11]. As the topology of [11] delivers more power for duty cycles less than 55%, this suggests its suitability for low power applications. In addition, the topology presented in [11] requires high switch's duty cycle to meet the predefined requirements compared with the proposed topology. Also increasing the duty cycle as in [1] will increase the conduction and switching losses of the power switch. The losses acquired of the components in the topologies of [1] and [11] are high. This is mainly related to utilisation of a higher number of capacitors and diodes in [11] and passage of high current through the input cell in [1]. Thus, the proposed topology is more efficient compared with the selected topologies.

Furthermore, in terms of size, the topology presented in [11] requires two extra capacitors and two extra diodes compared with the topology in [1] and the proposed one. Also, the utilised capacitors in the topology presented in [11] have a larger capacity, and hence, larger size and subsequently weight. In addition, the topology of [11] requires high duty cycle $D = 88\%$ for switching to meet the predefined requirements compared with the proposed topology ($D = 75\%$). The former is reported to be impractical by [1].

The manufacturing cost estimation of ($330\ V/11\ kV$) DC transformers' equipment received from two companies: (High Voltage) from India on the 28th of April 2018 and also, a company in Jordan (Saluos for Supply) on 20/05/2018 for the components' specifications and constraints. It is found that the cost of the passive components and semiconductors utilised in the proposed topology is higher by about 50% compared with the topology presented in [11]. This might be due to the cost of IGBTs ($V_{CE} = 3.3\ kV$) which in practice for $11\ kV$ utilisation almost a number of series connected IGBTs are needed to meet the predefined voltage level. In contrast, the cost topology presented in [1] is higher in comparison to the proposed topology, i.e. almost £$103{,}659.5$ (the total cost of the passive components and semiconductors) and £$79{,}552.2$ respectively.

7.2 Recommendations and Further work

This research work has provided a new MIMO step-up DC transformer design for medium to high voltage applications. Future research directions will focus on improving the proposed design by studying the following points:

1. Prototype construction of the proposed MIMO step-up DC transformer for validation of the proposed model simulated in MATLAB-SIMULINK software.

2. Further elaboration of fault modes in terms of non-linear arc resistance and the effect of the AC fault on the DC side operation or vice versa. Also, classification of faults types within the proposed DC transformer. In this work only two types of faults namely line to ground (short circuit across the switches) and (open circuit across the diodes) have been investigated.

3. Integration of the DC circuit breakers; where the circuit breakers will be positioned on DC grids and act when a fault occurs in the system. There are two types of HVDC circuit breakers: electromechanical and solid-state. Each type has a specific typical voltage and current ratings also its required time for clearing the fault.

4. Implementation of DC protection scheme. Possibly by using some of the existing AC protection schemes where a reviewing and development of both AC and DC protection devices such as measurement devices, relay, communication protocol and circuit breakers.

5. Improving the utilised controller performance in deferent cases (e.g. reducing the overshoot of the response curve when one of the utilised sources is no longer available in the system) possibly by combining two different control techniques, for example PID controller in conjunction with fuzzy logic control, artificial neural network, particle swarm or H2∞ control concept.

6. Ziegler-Nichols tuning (trial and error) approach has been used to design PID controller for MIMO systems. Thus, proposing a new tuning approach which is easy and not time consuming for MIMO systems in order to generalise the MIMO PID design.

REFERENCES

[1] K. Varesi, A. Ghandomi, and S. Hosseini, (2017). *An improved structure for Multi- Input high step-up DC-DC converters.* Mashhad: 8th Power Electronics, Drive Systems & Technologies Conference (PEDSTC), pp. 241–246.

[2] National Grid Electricity Transmission plc. (2018). *Offshore Development Information Statement: Future Scenarios Consultation*. [Online]. Available at: http://www.nationalgrid.com. [Accessed 08 November 2018].

[3] Bresesti, P. Kling, W. L. Hendriks, R. L and Vailati, R. (2007). *HVDC connection of offshore wind farms to the trans-mission system*. IEEE Trans. Energy Conv., vol. 22, no. 1, pp. 37-43.

[4] Macken, K.J.P. Driesen, J.L.J. Belmans, R.J.M. (2001). *A DC Bus System for connecting offshore wind turbines with utility system.* Denmark: European Wind Energy Conference 2001, Copenhagen, pp. 1030-1035, 2-6.

[5] Renewable energy magazine. (2015). *Siemens wins major order to connect British and Belgian national grids*. [Online]. Available at: http://www.renewableenergymagazine.com/article/siemens-wins-major-order-to-connect-british-20150608. [Accessed 08 June 2015]

[6] ABB Power System. (2018). *HVDC systems, Economic-and-environmental-advantages*. [Online]. Available at: http://new.abb.com/systems/hvdc/why-hvdc/economic-and-environmental-advantages. [Accessed 10 July 2018].

[7] Rudervall, R. Charpentier, J. and Sharma, R. (2000). *High voltage direct current transmission systems technology*. Sweden: ABB Power Syst. Review Paper.

[8] Slide share. (2010). *A Concise Introduction to Qualitative Research Methods in Information Sciences*. [Online]. Available at: https://www.slideshare.net/adfigueiredo/qualitative-research-methods. [Accessed 12 December 2017].

[9] European Wind Energy Association (EWEA). (2009). *Oceans of Opportunity: Harnessing Europe's largest domestic energy resource.* [Online]. Available at: http://www.ewea.org. [Accessed 08 November 2015].

[10] National Renewable Energy Laboratory (NREL). (2010). *Large-scale offshore wind power in the United States*. [Online]. Available at: http://www.osti.gov/bridge. [Accessed 8 November 2015].

[11] Hou, S. Chen, J. Sun, T. and Bi, X. (2016). *Multi-input step-up converters based on the switched-diode-capacitor voltage accumulator*. IEEE Trans. Power Electron, vol. 31, no. 1, pp. 381–393.

[12] Eriksson, E. Halvarsson, P. Wensky, D. and Hausler, M. (2003). *System Approach on Designing an Offshore Wind power Grid Connection*. Sweden: Proc. of the 4th International Workshop on Large-Scale Integration of Wind Power and Transmission networks for Offshore Wind Farms.

[13] Bolik, S. M. (2003). *Grid Requirements Challenges for Wind Turbines*. Sweden: Proc. of the 4th International Workshop on Large-Scale Integration of wind power and Transmission networks for Offshore Wind Farms.

[14] Giddani, O. A. Adam, G. P. Anaya-Lara, O. Burt, G. and Lo, K. L. (2010). *Potential benefits of decoupling the Scotland-England network using VSC-HVDC in AC and DC Power Transmission. ACDC*. 9th IET International Conference, pp. 1-5.

[15] Adamowitsch, G. W. (2008). *Connection to offshore wind power in Northern Europe*. Brussels: EU Coordinator's Rep.

[16] Heinemann, L. (2002). *Analysis and design of a modular, high power converter with high efficiency for electrical power distribution systems*. Proc. IEEE Power Eng. Soc. Conf., vol. 2, pp. 713–718.

[17] Bahram, M. Baker, M. Bowles, J. Bunch, R. LeMay, J. Long, W. McConnach, J. Menzies, R. Reeve, J. and Szechtman, M. (1995). *Integration of small taps into (existing) HVDC links*. IEEE Trans. Power Del., vol. 10, no. 3, pp. 1699–1706.

[18] Nanou, S. I. Papathanassiou, S. A. and Papadopoulos, M. P. (2014). *HV transmission technologies for the interconnection of Aegean Sea islands and offshore wind farms*. Athens: Med Power, pp. 1-6. doi: 10.1049/cp.2014.1674.

[19] Stamatiou, G. Srivastava, K. Reza, M. and Zanchetta, P. (2011). *Economics of DC wind collection grid as affected by cost of key components*. Sweden: world renewable energy congress.

[20] Mohan, N. Undeland, T. and Robbins, W. P. (1995). *Power Electronics Converters, Applications and Design*. Chapter one. New York: Wiley.

[21] Zhao, Q. and Lee, F. C. (2003). *High efficiency, high step up DC-DC converters*. IEEE Trans. Power Electron, vol. 18, no. 1, pp. 65–73.

[22] Hirachi, K. et al. (2002). *Circuit configuration of bi-directional DC/DC converter specific for small scale load levelling system*. Proc. Inst. Elect. Eng. Power Conversion Conf., pp. 603–609.

[23] Max, L. and Thiringer, T. (2007). *Control method and snubber selection for a 5 MW wind turbine single active bridge DC/DC converter*. Proc. Eur. Conf. Power Electronics and Applications, pp. 1–10.

[24] Jovcic, D. (2010). *Developing DC Transmission Networks Using DC Transformers*. IEEE transaction on power delivery, Vol. 25, no. 4, pp 2535-2543.

[25] Su, G. J. Peng, F. Z. and Adams, D. J. (2002). *Experimental Evaluation of a Soft-Switching DC-DC Converter for Fuel Cell Applications*. PET'02, pp. 39-44.

[26] Matsuo, H. Wenzhong Lin, Kurokawa, F. Shigemizu, T. and Watanabe, N. (2004). *Characteristics of the Multiple-Input DC-DC Converter*. IEEE Transactions on Industrial Electronics, Vol. 51, pp. 625-63 1.

[27] Dobbs, B. G. and Chapman, P. L. (2003). *A Multiple-Input DC-DC Converter Topology*. IEEE Power Electronics Letters, Vol. 1, pp. 6-9.

[28] Matsuo, H. Kobayashi, K. Sekine, Y. Asano, M. and Wenzhong, L. (1998). *Novel Solar Cell Power Supply System using the Multiple-Input DC-DC Converter*. IEEE INTELEC, pp. 797-802.

[29] Caricchi, F. et al. (1993). *Testing of a New DC/DC Converter Topology for Integrated Wind-Photovoltaic Generating Systems*. Brighton: 5th European Conference on Power Electronics and Applications, U.K.

[30] Solero, L. et al. (1996). *Performance of a 10 kW Power Electronic Interface for Combined Wind/PV Isolated Generating Systems*. Baveno: 27th Annual IEEE Power Electronics Specialists Conference, (PESC), Italy.

[31] Di Napoli, A. et al. (2002). *Multiple Input DC-DC Power Converter for Fuel-Cell Powered Hybrid Vehicles*. Cairns: 33rd Annual Power Electronics Specialists Conference, (PESC), Australia.

[32] Solero, L. et al. (2005). *Design of Multiple-Input Power Converter for Hybrid Vehicles*. IEEE Transactions on Power Electronics 20(5), pp 1007 – 1016.

[33] Liu D. and Li, H. (2005). *A Novel Multiple-Input ZVS Bidirectional DC-DC Converter*. Raleigh: 31st Annual Conference of IEEE Industrial Electronics Society, USA.

[34] Marchesoni, M. and Vacca, C. (2007). *New DC–DC Converter for Energy Storage System Interfacing in Fuel Cell Hybrid Electric Vehicles*. IEEE Transactions on Power Electronics 22(1), pp 301 – 308.

[35] Choung, S. H. and Kwasinski, A. (2008). *Multiple-Input DC-DC Converter Topologies Comparison.* Orlando: 34th Annual Conference of IEEE Industrial Electronics, (IECON), USA.

[36] Khaligh, A. Cao, J. and Lee, Y.J. (2009). *A Multiple-Input DC–DC Converter Topology*. IEEE Transactions on Power Electronics, 24(3), pp 862 – 868.

[37] Kwasinski, A. (2009). *Identification of Feasible Topologies for Multiple-Input DC–DC Converters*. IEEE Transactions on Power Electronics 24(3), pp 856 – 861.

[38] Song, J. and Kwasinski, A. (2009). *Analysis of the Effects of Duty Cycle Constraints in Multiple-Input Converters for Photovoltaic Applications*. Incheon: 31st International Telecommunications Energy Conference, (INTELEC), South Korea.

[39] Qian, Z. Abdel-Rahman, O. and Batarseh, I. (2010). *An Integrated Four-Port DC/DC Converter for Renewable Energy Applications*. IEEE Transactions on Power Electronics 25(7), pp 1877 – 1887.

[40] Jovcic, D. and Ooi, B. T. (2011). *Tapping on HVDC lines using DC Transformers*. Electric Power Systems Research 81(2), pp 561–569.

[41] Preti, T. et al. (2014). *Design High Gain DC-DC Boost Converter with Coupling Inductor and Simulation in PSIM*. International Journal of Research in Engineering and Technology, Volume: 03 Issue: 04, pp 156-163.

[42] Nithya, K. and Ramasamy, M. (2014). *Modeling of Multi-Input DC-DC Converter for Renewable Energy Sources*. International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, Special Issue 1, pp 970-975.

[43] Dusmez, S. and Li, X. (2016). *A New Multi input Three Level DC-DC Converter*. IEEE Transactions on Power Electronics, Vol. 31, no.2.

[44] Lopezo, O. Teodorescu, R. Doval-Gandoy, J. (2006). *Multilevel transformer-less topologies for single-phase grid-connected converters*. Proc. IEEE IECON'06, pp. 5191–5196.

[45] Carrasco, J.M. Franquelo, L.G. Bialasiewice, J.T. et al. (2006). *Power-electronic systems for the grid integration of renewable energy sources: a survey*. IEEE Trans. Ind. Electron., 53, (4), pp. 1002–1016.

[46] Myrzik, J. and Calais, M. (2003). *String and module integrated inverters for single-phase grid connected photovoltaic systems – a review*. Proc. IEEE Bologna Power Tech Conf., vol. 2, p. 8.

[47] Nouri, T. Hosseini, S. H. Babaei, E. and Ebrahimi, J. (2015). *Interleaved high step-up DC-DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell*. Power Electronics, lET, vol. 8, pp. 175-189.

[48] Wu, G. Ruan, X. and Ye, Z. (2015). *Nonisolated High Step-Up DC-DC Converters Adopting Switched-Capacitor Cell*. IEEE Transactions on Industrial Electronics, vol. 62, pp. 383-393.

[49] Zhou, W. Zhu, B. X. and Luo, Q. M. (2012). *High step-up converter with capacity of multiple input.* Power Electronics, I ET, vol. 5, pp. 524-531.

[50] Prudente, M. Pfitscher, L. L. Emmendoerfer, G. Romaneli, E. F. and Gules, R. (2008). *Voltage multiplier cells applied to non-isolated dc-dc converters*. IEEE Trans. Power Electron, vol. 23, no. 2, pp. 871–887.

[51] Prudente, M. Pfitscher, L. L. and Gules, R. (2005). *A boost converter with voltage multiplier cells*. Proc. IEEE Power Electron. Spec. Conf., pp. 2716–2721.

[52] Fardoun, A. A. and Ismail, E. H. (2010). *Ultra step-up DC-DC converter with reduced switch stress*. IEEE Trans. Ind. Appl., vol. 46, no. 5, pp. 2025–2034.

[53] Tyagi, P. Kotak, V.C. and Singh, V.P. (2014). *Design high gain DC-DC boost converter with coupling inductor*.

[54] Al-Saffar, M. and Ismail, E. (2014). *A high voltage ratio and low stress DC/DC converter with reduced input current ripple for fuel cell source*.

[55] Ajjami, W. Ardi, H. and Farakhor, A. (2012). *High voltage gain interleaved DC boost converter application for photovoltaic generation system*.

[56] Tang, Yu. Fu, D. and Zhiweixu, T. (2014). *Hybrid switched inductor converters for high step-up conversion*.

[57] Ajami, A. Ardi, H. and Farakhor, A. (2015). *A novel high step-up DC/DC converter based on integration coupled inductors and switched-capacitors techniques for renewable energy applications*.

[58] Jia Su, J. Peng, F. and Adams, D. (2002). *Experimental evaluation of soft- switching DC/DC converter for fuel cell vehicle applications*.

[59] Shiau, J. and Cheng, C. (2009). *Design of a non-inverting synchronous Buck-Boost DC/DC power convert with moderate power level*.

[60] Chiu, H.J. Huang, H. Lin, L.W. and Tseng, M. (2005). *A multiple -input DC/DC converter for renewable energy system*.

[61] © [2016] IEEE. Reprinted, with permission, from [Alzgool, M. Alzghoul, G. Nouri, H. and Toomer, C., *A Novel Multi-Inputs-Single-Output DC Transformer Topology*, Coimbra: 51st International Power Engineering Conference, ISEC Portugal, September/ 2016].

[62] Nami, A. Zare, F. Ghosh, A. and Blaabjerg, F. (2010). *Multi- output DC/DC converters based on diode- clamped converters configuration: topology and control strategy*.

[63] Nahavandi, A. Tarafdar, M. Sharifian, M. and Danyali, S. (2014). *A Non-isolated multi-input multi-output DC/DC boost converter for electric vehicle applications*.

[64] Boora, A. Zare, F. and Ghosh, A. (2010). *Multi-output buck-boost converter with enhanced dynamic response to load and input voltage changes*.

[65] Solero, L. Lidozzi, A. and Pomilio, J. (2005). *Design of multiple- input power converter for hybrid vehicles*.

[66] Matsuo, H. Shigemizu, T. Kurokawa, F. and Watanabe, N. (1993). *Characteristics of the multiple- input DC/DC converter*.

[67] Patra, P. Patra, A. and Misra, N. (2011). *A single-inductor multiple output switcher with simultaneous buck, boost and inverted output*.

[68] Boora, A. Zare, F. and Ledwich, G. (2008). *A new DC/DC converter with multi output topology and control strategies*.

[69] Zeng, J. Qiao, W. Luo, L. and Jiao, Y. (2014). *An isolated multiport dc-dc converter for simultaneous power management of multiple different renewable energy sources*. IEEE J. Emerg. Sel. Topics Power Electron, vol. 2, no. 1, pp. 70–78.

[70] Wu, H. Xu, P. Hu, H. Zhou, Z. and Xing, Y. (2014). *Multiport converters based on integration of full-bridge and bidirectional dc-dc topologies for renewable generation systems*. IEEE Trans. Ind. Electron., vol. 61, no. 2, pp. 856– 869.

[71] Lam, J. and Jain, P. (2014). *A novel electrolytic capacitor-less multi-input dc/dc converter with soft-switching capability for hybrid renewable energy system*. Proc. 16th Eur. Conf. Power Electron. Appl., pp. 1–10

[72] Zhang, Y. and Xu, D. (2007). *Design and implementation of an accurately regulated multiple output ZVS dc-dc converter*. IEEE Trans. Power Electron, vol. 22, no. 5, pp. 1731–1742.

[73] Kwasinski, A. (2009). *Identification of feasible topologies for multiple-input dc-dc converters*. IEEE Trans. Power Electron., vol. 24, no. 3, pp. 856– 861.

[74] Wai, R.J. and Jheng, K.H. (2013). *High-efficiency single-input multiple-output dc-dc converter*. IEEE Trans. Power Electron. vol. 28, no. 2, pp. 886–898.

[75] Ahsanuzzaman, S. Blackman, J. McRae, T. and Prodic, A. (2013). *A low-volume power management module for portable applications based on a multi output switched-capacitor circuit*. Proc. IEEE 28th Anu. Appl. Power Electron. Conf. Expo., pp. 1473–1479.

[76] Wai, R.J. and Liaw, J.-J. (2015). *High-efficiency isolated single-input multiple output bidirectional converter*. IEEE Trans. Power Electron. vol. 30, no. 9, pp. 4914–4930.

[77] Benavides, N. and Chapman, P. (2005). *Power budgeting of a multiple-input buck-boost converter*. IEEE Trans. Power Electron, vol. 20, no. 6, pp. 1303–1309.

[78] Tao, H. Kotsopoulos, A. Duarte, J. and Hendrix, M. (2006). *Family of multiport bidirectional dc-dc converters*. Proc. IEE, vol. 153, no. 3, pp. 451–458.

[79] Zhao, C. Round, S. and Kolar, J. (2008). *An isolated three-port bidirectional dc-dc converter with decoupled power flow management.* IEEE Trans. Power Electron, vol. 23, no. 5, pp. 2443–2453.

[80] Su, G.-J. and Tang, L. (2008). *A multiphase, modular, bidirectional, triple voltage dc-dc converter for hybrid and fuel cell vehicle power systems*. IEEE Trans. Power Electron, vol. 23, no. 6, pp. 3035–3046.

[81] Wu, H. Sun, K. Ding, S. and Xing, Y. (2013). *Topology derivation of non-isolated three-port dc-dc converters from DIC and DOC*. IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3297–3307.

[82] Behjati, H. and Davoudi, A. (2013). *A multiple-input multiple-output dc-dc converter*. IEEE Trans. Ind. Appl., vol. 49, no. 3, pp. 1464–1479.

[83] Behjati, H. and Davoudi, A. (2013). *Power budgeting between diversified energy sources and loads using a multiple-input multiple-output dc-dc converter*. IEEE Trans. Ind. Appl., vol. 49, no. 6, pp. 2761–2772.

[84] Behjati, H. and Davoudi, A. (2013). *Single-stage multi-port dc-dc converter topology*. IET Power Electron, vol. 6, pp. 392–403.

[85] Keyhani, H. and Toliyat, H. (2013). *A zvs single-inductor multi-input multioutput dc-dc converter with the step up/down capability*. Proc. IEEE Energy Convers, pp. 5546–5552.

[86] Danyali, S. Hosseini, S. and Gharehpetian, G. (2014). *New extendable single stage multi-input dc-dc/ac boost converter*. IEEE Trans. Power Electron, vol. 29, no. 2, pp. 775–788.

[87] Zeng, J. Qiao, W. and Qu, L. (2014). *An isolated multiport bidirectional dc-dc converter for PV-battery-dc microgrid applications*. Proc. IEEE Energy Convers, pp. 4978–4984.

[88] Hawke, J. Krishnamoorthy, H. and Enjeti, P. (2014). *A multiport power sharing converter topology for renewable-to-grid interface*. Proc. IEEE Energy Convers, pp. 4992–4999, Congr. Expo.

[89] Filsoof, K. Peter, and Lehn, W. (2016). *A Bidirectional Multiple-Input Multiple-Output Modular Multilevel DC–DC Converter and its Control Design*. IEEE Trans. Power Electron, vol. 31, no. 4.

[90] Nahavandi, A. Tarafdar Hagh, M. Bagher Bannae Sharifian, M. and Danyali, S. (2015). *A Nonisolated Multiinput Multioutput DC–DC Boost Converter for Electric Vehicle Applications*. IEEE Trans. Power Electron, vol. 30, no. 4.

[91] Michon, M. Duarte, J. L. Hendrix, M. A. and Simes, M. G. (2004). *A three port bidirectional converter for hybrid fuel cell systems*. Aachen: Proc. 35th Annu. IEEE Power Electron. Spec. Conf., Germany, pp.4736– 4741.

[92] Tao, H. Kotsopoulos, A. Duarte, J. L. and Hendrix, M.A. (2008). *Transformer coupled multiport ZVS bidirectional DC–DC converter with wide input range*. IEEE Trans. Power Electron. vol. 23, no. 2, pp. 771–781.

[93] Ji, C. Smith, K. M. Smedley, K. M. and King, K. (2001). *Cross regulation in flyback converters: analytic model and solution.* IEEE Trans. Power Electron. vol. 16, no. 2, pp. 231-239.

[94] Chung, H. S. Hui, S. Y. R. and Wang, W. (1999). *A zero-current-switching PWM flyback converter with a simple auxiliary switch*. IEEE Trans. Power Electron, vol. 14, no. 2, pp. 329-342.

[95] Hang, L. Li, B. Liu, S. Gu, Y. Yao, W. and Lu, Z. (2011). *Asymmetrical secondary structure of LLC series resonant DC/DC converter for multi-output applications*. IET Power Electron. vol. 4, no. 9, pp. 993-1001.

[96] Kim, H. Jung, J. Baek, J. and Kim, H. (2013). *Analysis and Design of a Multi output Converter Using Asymmetrical PWM Half-Bridge Flyback Converter Employing a Parallel – Series Transformer*. IEEE Trans. Ind. Electron., pp. 3115-3125.

[97] Tao, H. Kotsopoulos, A. Duarte, J. Hendrix, M. (2006). *Family of multiport bidirectional DC–DC converters*. IEE Proc. Electron. Power Appl., 153, (3), pp. 451–458.

[98] Zhang, Z. Thomsen, O. Andersen, M. Nielsen, H. (2012). *Dual-input isolated full-bridge boost dc–dc converter based on the distributed transformers*. IET Power Electronics, 5, (7), pp. 1074–1083.

[99] Babaei, E. and Abbasi, O. (2015). *Structure for multi-input multi-output dc–dc boost converter*. IET Power Electronics, ISSN 1755-4535.

[100] Khosrogo, S. et al. (2016). *Multi-input DC/DC converters in connection with distributed generation units-A review*. Renewable and Sustainable Energy Reviews 66: 360-379.

[101] Yang, L. Liang, T. and Chen, J. (2009). *Transformerless DC-DC converters with high step-up voltage gain*. IEEE Trans. Ind. Electron, vol. 56, no. 8, pp. 3144–3152.

[102] Nejabatkhah, F. Danyali, S. Hosseini, S. H. Sabahi, M. and Mozaffari Niapour, S. A. (2012). *Modeling and control of a new three-input DC–DC Boost converter for hybrid PV/FC/battery power system*. IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2309–2325.

[103] Boora, A. A. Nami, A. Zare, F. Ghosh, A. and Blaabjerg, F. (2010). *Voltage sharing converter to supply single-phase asymmetrical four-level diodeclamped inverter with high power factor load*. IEEE Trans. Power Electron, vol. 25, no. 10, pp. 2507–2521.

[104] Behjati, H. and Davoudi, A. (2012). *A MIMO topology with series outputs: An interface between diversified energy sources and diode-clamped multilevel inverter*. Proc. Appl. Power Electron. Conf. Expo.

[105] Behjati, H. and Davoudi, A. (2011). *A multi-port DC–DC converter with independent outputs for vehicular applications*. Proc. Vehicle Power Propulsion Conf.

[106] Jafari, M. Hunter, G. and Zhu, J. (2012). *A new topology of multi-input multi-output buck-boost DC-DC converter for microgrid applications*. Kota Kinabalu: Proc. Power and Energy (PECon), Malaysia, pp. 286–291.

[107] Verma, S. Singh, S.K. and Rao, A.G. (2013). *Overview of control techniques for DC-DC converters*. Research journal of engineering sciences, Vol. 2(8), 18-21.

[108] Lorentz, V. (2008). *Bidirectional DC Voltage Conversion for Low Power Applications*. Erlangen-Nuremberg: the University Friedrich-Alexander of Erlangen-Nuremberg, Germany.

[109] Kapat, S. and Krein, P.T. (2010). *PID controller tuning in a DC-DC converter: A geometric approach for minimum transient recovery time*. Control and Modeling for Power Electronics (COMPEL), IEEE 12th Workshop on, 1-6, 2010.

[110] Wu, Z. Zhao, J. and Zhang, J. (2006). *Cascade PID Control of Buck-Boost-Type DC/DC Power Converters*. Published in Intelligent Control and Automation, WCICA 2006, The Sixth World Congress on, 8467-8471.

[111] Adnan, M. F. Oninda, M. Nishat, M. and Islam, N. (2017). *Design and Simulation of a DC - DC Boost Converter with PID Controller for Enhanced Performance*. International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, Vol. 6 Issue 09.

[112] Mitulkumar, R. and Dave, K. C. (2012). *Analysis of boost converter using pi control algorithms*. International Journal of Engineering Trends and Technology 3.2: 71-73.

[113] Khwan-on, S. and Kongkanjana, K. (2017). *The Control of a Multi-Input Boost Converter for Renewable Energy System Applications*. Thailand: 5th International Electrical Engineering Congress, 8-10 March.

[114] Shareef, H. Mutlag, A. and Mohamed, A. (2015). *A novel approach for fuzzy logic PV inverter controller optimization using lightning search algorithm*. Neuro computing Vol. 168, pages 435-453.

[115] Shreeraman, R. Rajamayyoor, S. and Hari, B. (2012). *PID Controller Tuning Techniques: A Review*. Journal of Control Engineering and Technology (JCET), Vol. 2, Iss. 4.

[116] Erickson, W. (2007). *DC-DC Power Converters*. [Online] wiley online library-encyclopedia of electrical and electronics engineering. Available at: https://onlinelibrary.wiley.com/doi/abs/10.1002/047134608X.W5808.pub2.[Accessed 06 July 2018].

[117] Wikipedia, (2009). *Boost Converter*. [Online] Wikipedia the free encyclopedia. Available at: https://en.wikipedia.org/wiki/Boost_converter. [Accessed 05 July 2018].

[118] Wikipedia, (2013). *Power Electronics*. [Online] Wikipedia the free encyclopedia. Available at: https://en.wikipedia.org/wiki/Power_electronics. [Accessed 10 July 2018].

[119] Cyril, B. (2006). *Power Semiconductor Devices*. [Online] Wikipedia the free encyclopedia. Available at: https://en.wikipedia.org/wiki/Power_semiconductor_device#/media/File:Switches_domain.svg. [Accessed 05 February 2016].

[120] Rajashekara, K. Bhat, A. and Bose, B. (2000). *Power Electronics / Power semiconductors Devices*. The electrical engineering handbook, CRC Press LLC.

[121] Mueller, O. (1996). *Cryo-MOSFET and IGBT a Comparison*. Journal de Physique IV Colloque, 06 (C3), pp.C3-219-C3-224.

[122] Hassanain, B. (2008). *Design and Simulation of DC-DC Boost Converter*. IEEE Transactions on Power Electronics.

[123] © [2017] IEEE. Reprinted, with permission, from [Alzgool, M. and Nouri, H., *Design, Control and Modelling of a Novel Multi-Input Multi-Output Boost Converter Hub,* Amman: the 10th Jordan International Electrical and Electronics Engineering Conference (JIEEEC), May/ 2017].

[124] ABB group, (2015). *Economic-and-environmental-advantages*. [Online]. ABB Group. Available at: http://new.abb.com/systems/hvdc/why-hvdc/economic-and-environmental-advantages. [Accessed 05 July 2018].

[125] Reddy, M. Kalyani, Ch. Uthra M. and Elangovan, D. (2015). *A Small Signal Analysis of DC-DC Boost Converter*. Indian Journal of Science and Technology, Vol 8(S2), 1-6, January.

[126] Barberis Negra, N. Todorovic, J. and Ackermann, T. (2006). *Loss evaluation of HVAC and HVDC transmission solutions for large offshore wind farms.* Electric Power Systems Research 76 (2006) 916–927.

[127] Sengupta, U. (2006). *PWM and PFM Operation of DC/DC Converters for Portable Applications*. TI Portable Power Design Seminar, Topics 7, TI Literature No. SLPT015.

[128] Green, M. (2012). *Design Calculations for Buck-Boost Converters*. Texas Instruments Incorporated and its subsidiaries.

[129] Addula, S. and Prabhakar, M. (2017). *A Soft Switched Interleaved High Gain DC-DC Converter*. Journal of Engineering Science and Technology, Vol. 12, No. 9.

[130] Rao, N. and Chamund, D. (2014). *Power control through innovation/Power loss in IGBT*.

[131] International Rectifier Company, (2013). *Energy saving products*. [Online]. Available at: http://www.irf.com/reference-designs/design-family/_/N~1njcjd. [Accessed 05 July 2016].

[132] Bhat, Subramanya, X. and Nagaraja, H. N. (2014). *Effect of Parasitic Elements on the Performance of Buck-Boost Converter for PV Systems*. International Journal of Electrical and Computer Engineering 4.6.

[133] Abdolkarem and Salem. (2014). *DC-DC Boost Converter by H-infinity Controller*.

[134] Jamali and Hasmah, S. (2012). *Voltage tracking of DC-DC boost converter using Gaussian Fuzzy Logic Controller*. Malaysia: Diss. Universiti Tun Hussein.

[135] Atherton, P. (2009). *What is control engineering*. Control Engineering, publishing ApS, ISBN 978-87-7681-466-3.

[136] Smith, B. (2002). *Classical vs Intelligent Control*. [online]. Available at: https://www.engr.mun.ca/~baxter/Publications/ClassicalvsIntelligentControl. [Accessed 22 February 2017].

[137] Guo, L. Hung, J. and Nelms, R. (2009). *Evaluation of DSP-Based PID and Fuzzy Controllers for DC – DC Converters*. IEEE Transactions on Industrial Electronics. Vol. 56, No. 6, pp. 2237–2248.

[138] Biswal, M. (2011). *Control techniques for DC-DC Buck converter with improved performance*. [Online]. Available at: [http://ethesis.nitrkl.ac.in/2976/1/Thesis.pdf]. [Accessed 15 February 2017].

[139] Jha, V. Rai, P. (2012). *State Space Averaged Modelling of Basic Converter Topologies*. Published in VSRD International Journal of Electrical, Electronics, and Communication Engineering, vol. 2, no. 8, pp. 566-575.

[140] Fronczak and Kevin, (2013). *Stability analysis of switched dc-dc boost converters for integrated circuits*. Rochester: Rochester Institute of Technology.

[141] Marlin, T. (2015). *Process Control-Designing Processes and Control Systems for Dynamic Performance*. United State.

[142] Albertos, P. and Mareels, I. (2010). *Feedback and Control for Everyone*. Berlin: ISBN 978-3-642-03445-9.

[143] Anagnost, J. Desoer, C. (1991). *An elementary proof of the Routh-Hurwitz stability criterion circuits, systems and signal processing*. Volume 10, number 1, page 101.

[144] Wikibooks contributors, (2013). *Control Systems/Stability*. [online]. Available at: [https://en.wikibooks.org/w/index.php?title=Control_Systems/Stability&oldid=3418796]. [Accessed 05 May 2018].

[145] Quora authors. (2015). *Control engineering/ stability and poles location*. [online]. Available at: https://www.quora.com/How-stability-is-dependent-on-location-of-poles-in-the-characteristic-equation-of-control-systems. [Accessed 01 June 2017].

[146] Lee and Hoon, J. (2009). *A new PID controller with Lyapunov stability for regulation servo systems*. Published in Journal of Institute of Korean Electrical and Electronics Engineering (IKEEE).

[147] Close, C. Frederick, D. and Newell, J. (2001). *Modelling and Analysis of Dynamic Systems*. United States.

[148] Wikibooks contributors. (2013). *Control Systems/Bode_Plot*. [online]. Available at: [https://en.wikipedia.org/wiki/Bode_plot]. [Accessed 07 May 2018].

[149] Quora authors, (2015). *Control engineering/ Bode plot_Gain and phase margin*. [online]. Available at: [https://www.quora.com/In-which-condition-gain-margin-will-be-infinite]. [Accessed 03 June 2017].

[150] Sung, S. Lee, I. (1996). *Limitations and Countermeasures of PID Controllers*. Industrial & Engineering Chemistry journal, American Chemical Society.

[151] Gowtham, S. Balaji, M. Harish, S. Abraham Pinto, M. and Jagadeesh, G. (2017). *Fault Tolerant Single Switch PWM DC-DC Converters for Battery charging Applications*. Chennai: 1st International Conference on Power Engineering, Computing and control, (2- 4) March, VIT University, Chennai Campus.

[152] Deihimi, A. Mahmoodieh, M. E. S. and Iravani, R. (2017). *A new multi-input step-up DC–DC converter for hybrid energy systems*. Electr. Power Syst. Res., vol. 149, pp. 111–124.

[153] Chen, G. Jin, Z. Deng, Y. He, X. and Qing, X. (2017). *Principle and Topology Synthesis of Integrated Single-Input Dual-Output and Dual-Input Single-Output DC-DC Converters*. IEEE Trans. Power Electron, DOI 10.1109/TIE, 2760856.

[154] Deveci, O. Kasnakoglu, C. (2017). *MIMO nonlinear modelling and robust control of standalone dc photovoltaic systems*. International Journal Hydrogen Energy, 10.1016/j.ijhydene.2017.04.033.

[155] Augusti Lindiya, S. Palani, S. and Vijayarekha, K. (2017). *Modelling and Simulation of Photovoltaic System Fed Two Input Two Output DC-DC Boost Converter Interfaced with Asymmetric Cascaded H-Bridge Multilevel Inverter*. Indian Journal of Science and Technology, Vol 10(5), DOI: 10.17485/ijst/2017/v10i5/111139.

[156] Usha Anandhi, M. and Vimal Bharathi, N. (2016). *A Nonisolated Multiinput Multioutput DC–DC Boost Converter for Different Voltage Requirements*. International Journal of Advanced Engineering Research and Technology (IJAERT), Vol 4 Issue 5, ISSN No.: 2348 – 8190.

[157] Alves de Melo Bento, A. Diego Roberto Cabral da Silva, A. (2016). *Dual Input Dual Output Single Switch DC-DC Converter for Renewable Energy Applications*. IEEE Trans. Power Electron, 978-1-5090-0737-0/16/$31.00.

[158] Mohan Raj, K. Narayana Mohan, G. and Sekhar Dash, S. (2016). *Single Stage Multi Input DC-DC/AC Boost Converter with Sliding Mode Control*. Indian Journal for science and Technology, Vol 9, Issue 38, 603203.

[159] Babaei, E. and Abbasi, O. (2016). *Structure for multi-input multi-output dc-dc boost converter*. IET Power Electron, vol. 9, no. 1, pp. 9–19.

[160] Fathabadi, H. (2016). *Novel high efficiency DC/DC boost converter for using in photovoltaic systems.* Sol. Energy, 125, pp. 22-31.

[161] Hu, X. and Gong, C. (2015). *A high gain input-parallel output-series DC/DC converter with dual coupled inductors*. IEEE Trans. Power Electron, vol. 30, no. 3, pp. 1306–1317.

[162] Jayashankar, V. and Uma, R. (2015). *A Transformerless Multiinput Multioutput DC–DC Boost Converter Using Fuzzy Logic Controller for Electric Vehicle Applications*.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering. Vol. 4, Issue 9.

[163] Pan, C. T. Chuang, C. F. and Chu, C. C. (2014). *A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress*. IEEE Trans. Power Electron, vol. 29, no. 9, pp. 4787–4796.

[164] Pradeep, D. Dhamodharan, S. Vidhya, R. Arun, V. Rajkumar, M. Rajapandi, P. and Sampath, S. (2015). *Innovative DC-DC converter for hybrid energy sources using Multi-Inputs*. International Journal of Computer Science and Mobile Applications, Vol.3 Issue. 3.

[165] Tang, Y. Fu, D. Wang, T. and Xu, Z. (2015). *Hybrid switched-inductor converters for high step-up conversion*. IEEE Trans. Ind. Electron., vol. 62, no. 3, pp. 1480–1490.

[166] Khadmun, W. and Subsingha, W. (2013). *High voltage gain interleaved dc boost converter application for photovoltaic generation system*. Elsevier Energy Procedia, vol. 34, pp. 390–398.

[167] AI-Saffar, M. A. and Ismail, E. H. (2014). *A high voltage ratio and low stress DC-DC converter with reduced input current ripple for fuel cell source*. Renewable Energy.

[168] Scoltock, J. Lopez, G. and Wang, Y. (2017). *Design optimisation and trade-offs in multi-kW DC-DC converters*. Manchester: School of Electrical and Electronic Engineering. The University of Manchester, United Kingdom.

[169] © [2018] IEEE. Reprinted, with permission, from [Alzgool, M. and Nouri, H., *PID Controller Design for a Novel Multi-Input Multi-Output Boost Converter Hub*, Journal of Electrical Engineering (JEA), Vol 2, No 1, 2018].

[170] Infographic-Canva. (2018). *Renewable and Non-renewable energy sources*. [online]. Available at: [https://www.canva.com/design/DAC8lQ1V4ow/UMJ9aWxRFVt7s_Pq5tltxQ/edit]. [Accessed 07 July 2018].

Appendices

Appendix A

Companies' quotations for pricing requirements

HIGH VOLTAGE (INDIA),

C-335, 3rd main, 1st stage,Peenya Industrial Estate, Bangalore.
Mob.No. : 09341892339 email : contact@highvoltage.co.in

QN/HV/2804/2018-19 28-04-2018

To,
Mais.

Sir,

Sub : Quotation.

Ref : Your mail dated 18-04-2018.

We feel pleasure in submitting our lowest quotation for the followings:

S.No	Particulars	Amount (each)
1	10 mfd, 2.75 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 270/-
2	2.5 mfd, 1 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 170/-
3	25 mfd, 11 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 1,520/-
4	10.5 mfd, 3.6 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 340/-
5	5 mfd, 2 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 240/-
6	32 mfd, 11 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 1,860/-
7	10 mfd, 11 kV High Voltage DC Capacitor as per drawing & Technical Specification	USD 760/-

Our offer is subject to the following conditions :

a) Prices : Our prices are ex-factory.
b) Packing, forwarding and freight and insurance: USD 1,500/-.
c) Delivery : 10 - 12 weeks after the receipt of your firm order.
d) Payments : 100% advance against proforma by T/T.
e) Order mode : Order to be placed with our export agency:

Allied Marketing
M-408,7th Cross,1st Stage,Peenya Industrial Estate,Bangalore-560058.
Ph.No.: 080-65734517.
email : contact@alliedmarketing.in

f) Bank details : Name : Allied Marketing
A/c.No. : 64096784906
BANK : State Bank of India, Peenya Branch, 1st stage,
Peenya Industrial area,Bangalore -560058.
CODE : SBIN0040284

Should you require any further clarification, please do not hesitate to contact us on 00919341892339.

Thanking you.

Truly yours,
(Dr.Bhagwant Singh)

Saluos for supply

Date: 20/05/2018
Dear: Mais al zgool

Inductors

Inductance (H)	DC Current rating (A)	Unite prices$
27 m /630uH	414 /450A	3850
995 u /375uH	140	3268
2 m /313 uH	180 /200A	3455
91 m / 527uH	80 /75A	2280

IGBTs power switch

$frequency$=1kHz

Maximum operating voltage V_{CE} (kV)	Maximum operating power (kW)	Unite prices$
1	180 -200	6500
11	880-1000	0000
3.6 -3.5	1490	27950
2	1490	11450
2.75	385 -500	16750

Diodes

Maximum forward voltage (kV)	Maximum forward current (A)	Unite prices$
3.6 -4	63	895
11	11	5200
9 -10	11	4750
1	60	273
2.75	17	499
5.5	11	1700

Delivery day 2-8 weeks

Amman Jordan –telefax: 0096264615966,0096264650966, 0096264618966

Appendix B

Publications

53-167-2-CE

PID controller design for a novel multi-input multi-output boost converter hub

M Alzgool, H Nouri

Power Systems, Electronics and Control Research Laboratory, UWE Bristol, UK

Mais2.alzgool@live.uwe.ac.uk

ABSTRACT

This paper reports on the design, control, and modeling of a novel multi-input multi-output boost converter topology. The converter hub can integrate renewable energy sources such as wind turbines, photovoltaic arrays, and fuel cells for the provision of different output voltage levels. The advantage of energy sources integration is that the required output voltage levels could be made up from a range of sources. The designed converter has the advantages of a simple configuration, fewer components, high conversion ratio, and high efficiency. The regulated output voltage levels are achieved through classical PID controllers which utilize the concept of closed-loop voltage-mode control. Design of the converter control system requires comprehensive knowledge of the converter structure, its operation principle and the small-signal model for continuous-conduction operation mode. The validity of the converter's control performance is demonstrated through software simulation.

KEY WORDS**:** DC-DC Converter, Multi-Input Multi-Output (MIMO), Renewable energy, small signal modelling, state space averaging, Insulated Gate Bipolar Transistor (IGBT)

1. INTRODUCTION

Recently, the number of applications which require more than one power source or more than one kind of energy source is increasing. Generating multi-input converters, having the capability of diversifying different energy sources, will provide improved reliability and the system flexibility.

Many control methods are used for controlling DC-DC converters where the simple and low-cost controller structure is always in demand for most industrial and high-performance applications [1]. Most used technique to control switching power supplies is pulse width modulation [2].

When boost converter is employed in open loop mode, it exhibits poor voltage regulation and unsatisfactory dynamic response, and hence, this converter is provided with closed-loop control for output voltage regulation. Hence, various closed-loop techniques had been proposed such as PID controller, Fuzzy logic, and other techniques, as well as many other researchers came up with new designs to be controlled with appropriate control technique such as using soft switching technique [3,4] presented high-frequency power switches design and robust controller.

In controlling the DC-DC converters, a voltage mode control or current mode control could be applied simply by closing a feedback loop between the required output voltages and switching device's duty ratio signal [2]. Due to nonlinearity of current mode control dynamics, the difficulties of obtaining the small-signal model is achieved; furthermore, in current mode control, an additional inner feedback loop is needed to control the inductor current, and then the output voltage is regulated indirectly [5], thus the current mode control is more complex to implement than voltage mode control.

Within closed-loop system, PID control is considered as a traditional linear control method commonly used in many applications [6]. The PID controller is a popular control feedback used in industrial area due to its flexibility and easy implementation in real applications; furthermore, if the system is complex, the PID can be designed to track an error and assume the system as a black box. A PID controller calculates an error value as the difference between the measured value and the desired reference value [7], and by adjusting three parameters k_p, k_i, and k_d of the system which would affect the transient response, rise time, settling time and steady-state error, overshoot, and stability. Thus, it may not necessary for the system to utilize the three actions P, I, and D; it may use one or two actions to improve the system dynamic response.

In this paper, closed-loop voltage-mode control using a PID controller is employed to control the multi-input multi-output (MIMO) DC-DC boost converter topology structure as shown in Figure 1, where different input sources connected in such a way to integrate the available input sources to provide a high conversion ratio [8].

The paper organized as follows: Section 2 presents the proposed MIMO DC-DC boost converter topology with the mathematical representation for ideal and non-ideal converter. Furthermore, the operation principle of the proposed converter is presented in section 2. The dynamic modeling of the DC-DC boost converter for three-input source double output is presented in section 3 including the MATLAB simulation results. Finally, the conclusion of this study is summarized in section 4.

2. CONVERTER STRUCTURE AND OPERATION PRINCIPLES

A new design and efficient MIMO DC-DC boost converter is proposed with the specifications of high conversion ratio and lower number of components in comparison to the available MIMO boost converter topologies.

In this design, the stepping up voltage occurs in two stages, where the output voltage of the first stage (V_o) acts like the DC input voltage to the next stage, so that to provide a higher conversion ratio, which is important in high DC voltage applications.

The mathematical equations of the proposed MIMO boost converter have been derived assuming that the system is lossless (ideal components):

$$V_{o1} = \left[\frac{V_{i1}}{1-D_{i1}} + \frac{V_{i2}}{1-D_{i2}} + \frac{V_{i3}}{1-D_{i3}} + \ldots + \frac{V_{im}}{1-D_{im}}\right]\left[\frac{1}{1-D_{o1}}\right] \tag{1}$$

$$V_{on} = \left[\sum_{k=1}^{k=m} V_{ik}\frac{1}{1-D_{ik}}\right]\left[\frac{1}{1-D_{on}}\right] \tag{2}$$

Where,
V_{on} is the output DC voltage.
V_{ik} is the DC input voltage.

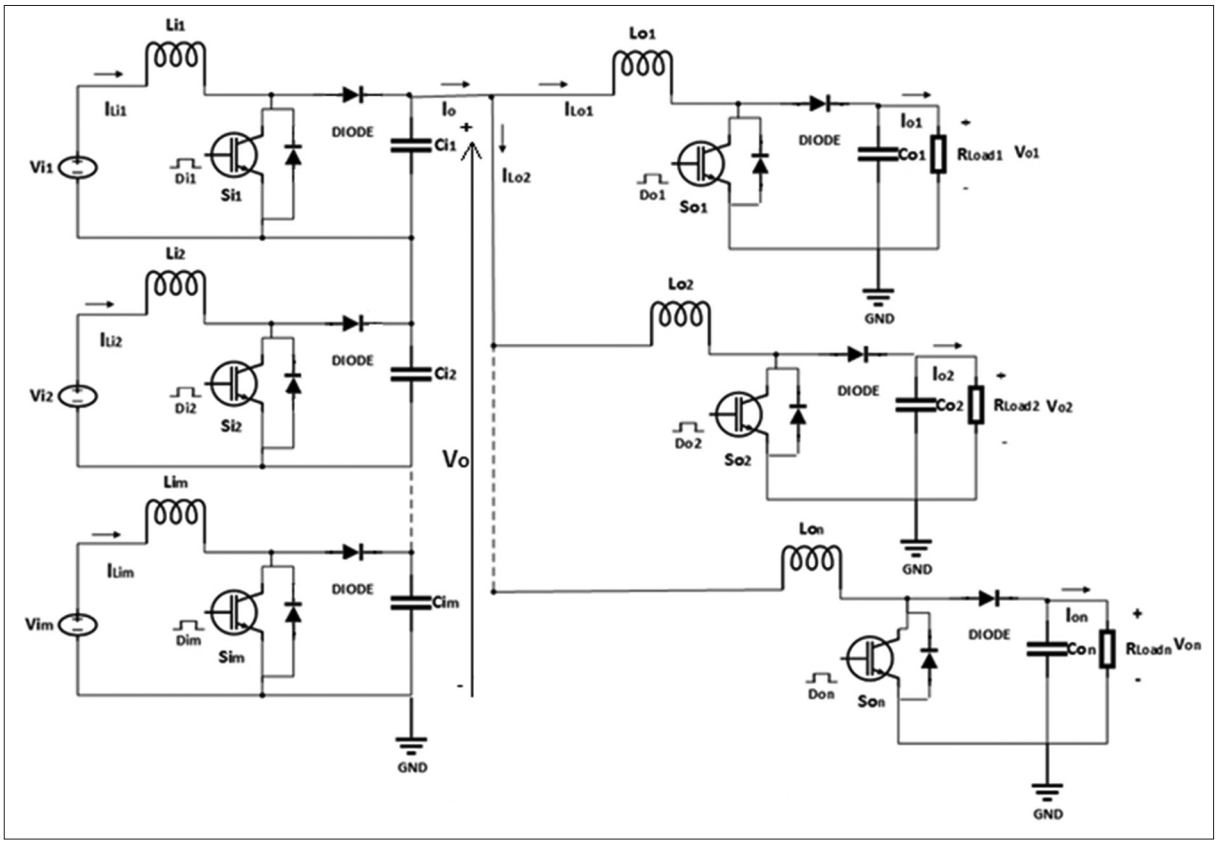


Figure 1. *Proposed multi-input multi-output DC-DC boost converter topology*

D_{ik} is the duty cycle of the input IGBT switches.
D_{on} is the duty cycle of the output IGBT switches.

From Equation (2), the conversion ratio of the proposed converter is expressed as:

$$\frac{V_{on}}{V_{im}} = \frac{m}{(1-Di)(1-Don)}; \text{ if } (D_{i1} = D_{i2} = D_{im} = D_i) \tag{3}$$

Where, m is the number of inputs of the proposed converter and n is the number of outputs.

If the conversion ratio of the proposed converter in Equation (3) is compared to the conversion ratio of the classical boost converter shown below in Equation (4).

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{4}$$

It is noticeable that the conversion ratio of the proposed converter is much higher than the classical boost as shown in Figure 2. For example, the classical boost conversion ratio for 80% duty cycle will be 5 while, for the same condition, the conversion ratio of the proposed single-input single-output (SISO) boost converter will be 25, which means 5 times more than the classical boost conversion ratio. In the same figure, you can see how the conversion ratio increases as the number of inputs increase.

Where $(D_{i1} = D_{i2} = D_{im} = D_{on})$

Moreover, for non-ideal components, the mathematical equations of the proposed MIMO converter by the inductor volt-second balance approach have been derived. Thus, the general equation of the non-ideal (including losses) MIMO boost converter output voltage will be:

$$V_{on(non-ideal)} = \left[\frac{1}{1-D_{on}}\right]\left[\sum_{k=1}^{k=m} V_{ik}\frac{1}{1-D_{ik}}\right] - \left[\sum_{k=1}^{k=m} V_{S_{ik-ON}}\frac{1}{(1-D_{ik})(1-D_{on})} - \frac{1}{(1-D_{ik})(1-D_{on})}\right] - I_{L_k}\left(R_{S_{ik}} - R_{L_{ik}}\right) - V_{DIODE_{ik-ON}} \tag{5}$$

$$\left[\sum_{j=1}^{j=n} V_{S_{oj-ON}}\left(\frac{D_{oj}}{1-D_{oj}}\right) - I_{L_{oj}}R_{L_{oj}}\left(\frac{D_{oj}}{1-D_{oj}}\right) - V_{DIODE_{oj-ON}}\right]$$

Where,
$V_{S_{ik-ON}}$ is the input IGBT-ON state voltage drop which is between two to three volts.

$V_{S_{oj-ON}}$ is the output IGBT-ON state voltage drop which is between two to three volts.

$V_{DIODE_{k,oj-ON}}$ is the diode forward voltage.

$R_{S_{ik}}$ and R_{L_k} are the DC resistance of the voltage source and the inductor, respectively.
$I_{L_{ik,oj}}$ is the input and output inductor current.

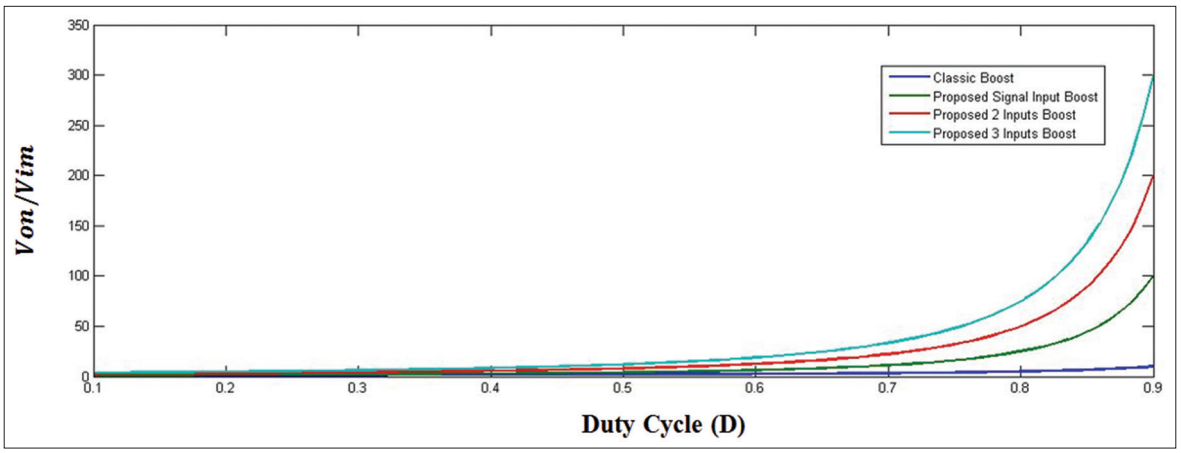


Figure 2. *Comparison between the conversion ratio of the proposed converter and the classical boost converter*

It is clear that the output voltage drops when the losses included, thus the converter's efficiency decreases [8], for example, if the efficiency of the proposed double inputs single output ideal converter 100%, then the efficiency of the non-ideal converter drops to reach 95.8% which is <4.2% of the ideal converter's efficiency due to losses. Figure 3 depicts the efficiency of the ideal and non-ideal converter with different number of outputs.

As the number of output increases the converter's efficiency decreases (for ideal and non-ideal converter) as more power switches conducted, and the output current will be reduced as the number of output increases to feed the whole loads. In spite of the losses of the proposed non-ideal converter, a high efficiency is acquired.

In this paper, three-input sources V_{i1}, V_{i2}, and V_{i3} are responsible for supplying the loads. The converter is designed to operate in continuous-conduction mode as the inductor current never reaches zero. In this mode, the five switches are active, and for each switch, a specific duty ratio is considered. Here, S_{i1} is active to regulate the first input source V_{i1} current to desired value. At the same time, S_{i2} and S_{i3} are active to regulate V_{i2}, V_{i3}, respectively, by controlling the input inductor currents IL_{i2} and IL_{i3}. By regulating the duty ratios of the input switches the DC bus voltage V_0 whrer ($V_0 = V_{c1} + V_{c2} + V_{c3}$). Furthermore, the output voltage V_{o1} is controlled by the output power switch S_{o1}; similarly, S_{o2} regulates the second output voltage V_{o2}. According to the switches' states, there are four different switching states in one switching period as shown in Figure 4. For each state, the inductor and capacitor equations have been investigated as follows:

a. Switching state 1: In this state, the switches on the input side S_{i1}, S_{i2}, and S_{i3} are turned ON, while the output switches S_{o1} and S_{o2} are turned OFF. When the input switches are ON, the input stage diodes are reversed biased, so S_{o1} and S_{o2} are OFF. Assuming that the output capacitors are fully charged, thus the power will deliver to the load R_{L1} and R_{L2}. The equivalent circuit of the proposed converter in this state is shown in Figure 4a. In this state, V_{i1}, V_{i2}, and V_{i3} charge the inductors L_{i1}, L_{i2}, and L_{i3}, respectively, so the inductors' current increases and the output capacitors are discharged.

   The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned}
L_{i1}\frac{di}{dt} &= v_{i1}\\
L_{i2}\frac{di}{dt} &= v_{i2}\\
L_{i3}\frac{di}{dt} &= v_{i3}\\
C_{i1}\frac{dv_{ci1}}{dt} &= -i_o\\
C_{i2}\frac{dv_{ci2}}{dt} &= -i_o\\
C_{i3}\frac{dv_{ci3}}{dt} &= -i_o\\
L_{o1}\frac{di}{dt} &= v_o - v_{co1}\\
L_{o2}\frac{di}{dt} &= v_o - v_{co2}\\
C_{o1}\frac{dv_{co1}}{dt} &= i_{Lo1} - \frac{v_{o1}}{R_{L1}}\\
C_{o2}\frac{dv_{co2}}{dt} &= i_{Lo2} - \frac{v_{o2}}{R_{L2}}
\end{aligned}\right\} \quad (6)$$

b. Switching state 2: In this state, the switches on the input side S_{i1}, S_{i2}, and S_{i3} are still ON, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are ON, the input stage diodes are reversed biased. Assuming that the output capacitors are fully charged, thus the power will deliver to the load R_{L1} and R_{L2}. The equivalent circuit of the proposed converter in this state is shown in Figure 4b. In this state, V_{i1}, V_{i2}, and V_{i3} charge the inductors L_{i1}, L_{i2}, and L_{i3}, respectively, also the output inductors L_{o1} and L_{o2} are charged from the capacitors C_{i1}, C_{i2}, and C_{i3}. Consequently, the inductors' current IL_{o1} and IL_{o2} increases. In addition, capacitors C_{o1} and C_{o2} are discharged. The equations for the inductors and capacitors in this mode are as follows:

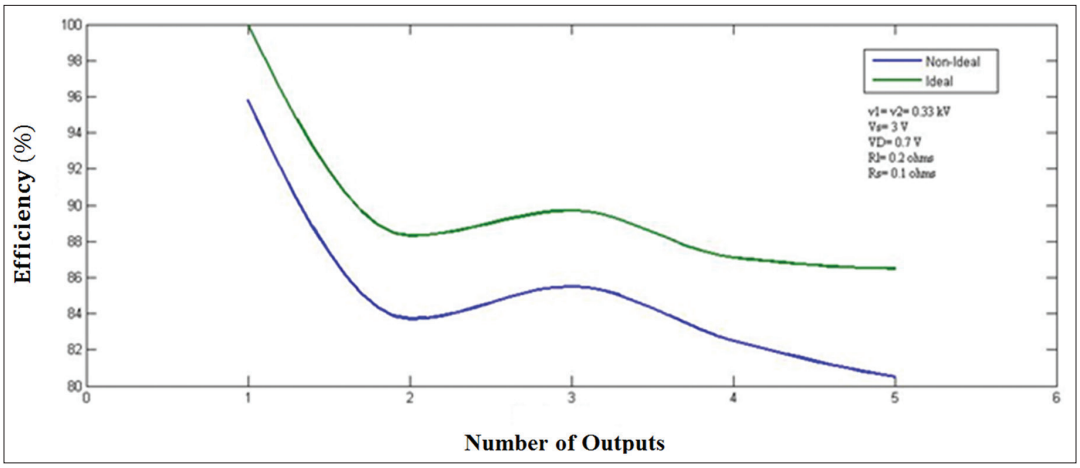


Figure 3. *The converter's efficiency of the ideal and non-ideal converter with different number of outputs*

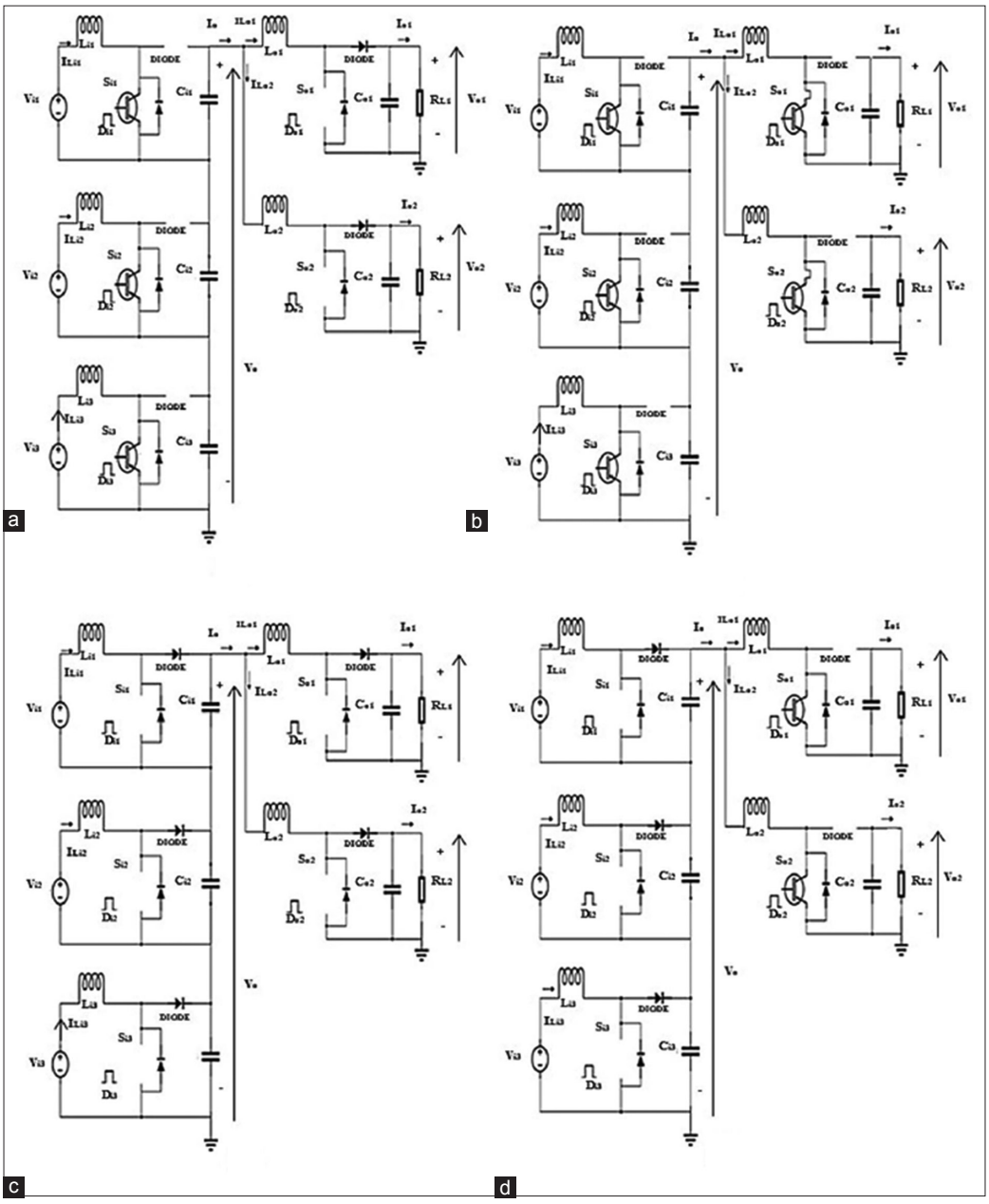


Figure 4. *Equivalent circuit of boost converter switching mode, (a) switching state 1, (b) switching state 2, (c) switching state 3, (d) switching state 4*

$$\left.\begin{aligned}
L_{i1}\frac{di}{dt} &= v_{i1}\\
L_{i2}\frac{di}{dt} &= v_{i2}\\
L_{i3}\frac{di}{dt} &= v_{i3}\\
L_{o1}\frac{di}{dt} &= v_{o}\\
L_{o2}\frac{di}{dt} &= v_{o}\\
C_{i1}\frac{dv_{ci1}}{dt} &= -\left(i_{Lo1}+i_{Lo2}\right)\\
C_{i2}\frac{dv_{ci2}}{dt} &= -\left(i_{Lo1}+i_{Lo2}\right)\\
C_{i3}\frac{dv_{ci3}}{dt} &= -\left(i_{Lo1}+i_{Lo2}\right)\\
C_{o1}\frac{dv_{co1}}{dt} &= \frac{-v_{o1}}{R_{L1}}\\
C_{o2}\frac{dv_{co2}}{dt} &= \frac{-v_{o2}}{R_{L2}}
\end{aligned}\right\} \quad (7)$$

c. Switching state 3: In this state, the switches on the input side S_{i1}, S_{i2}, and S_{i3} are turned OFF, and the output switches S_{o1} and S_{o2} are turned OFF. When the input switches are OFF, the input stage diodes are forward biased. In this state, the stored energy in the input inductors will deliver to charge the capacitors C_{i1}, C_{i2}, and C_{i3}. In addition, the stored energy in the output inductors will deliver to charge the output capacitors C_{o1} and C_{o2}, as well as to deliver the stored energy to the loads R_{L1} and R_{L2}. The equivalent circuit of the proposed converter in this state is shown in Figure 4c. In this state, the inductors' current IL_{i1}, IL_{i2}, and IL_{i3} decreases and the capacitors C_{i1}, C_{i2}, and C_{i3} charged. The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned}
L_{i1}\frac{di}{dt} &= v_{i1} - v_{ci1}\\
L_{i2}\frac{di}{dt} &= v_{i2} - v_{ci2}\\
L_{i3}\frac{di}{dt} &= v_{i3} - v_{ci3}\\
L_{o1}\frac{di}{dt} &= v_{o} - v_{co1}\\
L_{o2}\frac{di}{dt} &= v_{o} - v_{co2}\\
C_{i1}\frac{dv_{ci1}}{dt} &= i_{Li1} - i_{o}\\
C_{i2}\frac{dv_{ci2}}{dt} &= i_{Li2} - i_{o}\\
C_{i3}\frac{dv_{ci3}}{dt} &= i_{Li3} - i_{o}\\
C_{o1}\frac{dv_{co1}}{dt} &= i_{Lo1} - \frac{v_{o1}}{R_{L1}}\\
C_{o2}\frac{dv_{co2}}{dt} &= i_{Lo2} - \frac{v_{o2}}{R_{L2}}
\end{aligned}\right\} \quad (8)$$

d. Switching state 4: In this state, the switches on the input side S_{i1}, S_{i2}, and S_{i3} are still OFF, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are OFF, the input stage diodes are forward biased. In this state, the stored energy in the input inductors keeps charging the capacitors C_{i1}, C_{i2}, and C_{i3}. In addition, the stored energy in the input inductors will deliver to L_{o1} and L_{o2} through the switches S_{o1} and S_{o2}, respectively. Hence, the

inductors' current IL_{i1}, IL_{i2}, and IL_{i3} keep decreasing, while IL_{o1} and IL_{o2} increases. In addition, the capacitors C_{o1} and C_{o2} will discharge through the loads R_{L1} and R_{L2}. The equivalent circuit of the proposed converter in this state is shown in Figure 4d. The equations for the inductors and capacitors in this mode are as follows:

$$\left.\begin{aligned}
L_{i1}\frac{di}{dt} &= v_{i1} - v_{ci1}\\
L_{i2}\frac{di}{dt} &= v_{i2} - v_{ci2}\\
L_{i3}\frac{di}{dt} &= v_{i3} - v_{ic3}\\
L_{o1}\frac{di}{dt} &= v_o\\
L_{o2}\frac{di}{dt} &= v_o\\
C_{i1}\frac{dv_o}{dt} &= i_{Li1} - i_o\\
C_{i2}\frac{dv_o}{dt} &= i_{Li2} - i_o\\
C_{i3}\frac{dv_o}{dt} &= i_{Li3} - i_o\\
C_{o1}\frac{dv_{co1}}{dt} &= \frac{-v_{o1}}{R_{L1}}\\
C_{o2}\frac{dv_{co2}}{dt} &= \frac{-v_{o2}}{R_{L2}}
\end{aligned}\right\} \quad (9)$$

3. DYNAMIC MODEL OF THE DC-DC BOOST CONVERTER

The MIMO converter is controlled by switches S_{i1}, S_{i2}, S_{i3} and S_{o1}, S_{o2}. Each switch has its own specific duty cycle. By proper regulation of switches' duty cycles, the outputs voltage, namely, V_{o1} and V_{o2} can be adjusted. To design the closed-loop controller for the converter, it is necessary to obtain the dynamic model. As stated before in section 2, to control the output voltages, regulating the bus DC voltage V_o is also needed. In addition, as each input has its own power switch and different parameters values, thus different controllers need to be designed. Figure 5 depicts the control block diagram of the proposed converter with three inputs and two outputs.

Small-signal model is the basis for optimized controller design. Especially, for MIMO converters, an effective model will aid to realize closed-loop control and to optimize the converter dynamics [1]. Unlike the conventional SISO converters, the MIMO converter is a high order system, and the derivation of the plant transfer function is extensive; therefore, it is difficult to obtain values of poles and zeros for analysis.

The dynamics of the plant can be described in a matrix form. Based on small-signal modeling method [2], the state variables (x) and duty ratios (d), input voltages (v) contain two components, dc values (X, D, V) and disturbance values $(\hat{x},\hat{d},\hat{v})$. It is assumed that the perturbations are small and do not vary significantly during one switching period. Hence, the proposed converter equations are as follows:

$$\left.\begin{aligned}
i_{Li}(t) &= I_{Li} + \hat{i}_{Li}(t)\\
i_{Lo}(t) &= I_{Lo} + \hat{i}_{Lo}(t)\\
v_{o1}(t) &= V_{o1} + \hat{v}_{o1}(t)\\
v_{o2}(t) &= V_{o2} + \hat{v}_{o2}(t)\\
d_{i1}(t) &= D_{i1} + \hat{d}_{i1}(t)\\
d_{i2}(t) &= D_{i2} + \hat{d}_{i2}(t)\\
d_{i3}(t) &= D_{i3} + \hat{d}_{i3}(t)\\
d_{o1}(t) &= D_{o1} + \hat{d}_{o1}(t)\\
d_{o2}(t) &= D_{o2} + \hat{d}_{o2}(t)
\end{aligned}\right\} \quad (10)$$

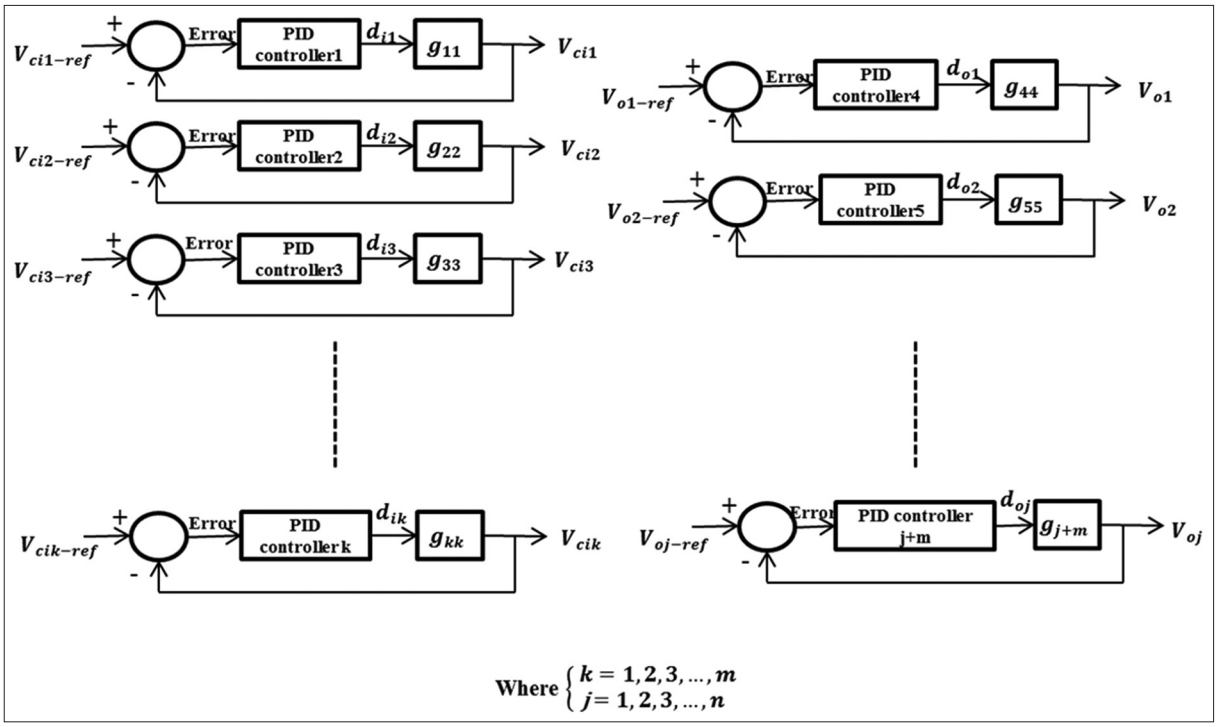


Figure 5. *The control block diagram of the proposed converter*

Where, iLi (t) and iLo (t) the input and output inductors' current and where the output capacitors' voltage v_{o1} (t) and v_{o2} (t) are state variables. Substitutes (10) into (6-9), then the averaging model is applied and multiplied by its corresponding duty cycle value. Hence, the system can be represented in a matrix form using a state-space averaging model. The state-space model takes the following form:

$$\left.\begin{aligned} \frac{dX}{dt} &= AX+BU \\ Y &= CX+DU \end{aligned}\right\} \tag{11}$$

Where, X is a matrix containing the state variables, U is a matrix containing the control inputs $\hat{d}_{i1}(t), \hat{d}_{i2}(t), \hat{d}_{i3}(t), \hat{d}_{o1}(t), \hat{d}_{o2}(t)$, and Y is a matrix containing the system outputs $\hat{v}_o(t), \hat{v}_{o1}(t), \hat{v}_{o2}(t)$.

Matrixes X, Y, and U take following form:

$$X = \begin{bmatrix} \hat{i}_{Li1}(t) \\ \hat{v}_{ci1}(t) \\ \hat{i}_{Li2}(t) \\ \hat{v}_{ci2}(t) \\ \hat{i}_{Li3}(t) \\ \hat{v}_{ci3}(t) \\ \hat{i}_{Lo1}(t) \\ \hat{v}_{co1}(t) \\ \hat{i}_{Lo2}(t) \\ \hat{v}_{co2}(t) \end{bmatrix}, Y = \begin{bmatrix} \hat{v}_{ci1}(t) \\ \hat{v}_{ci2}(t) \\ \hat{v}_{ci3}(t) \\ \hat{v}_{o1}(t) \\ \hat{v}_{o2}(t) \end{bmatrix}, U = \begin{bmatrix} \hat{d}_{i1}(t) \\ \hat{d}_{i2}(t) \\ \hat{d}_{i3}(t) \\ \hat{d}_{o1}(t) \\ \hat{d}_{o2}(t) \end{bmatrix}$$

The transfer function matrix of the converter is obtained from the small-signal model from matrices A, B, C, and D as follows:

$$G = C(SI-A)^{-1}B+D \tag{12}$$

The rank of transfer function matrix depends on the control variables; so according to the number of control variables, the rank of transfer function matrix G is 5×5

Where,

$$y = Gu \tag{13}$$

$$\begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} & g_{15} \\ g_{21} & g_{22} & g_{23} & g_{24} & g_{25} \\ g_{31} & g_{32} & g_{33} & g_{34} & g_{35} \\ g_{41} & g_{42} & g_{43} & g_{44} & g_{45} \\ g_{51} & g_{52} & g_{53} & g_{54} & g_{55} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

Where, y and u are the system output and input vectors, respectively, and component g_{ij} represents the transfer function between y_i and u_j. Hence, there are five transfer functions as follows:

$$g_{11} = \frac{\hat{v}_{ci1}}{\hat{d}_{i1}} = \frac{v_{i1}}{\left((1-D_{i1})(1+\frac{L_{i1}C_{i1}}{(1-D_{i1})^2})S^2\right)} \tag{14}$$

$$g_{22} = \frac{\hat{v}_{ci2}}{\hat{d}_{i2}} = \frac{v_{i2}}{\left((1-D_{i2})(1+\frac{L_{i2}C_{i2}}{(1-D_{i2})^2})S^2\right)} \tag{15}$$

$$g_{33} = \frac{\hat{v}_{ci3}}{\hat{d}_{i3}} = \frac{v_{i3}}{\left((1-D_{i3})(1+\frac{L_{i3}C_{i3}}{(1-D_{i3})^2})S^2\right)} \tag{16}$$

$$g_{44} = \frac{\hat{v}_{o1}}{\hat{d}_{o1}} = \frac{V_o(1-\frac{L_{o1}}{(1-D_{o1})^2 R_{L1}}S)}{\left((1-D_{o1})(1+\frac{(1-D_{o1})^2 R_{L1}\sqrt{\frac{C_{o1}}{L_{o1}}}}{\sqrt{L_{o1}C_{o1}}})S+\frac{L_{o1}C_{o1}}{(1-D_{o1})^2}S^2\right)} \tag{17}$$

$$g_{55} = \frac{\hat{v}_{o2}}{\hat{d}_{o2}} = \frac{V_o(1-\frac{L_{o2}}{(1-D_{o2})^2 R_{L2}}S)}{\left((1-D_{o2})(1+\frac{(1-D_{o2})^2 R_{L2}\sqrt{\frac{C_{o2}}{L_{o2}}}}{\sqrt{L_{o2}C_{o2}}})S+\frac{L_{o2}C_{o2}}{(1-D_{o2})^2}S^2\right)} \tag{18}$$

In this paper, the simulation results for three different input DC sources chosen within these ranges (V_{i1} = (200-500)V, V_{i2} = (350-875) V, and V_{i3} = (250-625) V) as an example of a different wind turbines DC voltage levels. Two output DC voltages are obtained using the integration of PID controllers. The values of the converter parameters the inductors L and the capacitors C have been obtained as discussed in our previous paper [8]. The controller has been designed in such a way to provide the following requirements, for the DC bus voltage, e.g. V_o = 4 kV,V_{o1}=8 kV and V_{o2}=11 kV. Hence, by controlling the bus DC voltage V_o through the PID controllers on the first stage of the designed converter to adapt itself as these inputs changes, thus the next stage will provide controlling the output DC voltages as the load changes. Figure 6 depicts the simulation results using MATLAB software of three-input and two-output DC-DC boost converter including the load and input sources variations to test the performance of the closed-loop control.

According to the results obtained from the simulation of a three-input and two-output DC-DC converter model associated with PID controllers, these results demonstrate the flexibility and robustness of the designed controller. The DC voltage Vo remains fixed as the input sources reduced by 20% and when the load changes by 50% with no

overshoot and with small peak to peak ripple voltage $V_{o_{(ripple)(p-p)}} = 20$ volts.

Similarly, the performance of the designed controller with the output voltages V_{o1} and V_{o2} has been tested as shown in Figure 6b and the controller demonstrates its flexibility and robustness in terms of the ability of the controller to keep the output voltages V_{o1} and V_{o2} fixed when the loads or the inputs changes with a good performance, i.e., 9.3% overshoot peak for V_{o1} and 7.2% for the second output V_{o2}, as well as small peak current and voltage ripple where

$$V_{o1_{(ripple)(p-p)}} = V_{o2_{(ripple)(p-p)}} = 40\,V$$

and

$$I_{o1_{(ripple)(p-p)}} = I_{o2_{(ripple)(p-p)}} = 200\,mA$$

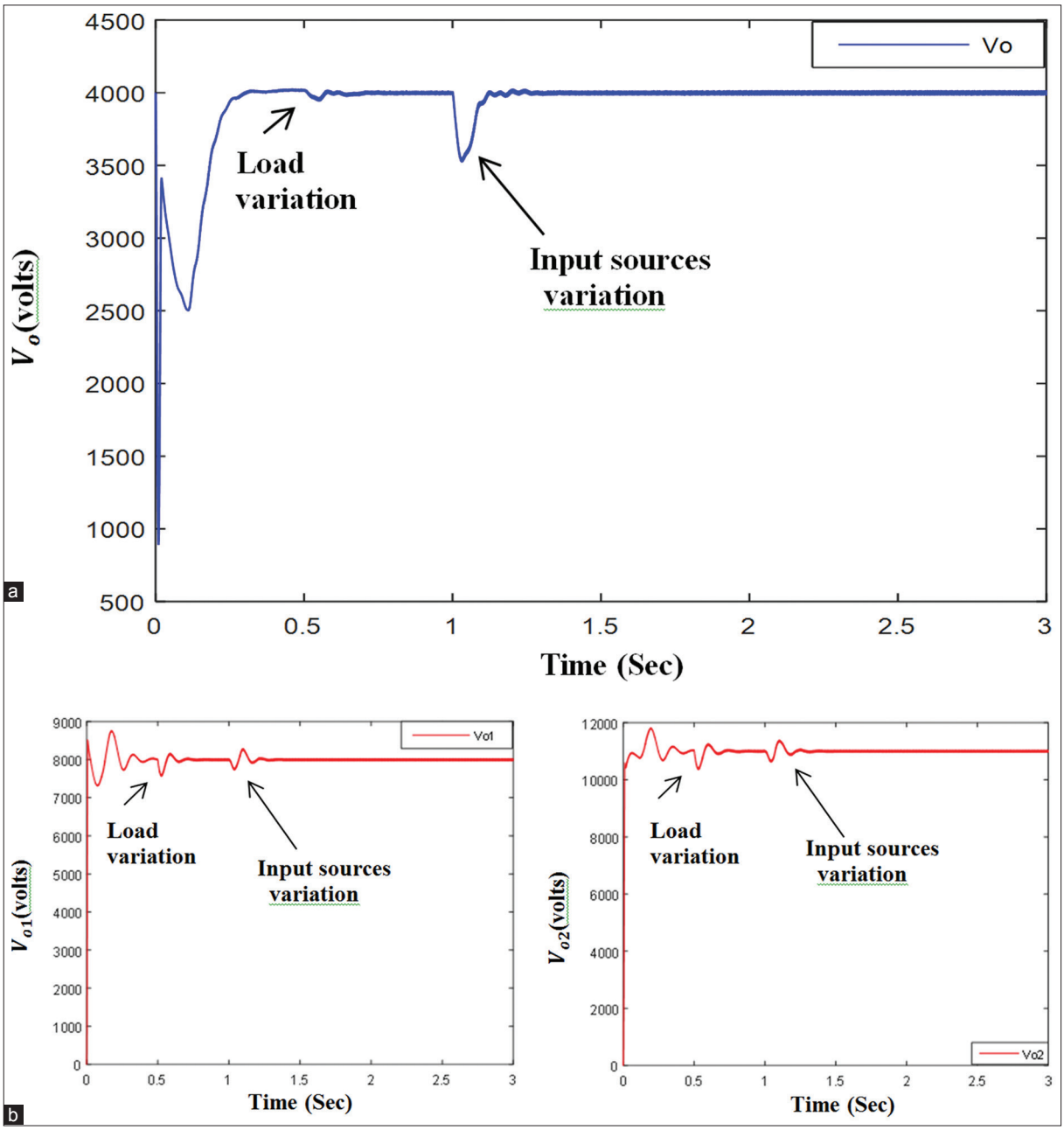


Figure 6. *Depicts the proposed converter output DC voltage results V_o = 4kV, V_{o1} = 8kV, V_{o2} = 11kV. (a) The bus DC voltage Vo with load variation at t=0.5 s and with input sources variation at t=1 s, (b) the output DC voltage V_{o1} and V_{o2} with load variation at t=0.5 s and with input sources variation at t=1 s*

Table 1. *Effects of the PID controller action on the time response curve specifications*

The time response curve specifications	Without the PID controller action	With the PID controller action
P.O	$P.O_{vo1}$ = 83.9% overshooting $P.O_{vo2}$ = 154.7% overshooting	$P.O_{vo1}$ = 9.3% overshooting $P.O_{vo2}$ = 7.2% overshooting
Rise time (s)	$t_{r\text{-}vo1}$ = 0.007 $t_{r\text{-}vo2}$ = 0.013	$t_{r\text{-}vo1}$ = 0.004 $t_{r\text{-}vo2}$ = 0.007
Settling time (s)	$t_{s\text{-}vo1}$ = 0.43 $t_{s\text{-}vo2}$ = 0.5	$t_{s\text{-}vo1}$ = 0.43 $t_{s\text{-}vo2}$ = 0.46
Steady-state error (%)	$S.S.e_{vo1}$ = 3.75 $S.S.e_{vo2}$ = 6.36	$S.S.e_{vo1}$ = 0 $S.S.e_{vo2}$ = 0
Peak-to-peak ripple voltage (volts)	$V_{o1(ripple)(p\text{-}p)}$ = 100 $V_{o2(ripple)(p\text{-}p)}$ = 160	$V_{o1(ripple)(p\text{-}p)}$ = 40 $V_{o2(ripple)(p\text{-}p)}$ = 40

P.O.: Percentage overshoot

The PID controller action has improved the output curve response as the percentage overshoot for each output has been reduced; also, the rise time has been decreased by almost 50% of its original value without using PID controller. The steady-state error has been eliminated due to the integration component of the PID controller.

Table 1 summarizes the effects of the PID controller action on the response curve. A comparison has been made between the time response specification curve with and without the PID controller action.

Hence, the designed controller has demonstrated that it has a good performance under input and load variations, as well as being adaptable.

4. CONCLUSION

In this study, a new MIMO DC-DC boost converter with the advantages of simple configuration, fewer components, and high conversion ratio for medium to high voltage applications is proposed. The mathematical representations of the proposed MIMO converter for ideal and non-ideal converter have been presented. The operation principles and the switching states with the dynamic modeling of the proposed converter have been provided. To verify the performance of the designed converter, MATLAB/SIMULINK simulations have been performed.

The results have proven the effectiveness of multi input sources integration; in terms of flexibility and reliability. Also demonstrated in the robustness of the designed controller through the simulation; where the controller automatically adapts the duty ratios of the power switches to achieve the predefined output voltages as the demand or the supply changes.The performance of designed controller provides fixed output voltages with ripple factor in order of 0.2% and with 100 mA peak ripple output currents. In addition, no overshoot in DC bus voltage response curve has been obtained also9.3%, 7.2% overshoot peak for V_{o1} and V_{o2} respectively. In addition, no overshoot in DC bus voltage response curve has been obtained also 9.3% and 7.2% overshoot peak for V_{o1} and V_{o2}, respectively.

To conclude, the controlled converter achieves a constant 8 kV, 11 kV for the two outputs from three DC input sources at an operating frequency of 1 kHz. The results prove the flexibility and reliability of the proposed converter and the simplicity of designing robust PID controllers to achieve a constant DC output voltage in different scenarios under inputs and load variations.

5. REFERENCES

[1] M.Biswal (2011), 'Control techniques for DC-DC buck converter with improved performance' National Institute of technology Rourkela, India.

[2] N. Mohan, T. M. Undeland and W. P. Robbins (1995), *Power Electronics Converters, Applications and Design,* Wiley, New York.

[3] M. K. Kazimierczuk (1988), Design-oriented analysis of boost zero-voltage- switching resonant DC/DC converter, *IEEE Trans. Power Electron*., **3**(2), 126-136.

[4] C. Buccella, C. Cecati and H. Latafat (2012), Digital control of power converters—A survey, *IEEE Trans. Industr. Inform.*, **8**(3), 437-447.

[5] J.Li (2009), 'Current-mode control: modelling and its digital application', Virginia polytechnic Institute and state university, Virginia, USA.

[6] L. Guo, J. Y. Hung, S. Member and R. M. Nelms (2009), Evaluation of DSP-based PID and fuzzy controllers for DC–DC converters, *IEEE Trans. Industr. Electron.*, **56**(6), 2237-2248.

[7] J. L. Calvo-Rolle and E. Corchado (2014), A bioinspired knowledge system for improving combined cycle plant control tuning, *Neurocomputing*, **126**, 95-105.

[8] M. Alzgool, G. Alzghoul, H. Nouri and C. Toomer (2016), A Novel Multi-Inputs-Single-Output DC Transformer Topology. *51st International Power Engineering Conference, ISEC Coimbra Portugal.*

Design, Control and Modelling of a Novel Multi-Input Multi-Output Boost Converter Hub

M Alzgool[1], H Nouri[1]

[1]Power Systems, Electronics and Control Research Laboratory, UWE Bristol, UK

***ABSTRACT*- This paper reports on the design, control and modelling of a novel Multi-Input Multi-Output Boost Converter topology. The converter hub can integrate renewable energy sources such as wind turbines, photovoltaic arrays, fuel cells, etc. for provision of different output voltage levels. The advantage of energy sources integration is that the required output voltage levels could be made up from a range of sources. The designed converter has the advantages of a simple configuration, fewer components, high conversion ratio and high efficiency.**
The regulated output voltage levels are achieved via classical PID controllers which utilise the concept of closed-loop voltage mode control. Design of the converter control system requires comprehensive knowledge of the converter structure, its operation principle and the small-signal model for continues conduction operation mode. The validity of the converter's control performance is demonstrated through software simulation.

Index Terms: DC-DC Converter, IGBTs, Multi-Input Multi-Output(MIMO), Renewable energy, small signal modelling, state space averaging.

I. INTRODUCTION

Recently, the number of applications which require more than one power source or more than one kind of energy source is increasing. Generating Multi-Input converters, having the capability of diversifying different energy sources, will provide improved reliability and the system flexibility.
Many control methods are used for controlling DC-DC converters where the simple and low cost controller structure is always in demand for most industrial and high performance applications [1]. Most used technique to control switching power supplies is Pulse Width Modulation [2].

When boost converter is employed in open loop mode, it exhibits poor voltage regulation and unsatisfactory dynamic response, and hence, this converter is provided with closed loop control for output voltage regulation. Hence, various close loop techniques had been proposed such as PID controller, Fuzzy logic and other techniques, as well as many other researchers came out with new designs to be controlled with appropriate control technique such as [3] using soft switching technique, and [4] presented high frequency power switches design and robust controller.

In controlling the DC-DC converters a voltage mode control or current mode control could be applied simply by closing a feedback loop between the required output voltages and switching device's duty ratio signal [2]. Due to nonlinearity of current mode control dynamics the difficulties of obtaining the small signal model is achieved, furthermore in current mode control an additional inner feedback loop is needed to control the inductor current and then regulate the output voltage indirectly [5], thus the current mode control is more complex to implement than voltage mode control.
Within close loop system, PID control is considered as a traditional linear control method commonly used in many applications [6]. The PID controller is a popular control feedback used in industrial area due to its flexibility and easy implementation in real applications, furthermore, if the system is complex, the PID can be designed to track an error and assume the system as a black box. A PID controller calculates an error value as the difference between the measured value and the desired reference value [7]. So the PID controller has to adjust three parameters k_p, k_i, k_d of the system which would affect the transient response, rise time, settling time and steady state error, over shoot and stability. Thus, it is not necessary for the system to get the three actions P, I and D it may use one or two actions to improve the system dynamic response.

In this paper a voltage mode control using a PID controller is presented to obtain the closed loop three Input Double Output DC-DC boost converter topology structure as shown in figure 1, where different input sources connected in such a way to integrate the available input sources to provide a high conversion ratio [8].
This paper organised as follow: section II presents the proposed Multi-Input Multi-Output (MIMO) DC-DC boost converter topology and its operation principle. The dynamic modelling of the DC-DC boost converter for three input source Double output is presented in section III including the MATLAB simulation results. Finally, the conclusion of this study is summarised in section IV.

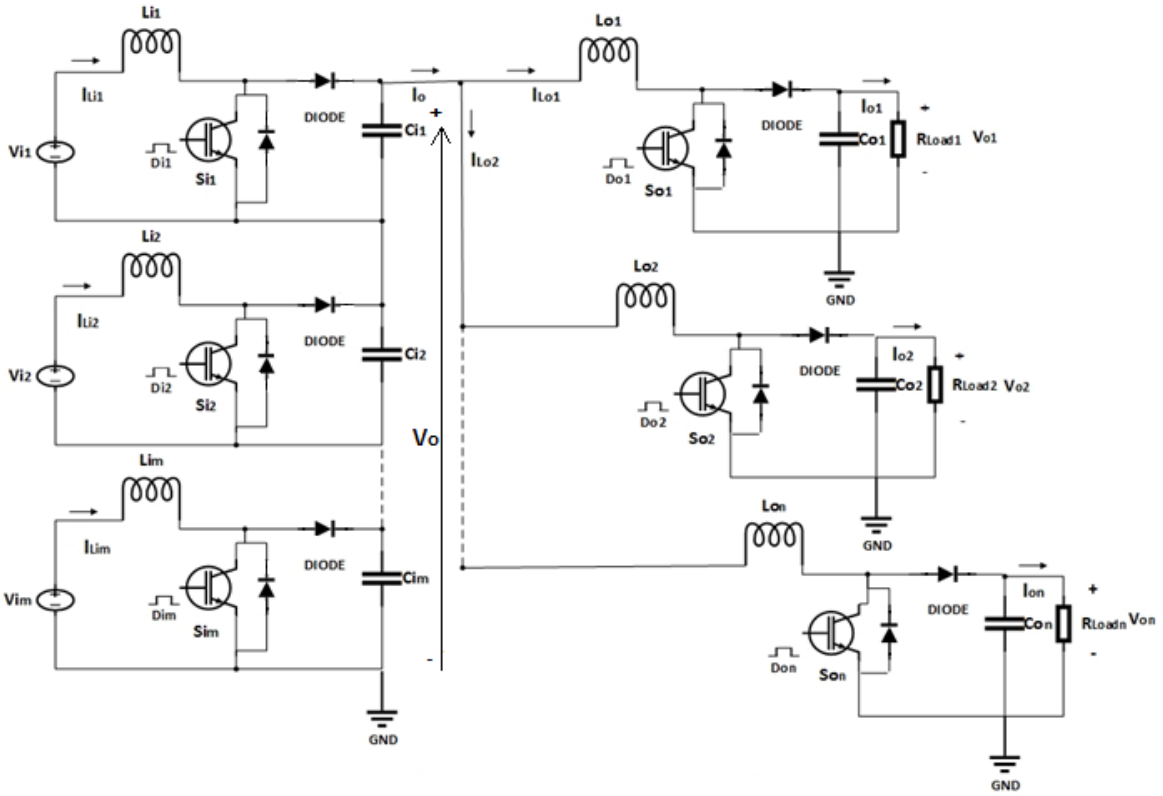


Figure.1. Proposed Multi-Input Multi-Output DC-DC boost converter topology

II. CONVERTER STRUCTURE AND OPERATION PRINCIPLES

A new efficient MIMO DC-DC Boost converter is proposed with the specifications of high conversion ratio and lower number of components with comparison to the available MIMO Boost converter topologies.
In this design the stepping up voltage occurs in two stages; where the output voltage of the first stage (V_o) acts like the input DC voltage to the next stage, so that means higher conversion ratio, which is important in high DC voltage applications.

The mathematical equations of the proposed (MIMO) Boost converter have been derived assuming that the system is lossless (ideal components):

$$V_{o1} = \left[\frac{V_1}{1-D_1} + \frac{V_2}{1-D_2} + \frac{V_3}{1-D_3} + \cdots + \frac{V_m}{1-D_m}\right]\left[\frac{1}{1-D_{o1}}\right] \quad (1)$$

$$\therefore V_{on} = \left[\sum_{k=1}^{k=m} V_k \frac{1}{1-D_k}\right]\left[\frac{1}{1-D_{on}}\right] \quad (2)$$

V_{on} : The output DC voltage.

V_k: The DC input voltage.

D_k: Duty cycle of the input IGBT switches.

D_{on}: Duty cycle of the output IGBT switches.

In this paper a three input sources V_{i1}, V_{i2}, V_{i3} are responsible for supplying the loads. The converter designed to operate in Continues Conduction Mode as the inductors current will never go to zero. In this mode the five switches are active. For each switch, a specific duty ratio is considered. Here, S_{i1} is active to regulate the first input source V_{i1} current to desired value. At the same time S_{i2}, S_{i3} are active to regulate V_{i2}, V_{i3} respectively, by controlling the input inductor currents I_{Li2} and I_{Li3}. Regulating the DC bus voltage $V_o = V_{ci1} + V_{ci2} + V_{ci3}$ to

a desired value, are duty ratios of the three input switches. Also, the output voltage V_{o1} is controlled by the output power switch S_{o1}, similarly S_{o2} regulates the second output voltage V_{o2}. According to switches' states, there are four different switching states in one switching period as shown in figure 2. For each state the inductor and capacitor equations have been investigated as follows:

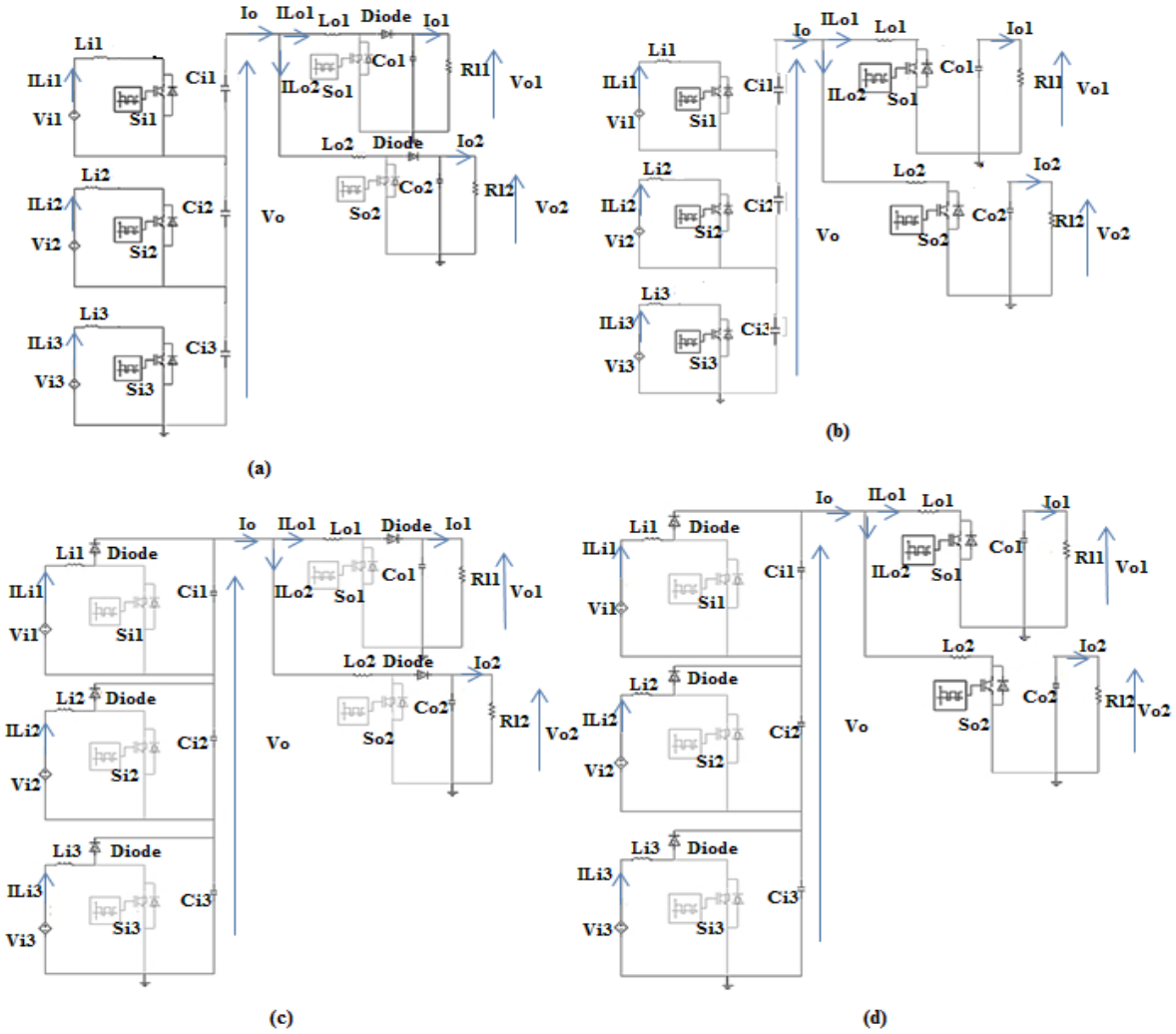


Figure.2. Equivalent circuit of Boost converter switching mode, (a) switching state 1, (b) switching state 2, (c) switching state 3, (d) switching state 4

a) Switching state 1: In this state, the input power switches S_{i1}, S_{i2}, S_{i3} are turned ON, while the output switches S_{o1} and S_{o2} are turned OFF. When the input switches are ON the input stage diodes are reversed biased, so S_{o1} and S_{o2} are OFF. Assuming that the output capacitors are fully charged, thus the power will deliver to the load R_{L1}, R_{L2}. The equivalent circuit of the proposed converter in this state is shown in figure 2(a). In this state, V_{i1}, V_{i2}, V_{i3} charge the inductors L_{i1}, L_{i2}, L_{i3} respectively, so the inductors' current increases and the output capacitors are discharged.

The equations for the inductors and capacitors in this mode are as follows:

$$\begin{cases} L_{i1}\frac{di}{dt} = v_{i1} \\ L_{i2}\frac{di}{dt} = v_{i2} \\ L_{i3}\frac{di}{dt} = v_{i3} \\ C_{i1}\frac{dv_{ci1}}{dt} = -i_o \\ C_{i2}\frac{dv_{ci2}}{dt} = -i_o \\ C_{i3}\frac{dv_{ci3}}{dt} = -i_o \\ L_{o1}\frac{di}{dt} = v_o - v_{co1} \\ L_{o2}\frac{di}{dt} = v_o - v_{co2} \\ C_{o1}\frac{dv_{co1}}{dt} = i_{Lo1} - \frac{v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} = i_{Lo2} - \frac{v_{o2}}{R_{L2}} \end{cases} \quad (3)$$

b) Switching state 2: In this state, the input power switches S_{i1}, S_{i2}, S_{i3} are still ON, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are ON the input stage diodes are reversed biased. Assuming that the output capacitors are fully charged, thus the power will deliver to the load R_{L1}, R_{L2}. The equivalent circuit of the proposed converter in this state is shown in figure 2(b). In this state, V_{i1}, V_{i2}, V_{i3} charge the inductors L_{i1}, L_{i2}, L_{i3} respectively, also the output inductors L_{o1}, L_{o2} are charged from the capacitors C_{i1}, C_{i2}, and C_{i3}. Consequently the inductors' current I_{Lo1}, I_{Lo2} increases. In addition, capacitors C_{o1}, C_{o2} are discharged. The equations for the inductors and capacitors in this mode are as follows:

$$\begin{cases} L_{i1}\frac{di}{dt} = v_{i1} \\ L_{i2}\frac{di}{dt} = v_{i2} \\ L_{i3}\frac{di}{dt} = v_{i3} \\ L_{o1}\frac{di}{dt} = v_o \\ L_{o2}\frac{di}{dt} = v_o \\ C_{i1}\frac{dv_{ci1}}{dt} = -(i_{Lo\,1} + i_{Lo\,2}) \\ C_{i2}\frac{dv_{ci2}}{dt} = -(i_{Lo\,1} + i_{Lo\,2}) \\ C_{i3}\frac{dv_{ci3}}{dt} = -(i_{Lo\,1} + i_{Lo\,2}) \\ C_{o1}\frac{dv_{co1}}{dt} = \frac{-v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} = \frac{-v_{o2}}{R_{L2}} \end{cases} \quad (4)$$

c) Switching state 3: In this state, the input power switches S_{i1}, S_{i2}, S_{i3} are turned OFF, and the output switches S_{o1} and S_{o2} are turned OFF. When the input switches are OFF the input stage diodes are forward biased. In this state the stored energy in the input inductors will deliver to charge the capacitors C_{i1}, C_{i2}, and C_{i3}. In addition, the stored energy in the output inductors will deliver to charge the output capacitors C_{o1}, C_{o2}, as well as to deliver the stored energy to the loads R_{L1}, R_{L2}. The equivalent circuit of the proposed converter in this state is shown in figure 2(c). In this state, the inductors' current I_{Li1}, I_{Li2}, and I_{Li3} decreases and the capacitors C_{i1}, C_{i2}, and C_{i3} charged. The equations for the inductors and capacitors in this mode are as follows:

$$\begin{cases} L_{i1}\frac{di}{dt} = v_{i1} - v_{ci1} \\ L_{i2}\frac{di}{dt} = v_{i2} - v_{ci\,2} \\ L_{i3}\frac{di}{dt} = v_{i3} - v_{ci\,3} \\ L_{o1}\frac{di}{dt} = v_o - v_{co1} \\ L_{o2}\frac{di}{dt} = v_o - v_{co2} \\ C_{i1}\frac{dv_{ci1}}{dt} = i_{Li\,1} - i_o \\ C_{i2}\frac{dv_{ci2}}{dt} = i_{Li\,2} - i_o \\ C_{i3}\frac{dv_{ci3}}{dt} = i_{Li\,3} - i_o \\ C_{o1}\frac{dv_{co1}}{dt} = i_{Lo1} - \frac{v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} = i_{Lo2} - \frac{v_{o2}}{R_{L2}} \end{cases} \quad (5)$$

d) Switching state 4: In this state, the input power switches S_{i1}, S_{i2}, S_{i3} are still OFF, and the output switches S_{o1} and S_{o2} are turned ON. When the input switches are OFF the input stage diodes are forward biased. In this state the stored energy in the input inductors keep charging the capacitors C_{i1}, C_{i2}, and C_{i3}. In addition, the stored energy in the input inductors will deliver to L_{o1} and L_{o2} through the switches S_{o1}, S_{o2} respectively. So the inductors' current I_{Li1}, I_{Li2}, and I_{Li3} keep decreasing, while I_{Lo1}, I_{Lo2} increases. In addition, the capacitors C_{o1}, C_{o2}, will discharge through the loads R_{L1}, R_{L2}. The equivalent circuit of the proposed converter in this state is shown in figure 2(d). The equations for the inductors and capacitors in this mode are as follows:

$$\begin{cases} L_{i1}\frac{di}{dt} = v_{i1} - v_{ci1} \\ L_{i2}\frac{di}{dt} = v_{i2} - v_{ci\,2} \\ L_{i3}\frac{di}{dt} = v_{i3} - v_{ic\,3} \\ L_{o1}\frac{di}{dt} = v_o \\ L_{o2}\frac{di}{dt} = v_o \\ C_{i1}\frac{dv_o}{dt} = i_{Li\,1} - i_o \\ C_{i2}\frac{dv_o}{dt} = i_{Li\,2} - i_o \\ C_{i3}\frac{dv_o}{dt} = i_{Li\,3} - i_o \\ C_{o1}\frac{dv_{co1}}{dt} = \frac{-v_{o1}}{R_{L1}} \\ C_{o2}\frac{dv_{co2}}{dt} = \frac{-v_{o2}}{R_{L2}} \end{cases} \quad (6)$$

III. DYNAMIC MODELING OF THE DC-DC BOOST CONVERTER

As mentioned before the proposed converter is controlled by switches S_{i1}, S_{i2}, S_{i3} and S_{o1}, S_{o2}. Each switch has its own specific duty cycle. By proper regulation of switches' duty cycles, outputs voltage V_{o1} and V_{o2} are adjustable. To design the closed loop controller for the converter, the dynamic model must be obtained. As stated before in section II in order to control the output voltages; regulating the bus DC voltage V_o is also needed. In addition, as each input has its own power switch and different parameters values, thus different controllers need to be designed.

Small signal model is the basis for optimised controller design. Especially, for MIMO converters, an effective model will be helpful to realise closed-loop control, and to optimise the converter dynamics [1]. Unlike the conventional Single Input Single Output (SISO) converters, the MIMO converter is a high order system, and the symbolic derivation of the transfer function of each plant is extensive; therefore, it is difficult to obtain values of poles and zeros for analysis.

The dynamics of the plant can be described in a matrix form; then computer software is used to plot the Bode graph of different transfer functions. Based on small signal modelling method [2], the state variables (x) and duty ratios (d), input voltages (v) contains two components, dc values (X, D, V) and disturbance values $(\hat{x}, \hat{d}, \hat{v})$. It is assumed that the perturbations are small and do not vary significantly during one switching period. So the proposed converter equations are as follows:

$$\begin{cases} i_{Li}(t) = I_{Li} + \hat{\imath}_{Li}(t) \\ i_{Lo}(t) = I_{Lo} + \hat{\imath}_{Lo}(t) \\ v_{o1}(t) = V_{O1} + \hat{v}_{o1}(t) \\ v_{o2}(t) = V_{O2} + \hat{v}_{o2}(t) \\ d_{i1}(t) = D_{i1} + \hat{d}_{i1}(t) \\ d_{i2}(t) = D_{i2} + \hat{d}_{i2}(t) \\ d_{i3}(t) = D_{i3} + \hat{d}_{i3}(t) \\ d_{o1}(t) = D_{o1} + \hat{d}_{o1}(t) \\ d_{o2}(t) = D_{o2} + \hat{d}_{o2}(t) \end{cases} \quad (7)$$

Where $i_{Li}(t)$, $i_{Lo}(t)$ the input and output inductors' current and where the output capacitors' voltage $v_{o1}(t), v_{o2}(t)$ are state variables. Substitutes (7) into (3)-(6), then the averaging model is applied and multiplied by its corresponding duty cycle value. So the system can be represented in a matrix form using a state space averaging model. The state space model takes the following form:

$$\begin{cases} \frac{dX}{dt} = AX + BU \\ Y = CX + DU \end{cases} \quad (8)$$

Where X is a matrix containing the state variables, U is a matrix containing the control inputs $\hat{d}_{i1}(t), \hat{d}_{i2}(t), \hat{d}_{i3}(t), \hat{d}_{o1}(t), \hat{d}_{o2}(t)$ and Y is a matrix containing the system outputs $\hat{v}_o(t), \hat{v}_{o1}(t), \hat{v}_{o2}(t)$.

Matrixes X, Y, U takes following form:

$$X = \begin{bmatrix} \hat{\imath}_{Li1}(t) \\ \hat{v}_{ci1}(t) \\ \hat{\imath}_{Li2}(t) \\ \hat{v}_{ci2}(t) \\ \hat{\imath}_{Li3}(t) \\ \hat{v}_{ci3}(t) \\ \hat{\imath}_{Lo1}(t) \\ \hat{v}_{co1}(t) \\ \hat{\imath}_{Lo2}(t) \\ \hat{v}_{co2}(t) \end{bmatrix}, Y = \begin{bmatrix} \hat{v}_{ci1}(t) \\ \hat{v}_{ci2}(t) \\ \hat{v}_{ci3}(t) \\ \hat{v}_{o1}(t) \\ \hat{v}_{o2}(t) \end{bmatrix}, U = \begin{bmatrix} \hat{d}_{i1}(t) \\ \hat{d}_{i2}(t) \\ \hat{d}_{i3}(t) \\ \hat{d}_{o1}(t) \\ \hat{d}_{o2}(t) \end{bmatrix}$$

The transfer function matrix of the converter is obtained from the small signal model from matrices A, B, C and D as follows:

$$G = C(SI - A)^{-1}B + D \quad (9)$$

The rank of transfer function matrix depends on the control variables; so according to the number of control variables as mentioned before, rank of transfer function matrix G is 5×5

Where

$$y = Gu \quad (10)$$

$$\begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} & g_{15} \\ g_{21} & g_{22} & g_{23} & g_{24} & g_{25} \\ g_{31} & g_{32} & g_{33} & g_{34} & g_{35} \\ g_{41} & g_{42} & g_{43} & g_{44} & g_{45} \\ g_{51} & g_{52} & g_{53} & g_{54} & g_{55} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

Using MATLAB software the transfer functions of the controller can be written as follows:

$$g_{11} = \frac{\hat{v}_{ci1}}{\hat{d}_{i1}} = \frac{V_{i1}}{\left((1-D_{i1})(1+\frac{Li1Ci1}{(1-Di1)^2})S^2\right)} \quad (11)$$

$$g_{22} = \frac{\hat{v}_{ci2}}{\hat{d}_{i2}} = \frac{V_{i2}}{\left((1-D_{i2})(1+\frac{Li2Ci2}{(1-Di2)^2})S^2\right)} \quad (12)$$

$$g_{33} = \frac{\hat{v}_{ci3}}{\hat{d}_{i3}} = \frac{V_{i3}}{\left((1-D_{i3})(1+\frac{Li3Ci3}{(1-Di3)^2})S^2\right)} \quad (13)$$

$$g_{44} = \frac{\hat{v}_{o1}}{\hat{d}_{o1}} = \frac{V_O(1-\frac{L_{o1}}{(1-D_{o1})^2 R_{L1}}S)}{\left((1-D_{o1})(1+\frac{(1-D_{o1})^2 R_{L1}\sqrt{\frac{C_{o1}}{L_{o1}}}}{\sqrt{L_{o1}C_{o1}}})S+\frac{L_{o1}C_{o1}}{(1-D_{o1})^2}S^2\right)} \quad (14)$$

$$g_{55} = \frac{\hat{v}_{o2}}{\hat{d}_{o2}} = \frac{V_o\left(1-\frac{L_{o2}}{(1-D_{o2})^2 R_{L2}}S\right)}{\left((1-D_{o2})\left(1+\frac{(1-D_{o2})^2 R_{L2}\sqrt{\frac{C_{o2}}{L_{o2}}}}{\sqrt{L_{o2}C_{o2}}}\right)S+\frac{L_{o2}C_{o2}}{(1-D_{o2})^2}S^2\right)} \quad (15)$$

In this paper the simulation results for three different input DC sources chosen within these ranges ($V_{i1} = (200-500)V$, $V_{i2} = (350-875)\,V$ *and* $V_{i3} = (250-625)\,V$), as an example of a different wind turbines DC voltage levels. Two output DC voltages are obtained using PID controller. The values of the converter parameters the inductors L and the capacitors C have been sized using a designing formulas [8], in order to achieve a constant DC output voltage where $V_o = 4\,kV, V_{o1} = 8\,kV$ *and* $V_{o2} = 11\,kV$. So by controlling the bus DC voltage V_o through the PID controllers on the first stage of the designed converter to adapt itself as these inputs changes, thus the next stage will provide controlling the output DC voltages as the load changes. Figure 3 depicts the simulation results using MATLAB software of three input two output DC-DC boost converter including the load and input sources variations to test the performance of the closed loop control.

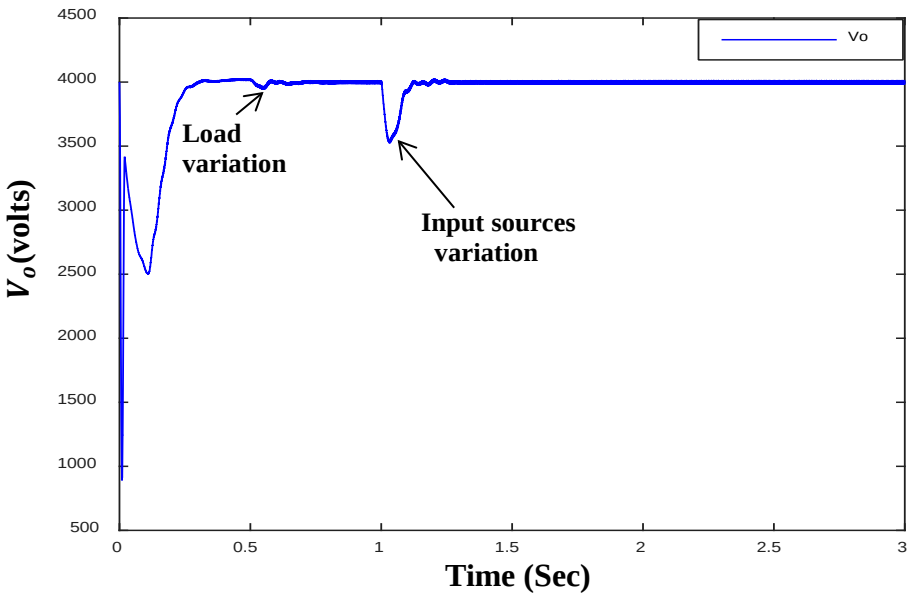


Figure (3.a) The bus DC voltage V_o with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\,\Omega$ and the input sources varied at t=1s as the input values reduced 20% of the original values.

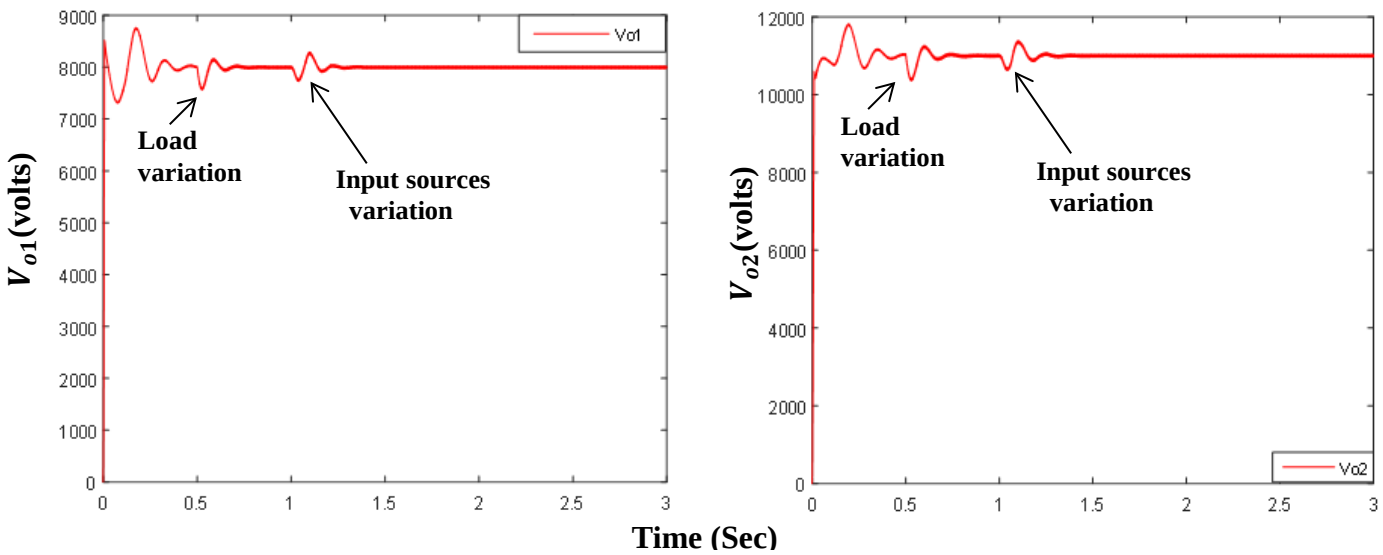


Figure (3.b) The output DC voltage V_{o1} ,V_{o2} with Load variation at t=0.5s where$R_L$changed from 1kΩ to $R_L = 500\,\Omega$ and the input sources varied at t=1s as the input values reduced 20% of the original values.

Figure 3 depicts the proposed converter output DC voltage results $V_o = 4\,kV, V_{o1} = 8\,kV, V_{o2} = 11\,kV$

According to the results obtained from the simulation of a three input two output DC-DC converter model associated with PID controllers these results demonstrate the flexibility and robustness of the designed controller. The DC voltage V_o remains fixed as the input sources reduced by 20% and when the load changes with no overshoot and with small peak to peak ripple voltage ($V_{o(ripple)(p-p)} = 20$) volts.

Similarly, the performance of the designed controller with the output voltages V_{o1}, V_{o2} has been tested as shown in figure 3.b and the controller demonstrates its flexibility and robustness in terms of the ability of the controller to remain the output voltages V_{o1}, V_{o2} fixed whatever the loads or the inputs changes with a good performance with 9.3% overshoot peak for V_{o1} and 7.2% for the second output V_{o2} , as well as small peak current and voltage ripple where

$$V_{o1_{(ripple)(p-p)}} = V_{o2_{(ripple)(p-p)}} = 40 \text{ V}$$

And

$$I_{o1_{(ripple)(p-p)}} = I_{o2_{(ripple)(p-p)}} = 200 \text{ mA}.$$

Hence, the designed controller has demonstrated that it has a good performance under input and load variations, as well as being adaptable.

IV. CONCLUSION

In this study, a new Multi-Input Multi-Output DC-DC Boost converter with the advantages of simple configuration, fewer components and high conversion ratio for medium to high voltage applications is proposed. The operation principles and the switching states with the dynamic modelling of the proposed converter have been provided. To verify the performance of the converter MATLAB simulations have been performed.

The presented Boost converter achieves a constant 8 kV, 11 kV for the two outputs from three DC input sources at an operating frequency of 1 kHz. As a whole, the results prove the effective integrated operation of input sources which will provide a reliable and flexible system, as well as the simplicity of designing the controller to achieve a constant DC output voltage in different scenarios when the inputs or the load changes.

REFERENCES

[1] Biswal,M., 2011[Online]. Available at: http://ethesis.nitrkl.ac.in/2976/1/Thesis.pdf.

[2] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design. New York: Wiley, 1995.

[3] Kazimierczuk M. K. 1988. Design-Oriented Analysis of Boost Zero-Voltage- Switching Resonant DC / DC Converter. IEEE Transactions on Power Electronics.Vol. 3, No. 2, pp. 126–136.

[4] Buccella C., Cecati C. and Latafat H. 2012. Digital Control of Power Converters — A Survey. IEEE Transactions on Industrial Informatics, Vol. 8, No. 3, pp. 437–447.

[5]https://vtechworks.lib.vt.edu/bitstream/handle/10919/27019/Disseration_JianLi_revision_new.pdf?sequence=1

[6] Guo L., Hung J. Y., Member S. and Nelms R. M. 2009. Evaluation of DSP-Based PID and Fuzzy Controllers for DC – DC Converters. IEEE Transactions on Industrial Electronics. Vol. 56, No. 6, pp. 2237–2248.

[7] Calvo-Rolle J. L. and Corchado E. 2014. A Bioinspired knowledge system for improving combined cycle plant control tuning. Neurocomputing, Vol. 126, pp. 95–105.

[8] Alzgool M, Alzghoul G, Nouri H, Toomer C.2016. A Novel Multi-Inputs-Single-Output DC Transformer Topology. 51st International Power Engineering Conference, ISEC Coimbra Portugal; 09/2016.

A Novel Multi-Inputs-Single-Output DC Transformer Topology

M Alzgool[1]

[1]Power Systems, Electronics and Control Research Laboratory, UWE Bristol, UK

H Nouri[1] and C Toomer[1]

[1]Power Systems, Electronics and Control Research Laboratory, UWE Bristol, UK

G Alzghoul[2]

[2]Jordanian Armed Forces, Jordan

ABSTRACT- **In this paper a novel Multi- Input-Single-Output (MISO) Boost Converter topology for renewable energy systems is proposed and presented. This pro- posed topology will be used to obtain different output voltage levels from several power sources, such as wind turbines, photovoltaic arrays, fuel cells, etc. Multi- Input-Single-output converters provide flexibility in terms of the choice and the availability of power source, as well as enhancement in system reliability. The comprehensive operating principle, theoretical analysis and results are discussed in this paper.**

The designed converter has the advantages of simple configuration, fewer components, high conversion ratio and high efficiency. Inputs and output are related mathematically in terms of L, C and the duty cycle of the IGBTs power switches. Also discussed is the derivation of the employed inductor L and the capacitor C in terms of size for a particular application.

The derived input and output expressions (for ideal and non-ideal converters) are solved numerically and the results are validated through PSCAD simulation.

Index Terms: DC-DC Converter, HVDC, IGBTs, Multi Input, and Renewable energy.

I. INTRODUCTION

the demands of a growing worldwide population on the electricity supply, alongside concerns regarding fossil-fuels, greenhouse gases and climate change have led power engineers to seek alternative energy sources [1]-[2]. Hence, renewable energy has received much attention in recent decades [3].

The UK government has set out a target to develop 25 GW offshore wind farms by 2020 and 59 GW by 2030 in order to meet the EU renewable energy target [1]. To integrate such a large amount of remote offshore energy generation into the existing onshore net- works creates a number of technical, economical and environmental challenges for the developers and system operators [4]-[6].

In the future, proposed wind farms at distances of over 60 km from the shore will be connected to the mainland grid Only through DC links [1]. Therefore, HVDC transmission is considered an effective way of connecting offshore wind farms to the main grid. Many large HVDC links experience limitations on power levels since the sending/ receiving end of the DC networks have difficulties in accommodating the number of injections/distributions of high powers at a single point. This HVDC limitation is driving the demand for Multi-Input (MI) DC-DC converters (DC Transformers) or DC Sub- stations by highlighting the significant incentive of a technology that can provide additional access points see Fig. 1.

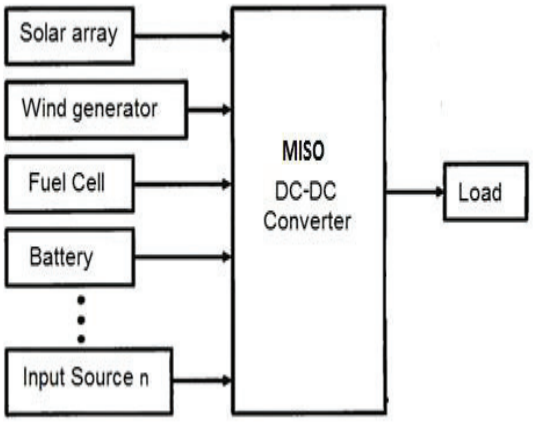


Fig. 1. Multi Input Single Output DC-DC Converter

DC–DC converters have been extensively utilised at low power levels and a number of topologies exist. However, most of these technologies are not suitable for scaling up to megawatt power levels. Conventional, unidirectional boost converters [7] cannot achieve gains larger than 2–4 because of difficulties with the output diode. There have been at-tempts to develop DC-DC converters with internal ac transformers [7]–[8] at higher power levels; however, some serious inherent limitations, in terms of stepping ratios and power levels have been demonstrated [9].

In recent research Jovcic [10] noted that the multi-terminal DC substation is considerably more complex than two-terminal units and that there is need for more research on design optimisation.

Multiple-input and single output DC-DC converters (also

known as multi-terminal DC substations) have been shown as useful for combining several energy sources of different power capacity and/or voltage level, to obtain a well-regulated output voltage [11]-[14]. (Caricchi, Crescimbini et al. 1993) analytically studied the operation modes of a two input – Single Output DC-DC step-up converter for small-size wind-photovoltaic generation in terms of voltage ripples for each operation mode. The converter topology consists of two step-up DC-DC choppers connected in series and tested via computer simulation.

The paper presented by Liu et al (Liu and Li 2005) uses the concept of the zero voltage switching (ZVS) Multi-Input bidirectional DC-DC converter with a multi-winding transformer as a link between the input and output. When in reversed mode this converter can work with only one input. The application of two input DC-DC boost converter topology that uses one less switch for hybrid vehicles is discussed by Marchesonit et al (Marchesoni and Vacca 2007). Authors also analyse and describe mathematically the operation modes of the converter. Khaligh (Khaligh, Cao et al. 2009) presented a bi- directional multi-input/one output DC-DC transformer/converter. The converter has only one inductor connected to all the inputs. It can operate in boost, buck or buck-boost mode. In boost mode it can have only one input connected.

Most recently Preti et al [mmm] have de- signed a high gain DC-DC converter with a coupling inductor, designed to boost low voltages to voltages into a high range of 30 to 50 times Input voltage with the help of a PI controller. To achieve high voltage output, gain the Converter output terminal and boost output terminal are connected in series with the isolated inductor with less voltage stress on the controlled power switch and power diodes.

K. Nithya et al have simulated a proposed multi-input DC-DC boost converter which draws power from several input sources. This Multi-Input Converter (MIC) can deliver power from all of the input sources to the load, either individually or simultaneously. The MIC reduces the system size and cost by reducing the number of components with stepping up the voltage by no more than 3 times.

Serkan Dusmez (Serkan and Xiong 2016) presented a multi input single output isolated three-level DC-DC converter with a trans- former links the output of the system to the input sources. In this topology a transformer with full-bridge converter have been used; so this will increase the cost as well as the size of the DC-DC converter, thus this bulky de- sign is not feasible for offshore wind farm.

In this study, a new Multi Input Single Out- put (MISO) DC-DC Boost converter for renewable energy systems is proposed, as shown in Fig. 2, where -n- different input sources connected in series in such a way to integrate the available input sources to pro- vide a high conversion ratio and high efficiency with reducing the number of components including the power switches with no need to add an additional coupling inductor.

This paper is organised as follow: section II presents the MISO Boost converter topology with explanation of the operation principles and the mathematical equations of In-puts/Output DC-DC Boost converter in terms of the duty cycle of the Insulated Gate Bipolar Transistor (IGBTs) switches are present- ed. The simulations using PSCAD for high voltage DC of three input sources are presented in section III. Finally, the conclusion of this study is summarised in section IV.

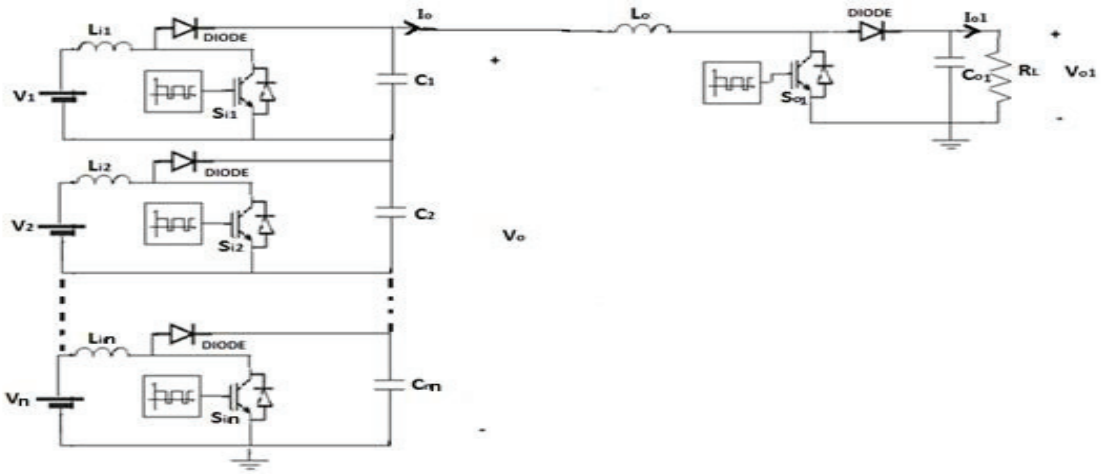


Fig. 2. A Proposed Multi Input Single Output DC-DC Boost Converter

II. PROPOSED MULTI INPUT SINGLE OUTPUT DC-DC BOOST CONVERTER

A Boost converter is a switch mode DC to DC converter in which the output voltage is greater than the input voltage. It is also called as step up converter, so the Boost converters used in applications where the output DC voltage needs to be higher than the input DC voltage. By law of conservation of energy, the input power has to be equal to output power (assuming no losses), Since $V_I<V_O$ in a Boost converter, it follows then that the output current is less than the input current.

Therefore, in Boost converter:

$$V_I<V_O \text{ and } I_I > I_O$$

The proposed multi input DC-DC Boost converter based on the integration of all input sources in such a way to increase the conversion ratio of the Boost converter as the boosting process acquired within two stages as shown in Fig. 2. The input sources are connected in series producing a fixed output DC voltage Vo and then Vo acts as input voltage source of the next stage Boost converter to generate a high DC output voltage Vo1, thus by this design a higher conversion ratio acquired without using extra coupling inductor compared to the available DC-DC Boost converter topologies.

The mathematical equations of the pro-posed Multi Input Single Output DC-DC Boost converter by the Inductor Volt second Balance approach have been derived assuming that the system is lossless (ideal components):

$$V_O = \frac{V_1}{1-D_1} + \frac{V_2}{1-D_2} + \cdots + \frac{V_n}{1-D_n} \quad (1)$$

$$V_{O1} = \left[\frac{V_1}{1-D_1} + \frac{V_2}{1-D_2} + \cdots + \frac{V_n}{1-D_n}\right]\left[\frac{1}{1-D_{O1}}\right] \quad (2)$$

$$\therefore V_{O1} = \left[\sum_{n=1}^{n=N} V_n \frac{1}{1-D_n}\right]\left[\frac{1}{1-D_{O1}}\right] \quad (3)$$

Where

V_{o1}: DC output voltage.
V_n: DC input voltage.
D_n: Duty cycle of the input IGBT switches.
D_{o1}: Duty cycle of the output IGBT switch.

And for non-ideal converter the output DC voltage for single input single output will be:

$$V_{O1} = \frac{1}{(1-D_{O1})}\frac{1}{(1-D_1)}V_1 - \frac{1}{(1-D_{O1})}\frac{1}{(1-D_1)}V_{S1-ON} - \frac{1}{(1-D_{O1})}\frac{1}{(1-D_1)}I_{L1}(R_{S1}+R_{L1}) - V_{D1-ON} - \frac{D_{O1}}{1-D_{O1}}V_{So1-ON} - \frac{D_{O1}}{1-D_{O1}}I_{Lo1}R_{Lo1} - V_{Do1-ON} \quad (4)$$

Where

V_{o1}: the output DC voltage.
$V_{s1\text{-}ON}$: IGBT-ON state voltage drop. (2-3) volts
$V_{D1\text{-}ON}$: Diode forward voltage.
Rs_1 and R_{L1}: the DC resistance of the voltage source and the inductor respectively.

Efficiency is an important DC-DC converter characteristic, it impacts the thermal and electrical losses in the system, as well as the cooling required. A power converter's efficiency is determined by comparing its input power to its output power. More precisely, the efficiency of the converter is calculated by dividing the output power (P_{out}) by its input power (P_{in}).
Here is the formula for determining a SISO DC-DC Boost converter's Efficiency (η).

$$\text{Efficiency } (\eta) = \frac{P_{out}}{P_{in}} \times 100\% \quad (5)$$

For ideal converter:

$$\text{Efficiency } (\eta) = \frac{\left[\frac{V_1}{1-D_1}\frac{1}{1-D_{O1}}\right]^2 / R_L}{V_1 \times I_1} \times 100\% \quad (6)$$

And for non-ideal converter:

$$\text{The output power } P_{out} = [V_{o1}]^2/R_L \quad (7)$$

Where V_{o1} as mentioned before is:

$$V_{O1} = \frac{1}{(1-D_{O1})}\frac{1}{(1-D_1)}V_1 - \frac{1}{(1-D_{O1})}\frac{1}{(1-D_1)}V_{S1-ON} - \frac{D_1}{(1-D_{O1})}\frac{1}{(1-D_1)}I_{L1}(R_{S1}+R_{L1}) - V_{D1-ON} - \frac{D_{O1}}{1-D_{O1}}V_{So1-ON} - \frac{D_{O1}}{1-D_{O1}}I_{Lo1}R_{Lo1} - V_{Do1-ON} \quad (8)$$

In general, the output power of Multi input Single Output DC-DC Boost converter is:

$$P_{out} = \left[\left[\sum_{n=1}^{n=N} V_n \frac{1}{1-D_n}\right]\left[\frac{1}{1-D_{O1}}\right]\right]^2 \Big/ R_L \quad (9)$$

III. DESIGN AND PSCAD SIMULATION OF MULTI INPUT SINGLE OUTPUT DC-DC BOOST CONVERTER

The proposed MISO DC-DC converter can be used in various applications such as high voltage applications (offshore wind farms) or low voltage applications (hybrid electric vehicles).

In this paper an example of two wind generators input sources with single output is designed as follow:
$V_1 = V_2 = 0.33$ kV, $V_O = V_{c1} + V_{c2} = 2$ kV, $V_{o1} = 11$ kV, $I_i = 0.6$ kA, and the switching frequency of 1 kHz. The values of L and C are calculated for these parameters as shown in Fig. 3, also the duty cycle of each IGBT switch $D_1 = D_2 = 67\%$ and $D_{o1} = 81\%$ in addition the inductors and capacitors are sized as follow **$L_{i1} = L_{i2} = 1.9$mH, $C_1 = C_2 = 2.5$mF, $L_o = 91$mH** and **$C_o = 25.1$uF**.

In this case the conversion ratio of the proposed DC-DC Boost converter reaches up to 33.3 times with more than 94% efficiency for non-ideal converter and these factors are needed in HVDC applications.

The simulations using PSCAD software is carried out for the pre mentioned parameters and the results have shown in Fig. 4, where an 11kV output DC voltage is acquired from 0.33kV input DC source

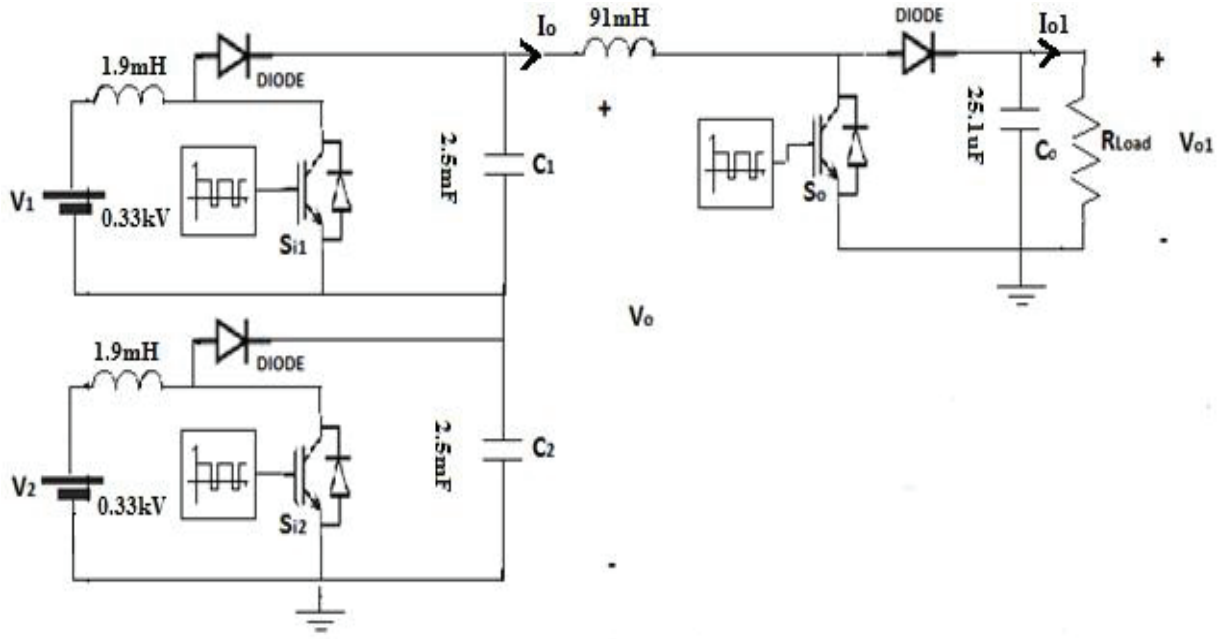


Fig. 3. A Proposed Multiple Inputs Single Output DC-DC Boost Converter

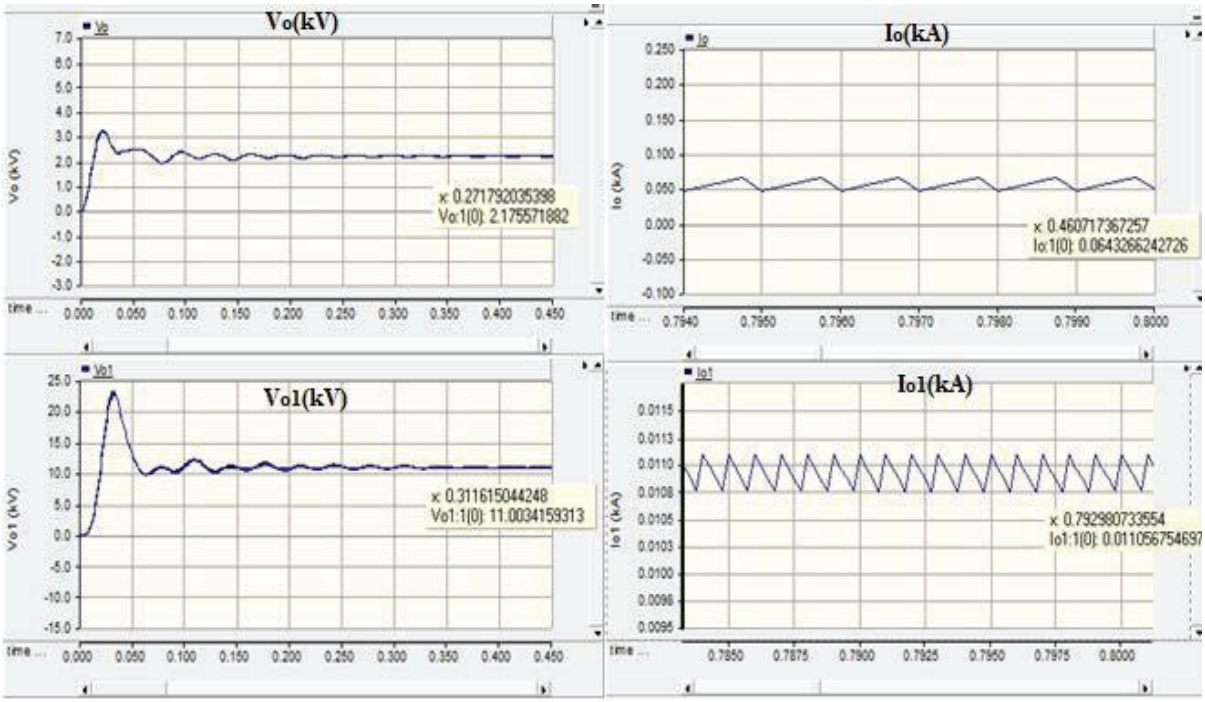


Fig. 4. PSCAD simulation results: $V_1 = V_2 = 0.33$kV, $V_o = 2.1$kV, $V_{o1} = 11$kV, $I_o = 0.064$kA, $I_{o1} = 0.011$kA

IV. CONCLUSION

In this study, a new Multi Input Single Output DC-DC Boost converter with the advantages of simple configuration, fewer components, high conversion ratio and high efficiency for medium to high voltage applications is proposed. The operation principles and the theoretical analysis of the proposed converter have been provided, with proper selection of input and out- put inductors and capacitors. To verify the operation of the converter PSCAD simulations have been performed. The presented Boost converter achieves a constant 11 kV output from 330 V inputs, thus a high step up voltage gain achieved. As a whole, the results prove the effective integrated operation of input sources as the Boost converter achieved efficiency above 94% with high voltage gain (up to 33) at an operating frequency of 1 kHz.

REFERENCES

[1] National Grid Electricity Transmission plc, "Offshore Development Information Statement: Future Scenarios Consultation," February 2011. [Online]. Available: http://www.nationalgrid.com. [Accessed 08 November 2012].

[2] European Wind Energy Association (EWEA), "Oceans of Opportunity: Harnessing Europe's larg- est domestic energy resource," September 2009. [Online]. Available: http://www.ewea.org. [Ac- cessed 08 November 2012].

[3] National Renewable Energy Laboratory (NREL), "Large-scale offshore wind power in the United States," September 2010. [Online]. Availa- ble: http://www.osti.gov/bridge. [Accessed 8 No- vember 2012].

[4] E. Eriksson, P. Halvarsson, D. Wensky, and M. Hausler, "System Approach on Designing an Off- shore Windpower Grid Connection", Proc. of the 4th International Workshop on Large-Scale Integration of Wind Power and Transmission networks for Offshore Wind Farms, Sweden, Oct. 2003.

[5] S. M. Bolik, "Grid Requirements Challenges for Wind Turbines",Proc. of the 4th International Workshop on Large-Scale Integ ration of Wind Power and Transmission networks for Off- shore Wind Farms, Sweden, Oct. 2003.

[6] O. A. Giddani, G. P. Adam, O. Anaya-Lara, G. Burt, and K. L. Lo, "Potential benefits of decou- pling the Scotland-England network using VSC- HVDC," in AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on, 2010, pp. 1-5.

[7] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design. New York: Wiley, 1995.

[8]Q. Zhao and F. C. Lee, "High efficiency, high step up DC-DC converters," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 65–73, Jan. 2003.

[9] K. Hirachi et al., "Circuit configuration of bi- directional DC/DC converter specific for small scale load leveling system," in Proc. Inst. Elect. Eng. Power Conversion Conf., 2002, pp. 603–609.

[10] D. Jovcic, "Developing DC Transmission NetworksUsing DC Transformers", IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 25, NO. 4, OCTOBER 2010, pp 2535-2543.

[11] G. J. Su, F. Z. Peng, and D. J. Adams, "Exper- imental Evaluation of a Soft-Switching DC-DC Converter for Fuel Cell Applications," PET'02, pp. 39-44.

[12] H. Matsuo, Wenzhong Lin; F. Kurokawa, T. Shigemizu, and N. Watanabe, "Characteristics of the Multiple-Input DC-DC Converter," IEEE Transactions on Industrial Electronics, Vol. 51, June 2004, pp. 625-63 1.

[13] B. G. Dobbs, and P. L. Chapman, "A Multiple- Input DC-DC Converter Topology" IEEE Power Electronics Letters, Vol. 1, March 2003, pp. 6-9.

[14] H. Matsuo, K. Kobayashi, Y Sekine, M. Asa- no, and Lin Wenzhong, "Novel Solar Cell Power Supply System using the Multiple-Input DC-DC Converter," IEEE INTELEC, Oct. 1998, pp. 797- 802.

[15] Caricchi, F., et al, "Testing of a New DC/DC Converter Topology for Integrated Wind- Photovoltaic Generating Systems" 5th European Conference on Power Electronics and Applications, 1993, Brighton, U.K.

[16] Liu, D. and H. Li, "A Novel Multiple-Input ZVS Bidirectional DC-DC Converter" 31st Annual Conference of IEEE Industrial Electronics Society, 2005, Raleigh, USA.

[17] Marchesoni, M. and C. Vacca, "New DC–DC Converter for Energy Storage System Interfacing in Fuel Cell Hybrid Electric Vehicles" IEEE Transac- tions on Power Electronics 22(1), 2007, pp 301 - 308.

[18] Khaligh, A., et al, "A Multiple-Input DC–DC Converter Topology" IEEE Transactions on Power Electronics, 24(3), 2009, pp 862 - 868.

[19] Preti, T et al, "Design High Gain DC-DC Boost Converter with Coupling Inductor and Simulation in PSIM" International Journal of Research in Engineering and Technology, Volume: 03 Issue: 04 | Apr-2014, pp 156-163.

[20] Nithya. K and M. Ramasamy, "Modeling of Multi-Input DC-DC Converter for Renewable Energy Sources" International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, Special Issue 1, February 2014, pp 970- 975.

[21]SerkanDusmez and XiongLi,"A New Multi- input Three Level DC-DC Converter" IEEE Trans- actions on Power Electronics, VOL. 31, NO. 2, FEBREUARY 2016.

Appendix C

Laplace Transform Table

$f(t)$	$F(s)$
$f(t)$	$sF(s) - f(0)$
$f''(t)$	$s^2F(s) - sf(0) - f(0)$
$\frac{d^n f(t)}{dt^n}$	$s^nF(s) - \sum_{i=0}^{n-1} s^{n-1-i} f^{(i)}(0)$
$f(t - t_0)\, u(t - t_0)$	$F(s)e^{-st_0}$
$\int_0^t f(\tau)\, d\tau$	$\frac{1}{s} F(s)$
$f(t - \tau)$	$F(s)e^{-s\tau}$
$e^{-at} f(t)$	$F(s + a)$
$f(0) = \lim_{t \to 0} f(t) = \lim_{s \to \infty} s\, F(s)$	
$f(\infty) = \lim_{t \to \infty} f(t) = \lim_{s \to 0} s\, F(s)$	
$-t\, f(t)$	$\frac{d}{ds} F(s)$
$\delta(t)$	1
$\delta_{-1}(t)$ or 1	$\frac{1}{s}$
e^{-at}	$\frac{1}{s + a}$
t	$\frac{1}{s^2}$
$\sin(at)$	$\frac{a}{s^2 + a^2}$
$\cos(at)$	$\frac{s}{s^2 + a^2}$

The Laplace Transformation

$$F(s) = \int_0^\infty f(t) e^{-st} dt$$

$$f(t) = \frac{1}{2\pi i} \int_{\sigma - i\omega}^{\sigma + i\omega} F(s) e^{st} ds$$

Appendix D

Total recorded time: total time required to simulate the model

Total time spent executing all invocations of functions as an absolute value and as a percentage of the total simulation time.

SIMULINK: analysis –performance tools – show profiler report.

Simulink Profile Report: Summary

Report generated 19-Apr-2018 12:56:26

Total recorded time:	61.19 s
Number of Block Methods:	181
Number of Internal Methods:	14
Number of Model Methods:	14
Clock precision:	0.00000003 s
Clock Speed:	3300 MHz

To write this data as evaluation1ProfileData in the base workspace click here

Function List

Name	Time		Calls	Time/call	Self time		Location (must use MATLAB Web Browser to view)
simulate(evaluation1)	61.18750000	100.0%	1	61.18750000000000	0.00000000	0.0%	evaluation1
simulationPhase	60.53125000	98.9%	1	60.53125000000000	5.45312500	8.9%	evaluation1
solverPhase	44.12500000	72.1%	91470	0.00048239860063	0.89062500	1.5%	evaluation1
ode23tb.Integrate	34.18750000	55.9%	91470	0.00037375642287	1.10937500	1.8%	evaluation1
evaluation1.Outputs.Minor	31.62500000	51.7%	467304	0.00006767543184	16.37500000	26.8%	evaluation1
ode23tb.FirstNewtonIteration	14.76562500	24.1%	106276	0.00013893658963	1.31250000	2.1%	evaluation1
evaluation1.Outputs.Major	10.23437500	16.7%	98018	0.00010441322002	4.65625000	7.6%	evaluation1
ode23tb.SecondNewtonIteration	9.71875000	15.9%	104161	0.00009330507580	0.92187500	1.5%	evaluation1
detectZeroCrossings	5.68750000	9.3%	91470	0.00006217885646	0.31250000	0.5%	evaluation1
bracketZeroCrossingInterval	3.78125000	6.2%	10123	0.00037353057394	0.34375000	0.6%	evaluation1

SIMULINK profile report (MATLAB solver time) of the topology of [1]

Simulink Profile Report: Summary

Report generated 19-Apr-2018 12:19:15

Total recorded time:	75.81 s
Number of Block Methods:	204
Number of Internal Methods:	14
Number of Model Methods:	14
Clock precision:	0.00000003 s
Clock Speed:	3300 MHz

To write this data as evaluation2ProfileData in the base workspace click here

Function List

Name	Time		Calls	Time/call	Self time		Location (must use MATLAB Web Browser to view)
simulate(evaluation2)	75.81250000	100.0%	1	75.81250000000000	0.00000000	0.0%	evaluation2
simulationPhase	75.14062500	99.1%	1	75.14062500000000	6.34375000	8.4%	evaluation2
solverPhase	56.42187500	74.4%	93708	0.00060210307551	0.71875000	0.9%	evaluation2
ode23tb.Integrate	42.53125000	56.1%	93708	0.00045387000043	1.93750000	2.6%	evaluation2
evaluation2.Outputs.Minor	41.34375000	54.5%	552083	0.00007488683767	20.65625000	27.2%	evaluation2
ode23tb.FirstNewtonIteration	17.39062500	22.9%	112249	0.00015492899714	1.53125000	2.0%	evaluation2
evaluation2.Outputs.Major	11.57812500	15.3%	103647	0.00011170728530	5.75000000	7.6%	evaluation2
ode23tb.SecondNewtonIteration	11.14062500	14.7%	108384	0.00010278846509	1.01562500	1.3%	evaluation2
detectZeroCrossings	8.95312500	11.8%	93708	0.00009554280318	0.46875000	0.6%	evaluation2
bracketZeroCrossingInterval	6.79687500	9.0%	15077	0.00045081083770	0.48437500	0.6%	evaluation2

SIMULINK profile report (MATLAB solver time) of the topology of [11]

Simulink Profile Report: Summary

Report generated 19-Apr-2018 12:20:41

Total recorded time:	28.42 s
Number of Block Methods:	215
Number of Internal Methods:	12
Number of Model Methods:	13
Clock precision:	0.00000003 s
Clock Speed:	3300 MHz

To write this data as evaluationProfileData in the base workspace click here

Function List

Name	Time		Calls	Time/call	Self time		Location (must use MATLAB Web Browser to view)
simulate(evaluation)	28.42187500	100.0%	1	28.42187500000000	0.00000000	0.0%	evaluation
simulationPhase	27.31250000	96.1%	1	27.31250000000000	2.28125000	8.0%	evaluation
solverPhase	21.06250000	74.1%	28085	0.00074995549226	0.29687500	1.0%	evaluation
ode45.Integrate	17.87500000	62.9%	28085	0.00063646074417	0.89062500	3.1%	evaluation
evaluation.Outputs.Minor	16.79687500	59.1%	187591	0.00008953987665	8.50000000	29.9%	evaluation
evaluation.Outputs.Major	3.73437500	13.1%	28919	0.00012913223140	1.65625000	5.8%	evaluation
evaluation.Derivatives	1.35937500	4.8%	174656	0.00000778315660	0.79687500	2.8%	evaluation
detectZeroCrossings	1.28125000	4.5%	28085	0.00004562043796	0.15625000	0.5%	evaluation
compileAndLinkPhase	1.01562500	3.6%	1	1.01562500000000	1.01562500	3.6%	evaluation
handleZeroCrossings	1.00000000	3.5%	6019	0.00016614055491	0.06250000	0.2%	evaluation
evaluation.ZeroCrossings	0.90625000	3.2%	63099	0.00001436235123	0.59375000	2.1%	evaluation
bracketZeroCrossingInterval	0.73437500	2.6%	6019	0.00012200947001	0.03125000	0.1%	evaluation

SIMULINK profile report (MATLAB solver time) of the proposed topology