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APPLIED PHYSICS REVIEWS

Heterogeneous 2.5D integration on through silicon interposer

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Driven by the need to reduce the power consumption of mobile devices, and servers/data centers, and yet continue to deliver improved performance and experience by the end consumer of digital data, the semiconductor industry is looking for new technologies for manufacturing integrated circuits (ICs). In this quest, power consumed in transferring data over copper interconnects is a sizeable portion that needs to be addressed now and continuing over the next few decades. 2.5D Through-Si-Interposer (TSI) is a strong candidate to deliver improved performance while consuming lower power than in previous generations of servers/data centers and mobile devices. These low-power/high-performance advantages are realized through achievement of high interconnect densities on the TSI (higher than ever seen on Printed Circuit Boards (PCBs) or organic substrates), and enabling heterogeneous integration on the TSI platform where individual ICs are assembled at close proximity (<1 mm separation) compared with several centimeters on a typical PCB. In this paper, we have outlined the benefits of adopting 2.5D TSI technology and also highlighted the current day approaches to implement this technology in Si fabrication facilities, and in assembly/packaging factories. While the systems and devices that power the mobile society benefit from exploiting advantages of 2.5D integration on TSI, there do exist surmountable challenges that need to be addressed for this relatively new technology to be used in high volume production of next generation semiconductor devices. The key areas of focus and challenges include: Technology planning and design-execution that are necessary for harnessing 2.5D TSI for building systems, processing flow for the fabrication of 100 μm thick TSI at acceptable costs, manufacturing flow for assembling multiple ICs on a 100 μm thick TSI in a repeatable, and reliable manner, thermo-mechanical analysis and optimization for addressing warpage issues, and thermal management for addressing heat dissipation. We have outlined design, manufacturing methodologies, and challenges, along with solutions to the challenges associated with taking 2.5D TSI technology to high volume production within the next few years. © 2015 AIP Publishing LLC.
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I. SYSTEMS TRENDS AND 2.5D/3D TECHNOLOGY INTEGRATION BENEFITS

We live in a mobile society where mobile devices allow us to communicate readily with people that are socially and professionally connected to us. Today's mobile society leverages on the performance and reliability of mobile devices (phones and tablets) and the vast internet infrastructure. In these two areas, amazing technical innovations are strongly driven by the large market size and customer base. Continued innovations are needed as the adoption of mobile devices rapidly penetrates developed as well as emerging economies of the world. Innovations are necessary since such adoption will drive the processing and transfer of large volumes of data in the mobile society.

Recent data show that there is a greater than 10 times increment in the mobile data traffic from 2012 to 2017 and

the daily data traffic amounts to be quintillion bytes ("*Big Data*").[1] These data originate from all around the world in the forms of climate information, pictures and videos, banking transactions, and global positioning system (GPS) data, etc. Handling such data traffic is dependent on the use of various Si technologies (e.g., Logic-CMOS, dynamic random access memory (DRAM), BiCMOS, Si Photonics, etc.). A key concern is the performance and power consumption of integrated circuits (ICs) and devices for transferring large amounts of data. In this review paper, we look into the opportunities and trends in the heterogeneous integration of various Si technologies using 2.5D Through-Si-Interposer (TSI) as a next generation Si technology platform to manufacture next generation IC and devices that will support the explosion in the data traffic.

A. Interconnect bottleneck

When one looks closely at data traffic at the system/subsystem level (e.g., mobile phones, tablets, data centers, and line cards), the data traffic most typically occurs between the logic and memory devices and is transmitted across Cu interconnects. With large amounts of data processed or transferred, a key bottleneck is the movement of the data between a logic device and a memory or between 2 or more logic devices. Such data transfer happens over interconnects. Interconnects within computers, mobile devices, and within data-centers are typically using Cu lines on Printed Circuit Boards (PCBs) or Organic Substrates, or on System-on-Chip (SoC) interconnects—for electrical data transfer. A simplest case that can be considered is that of a multi-core processor transferring data to a nearby memory (known as logic-memory interface) over Cu interconnects. Such data transfer occurs all the time in a mobile device or in a data-center or in a switching network. It turns out, the performance of, and the power consumed by the logic-memory interface is a critical bottleneck that needs to be addressed for both mobile devices and data-centers that form a central part of today's internet infrastructure.

1. More-on-Moore SoC scaling

The challenge with improving the efficiency and speed of the logic-to-memory interface is also referred to as the "memory-wall." This is because logic-device (or processor) performance is steadily improving over past decades due to CMOS technology advancement that is guided by Moore's law.[2] The More-on-Moore miniaturization[3] drives the minimum chip feature size (transistor gate length) to shrink about 50% every 18 months, allowing for faster transistors on logic devices (processors). Processor optimization has also led to the use of multi-core (8-core, 32-core, 64-core, and so on) processors to enhance the performance of advanced processors called Central Processing Units (CPU). In a high performance system, this means that each of these individual processor-cores needs to have separate access channel to data in the memory. However, there is a limitation to how fast multiple processors can exchange data with increasingly large amounts of memory. This is a fundamental interconnect related challenge faced by today's PCBs and electronic

packages. Therefore, they cannot support the density of interconnects that is needed to support this data transfer. In addition to interconnect density, the length of the interconnects on PCBs is quite long (order of centimeters), which means that significantly higher power consumption is required when multiple processors send and receive data from memory devices.

CMOS technology miniaturization (Moore's law[2]) can be translated into system level performance improvements by using the System-On-Chip architecture—where both logic and memory are fabricated in the same Si wafer. However, as mentioned above, the advent of multi-core processors that need to have large amounts of adjacent memory (several Gigabytes) places several limitations on the Moore's law-enabled SoC architecture in terms of the sheer size of Si needed (larger Si chip means lower yields). In addition, the high performance Si technology for producing logic processors is highly unsuitable for making low-power memory functions (e.g., DRAM). The separation of the logic and memory functions into discrete packages places the burden on the PCB, and the electronic packages. When the complexity of ICs increases, the number of I/O pins rises exponentially according to the well known Rents rule,[4] thereby giving rise to increased wiring demands[5,6] on the system level. For next generation systems, the PCB and electronic packages face serious challenges from (a) limited interconnect density of electronic packages that connect logic and memory, (b) I/O circuit power consumption related to higher parasitics from longer PCB and package wire lengths, and (c) power disadvantage $(1/2 \ f.C.V^2)$ at higher clock rates are typically used to transfer large amounts of data within systems with I/O count limitations. Package (C4) bump-pitch has scaled at a significantly slower rate in comparison with CMOS technology nodes, and it demonstrates the manifestation of the interconnect challenge.[7]

Therefore, traditional electronic packaging combined with Moore's Law presents a bottleneck for system scaling, i.e., increasing system speed, reducing system power, and shrinking system size.

2. More-than-Moore system scaling

In order to provide a multi-generational solution to address the challenges to system-scaling, one needs an alternative approach that overcomes the limitations on system scaling placed by the memory-wall, limitations of Moore's law/SoC architecture, and the lack of interconnect scaling on PCBs and electronic packages. First, high performance systems need optimized Si technologies to obtain the necessary performance and power requirements of different parts of the system, namely, logic gates, memory cells, RF/Analog blocks, etc. Thus, one needs to think in terms of "disintegrating" the SoC to achieve optimization of given function: (a) Logic-speed and power, (b) memory density/ power/ performance, (c) RF/Analog performance, and (d) optimized interconnect that links these features to make high performance/low-power systems. With the ability to optimize Si technologies based on the functions, one can develop both memory and logic (CPU) ICs with the necessary number of I/O counts that can overcome the memory-wall. To

interconnect the tens to hundreds of thousands of I/Os, between logic ICs and memory ICs, one can use fine pitch copper wiring that can be readily derived from CMOS copper interconnects using Si fabrication. This provides Si substrate to connect several thousands of interconnects between ICs, and deliver power and ground supply to the ICs on the Si substrate. Second, unpackaged individual ICs are attached using micro-solder-joints or micro-bumps to the Si substrate containing fine pitch interconnects (pitch capable of reaching <2 μm line/space compared to 10–20 μm line/space on organic packages and PCBs). Such unpackaged ICs have much reduced package parasitics. The signal, power, and ground connections are provided by Through-Si-Vias (TSVs),[8] enabling electrical connections from the bottom side of the Si substrate to the front side where the ICs are attached. Such a Si substrate is called a TSI.[9–11] This technology referred to as 2.5D integration (or 2.5D ICs) using TSIs offers significant benefits to overcome limitations to system-scaling and is considered a game-changer for current and future systems that are expected to drive mobile-handheld and data-center applications for decades to come. The term 2.5D stems from the fact that using TSI technology for stacking ICs side-by-side on a TSI can be considered a midpoint between

traditional ICs in package representing 2D integration, and chips stacked on top of one another that represents 3D integration. The TSI offers a technology platform to integrate disparate technologies (such as CMOS, memory, sensors, high density copper interconnects, optical interconnects supported by Si photonics, etc.) and thus enable heterogeneous integration. This form of integration is also known as More-than-Moore integration.

Figure 1(a) shows an example of a TSI platform which provides the necessary high density interconnects to address the gap between chip scaling and system wiring in many of the heterogeneous systems. TSI allows designers to connect multiple ICs with high density and significantly shorter (<1 mm), fine pitch (<4 μm) sub micron interconnects (than provided by traditional packaging), and micro-bump (pitch < 40 μm) technology. TSVs provide the access to a package/PCB for power supply or ground and external I/Os.

Figure 1(b) illustrates how the fine pitch (pitch = 40 μm) micro-bumps connect field-programmable gate array (FPGA) slice to the TSV interposer. The C4 bumps (pitch = 200 μm) in turn connect the TSI to the package. Large package balls (pitch = 1000 μm) connect the package to the PCB.

(a)

(b)

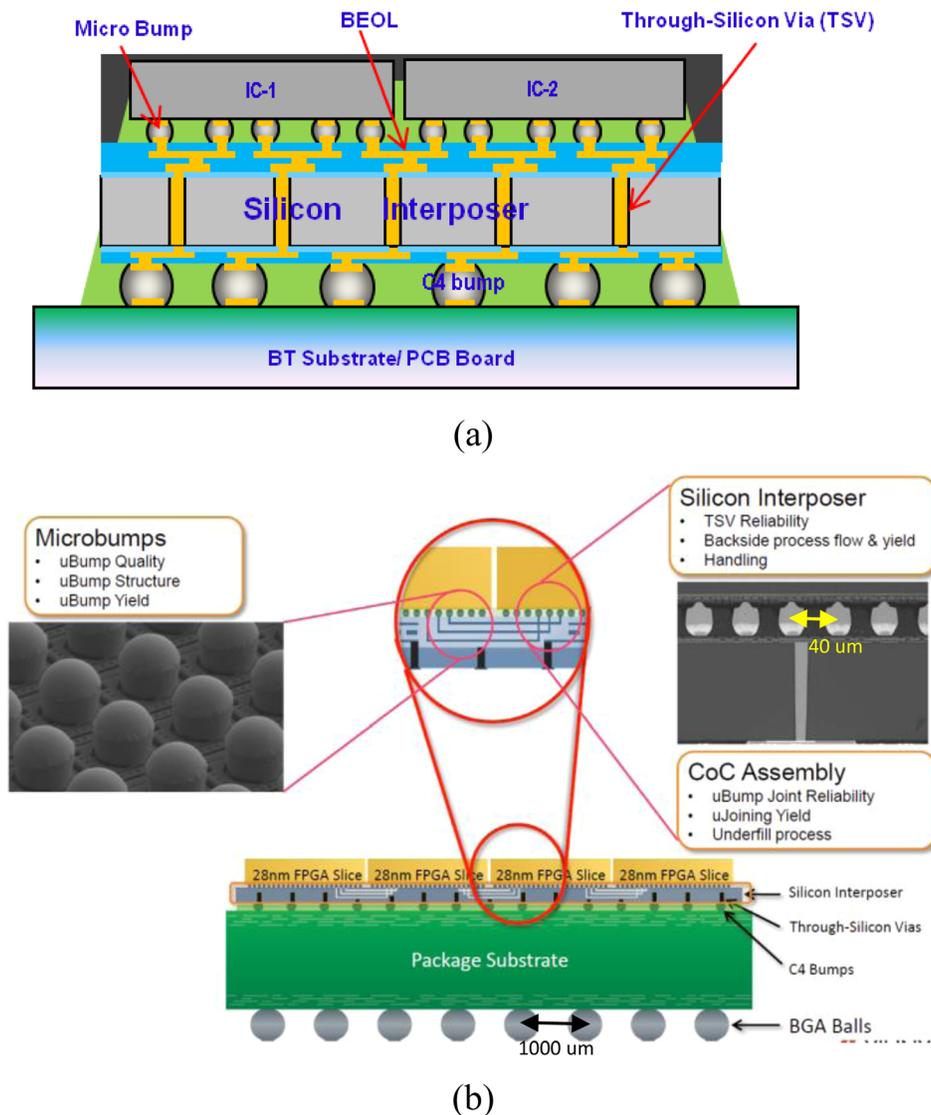FIG. 1. (a) Schematic of IC integration on a TSI platform. (b) Cross-section of the Xilinx 2.5D TSI based Virtex-7HT FPGA.[12] Reproduced with permission from Madden *et al.*, "Advancing high performance heterogeneous integration through die stacking," in Proceedings of European Solid-State Device Research Conference (ESSDERC) (2012). Copyright 2012 Institute of Electrical and Electronics Engineers.
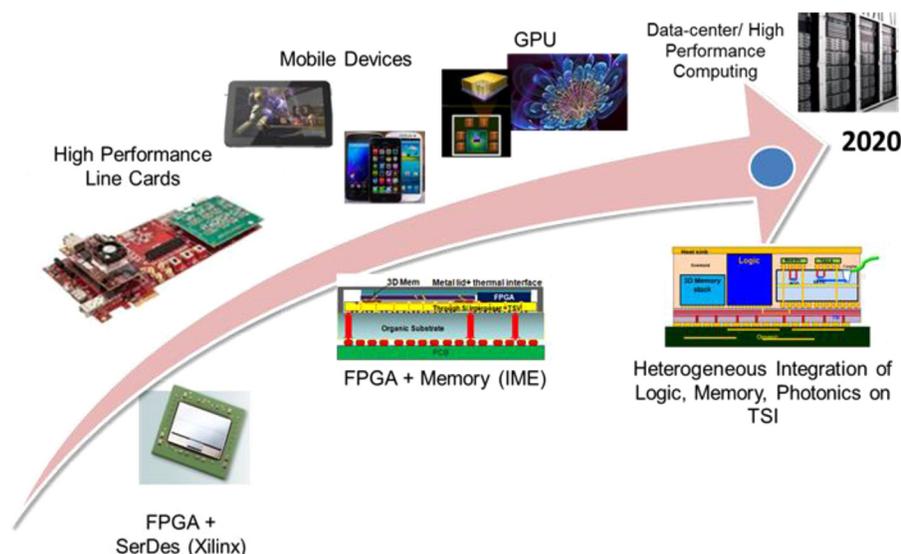
FIG. 2. Si interposer application examples and development roadmap.

Over the past few years, a significant research effort has been invested on 2.5D integration technologies encompassing fabrication, assembly, packaging, and design automation tools and electrical design issues such as signal integrity/power integrity (SI/PI).[13] This review paper attempts to capture the advantages of this technology and reviews major challenges and solutions developed by the industry, IME, and other research institutes.

3. Application examples

Figure 2 shows a proposed roadmap for the application of 2.5D TSI technology for mobile devices and data centers. In 2012, Xilinx[12] demonstrated virtex-7 FPGA with 2.5D TSI technology integrating high density gate arrays with high-speed Serializer-Deserializer (SERDES). The next phase of heterogeneous integration using 2.5D TSI will allow the integration of high-speed Graphic Processor Units (GPU) or Application Processor Engines (APE) with high density 3D stacked memories (High-Band-Width Memory (HBM)[14] and Hybrid Memory Cube (HMC)[15]) for graphic computing, and mobile tablets. As data traffic continues to explode, optical interconnects are needed for transferring large volumes of data between racks in data centers and high performance computers. In such applications, the photonic IC (PIC)[16] needs to be in close proximity with logic device/SERDES. 2.5D TSI can heterogeneously integrate logic and memory subsystems with photonics that drive optical data communications at sub pJ/bit energy efficiencies. Thus 2.5D TSI technology has the potential to be a key enabler in high speed data communications in the next several decades.

Figure 3 shows a larger picture of the Xilinx Virtex 7HT FPGA. The individual FPGA slices are manufactured using an optimized 28 nm CMOS technology, while the SERDES is manufactured using 28 nm high-performance CMOS technology. This optimized technology choice for the FPGA and SERDES functions allows unprecedented 2.8 Tb/s data transfer capability using 2.5D ICs at lower power consumption. Figure 5 shows how 2.5D/3D TSV/TSI technology can help reduce the footprint of a state-of-the-art logic processor

(CPU) and DDR4 DRAM system. On the left side, we show a PCB which is typically greater than 20 cm on one side. On either sides of the packaged CPU, there are multiple banks of packaged DDR4 memories. The length of interconnect between CPU and memory IOs can be of the order of 10 cm. This results in higher parasitic capacitances, as well as signal reflections due to different physical boundaries. In addition, due to the required bandwidth (BW) of 4 Tb/s between CPU and DRAM total power can be up to 640 W (20 pJ/bit energy consumption for IOs). On the right side of Figure 4, the same system is implemented on a 2.5D TSI that is around 40 mm × 40 mm in size. The four banks of DDR4 are replaced by four 3D stacked high density DRAMs that are in bare die form. The 3D DRAMs are attached to the TSI (yellow color) with fine pitch micro-bumps that can connect thousands of 3D DRAM IOs to the TSI. The CPU, also in an unpackaged, bare die form, is connected to the TSI through fine pitch micro-bumps. The thousands of IOs between the
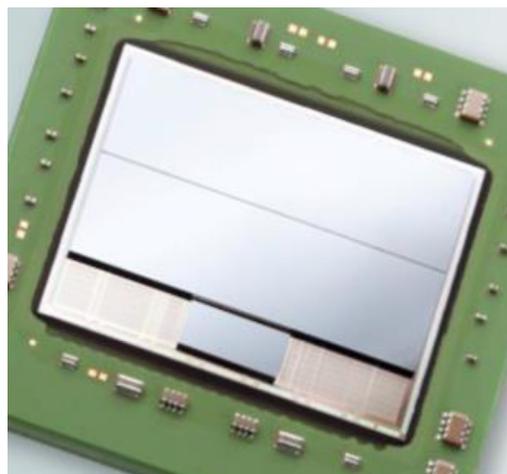

FIG. 3. Xilinx Virtex 7HT with a 2 slices of FPGA integrated with SERDES IC.[12] Reproduced with permission from Madden *et al.*, "Advancing high performance heterogeneous integration through die stacking," in Proceedings of European Solid-State Device Research Conference (ESSDERC) (2012). Copyright 2012 Institute of Electrical and Electronics Engineers.
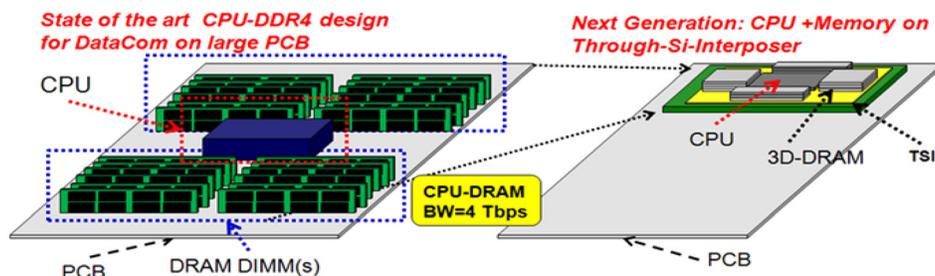
FIG. 4. A typical CPU-memory system showing (a) higher interconnect density and (b) shorter interconnects in TSI based system.

CPU and 3D DRAM are laid out on the TSI using fine pitch copper interconnects. Typically, interconnects in the TSI can support up to 1000 connections per mm cross-section. Because we are using bare die that can be assembled at close proximity (<1 mm), the length of interconnect can be around 10 mm, leading to a significantly lower energy consumption of <3.2 pJ/bit. Therefore, for a BW of 4 Tb/s, the power consumption is 12.8 W, which corresponds to 84% energy saving. Another benefit of this approach stems from the improvement of the form-factor of the sub-system from 20 cm × 20 cm on a PCB to a package size of around 6 cm × 6 cm. The details of the logic memory connection are shown in Figure 5, which schematically shows a TSI that heterogeneously integrates a CPU and 3D memory.

Optical interconnects are known to have the highest bandwidth and lowest power consumption, making them suitable for high bandwidth applications. With future high bandwidth systems, one needs to have optical interconnects to carry data in and out of PCBs that are in server racks. The challenge for using optical interconnects is to bring "optics" as close to CMOS electronics as possible. 2.5D integration using TSI technology can bring optical communication close to high performance CMOS technology—thus allowing servers in datacenters to have the best of both worlds (CMOS technology and optical interconnects). Figure 6 shows another application that benefits from the use of 2.5D TSI technology. It is a high performance line card that may be used in the racks of a server. In this example, an optical fiber connector is used to take data in and out of the line-card. Using 2.5D TSI technology, the PIC and the CMOS drivers can be integrated on the interposer and achieve significant improvements of form-factor. A typical 180 mm × 90 mm line card can be reduced to a 35 mm × 40 mm area. The schematic representation of the Electronic –PIC on 2.5D TSI is shown in Figure 6.

One way to implement optical interconnects is to use photonic integrated circuits. Optical interconnects are implemented through continuous wave Distributed Feed Back (DFB) lasers with Si photonics ICs. Heterogeneous integration of electronic and photonic ICs on TSI allows

independent technology optimization for Si CMOS processors, memory, CMOS/BiCMOS drivers, and silicon on insulator (SOI) PIC. The integration of Si photonics with TSI will enable the performance requirement of data-centers, super-computers, and high-performance-networking to be met (Fig. 7).

B. General summary in advancement

Up to this point, we started with how the exploding data traffic in the mobile society is expected to challenge the way we design and manufacture systems. From the application examples shown above, it can be seen that 2.5D Heterogeneous integration on TSI is a technology platform that can enable system-scaling for the next generation of systems that will be a part of our mobile society. Systems using 2.5D TSI can address both performance and power constraints in a manner that traditional packaging of SoC's built with Moore's law scaling alone cannot. In summary, 2.5D integration allows for a scalable approach to meet power and performance requirements of future generation systems. Heterogeneous integration allows for a manufacturing approach to realize the improvements in power performance metrics that are needed to achieve system scaling for mobile devices, data-centers, and high performance computers. In the rest of this paper, we will highlight the detailed features of this technology to facilitate an understanding of what it takes to design, fabricate, and assemble 2.5D ICs using TSI technology.

C. Challenges for heterogeneous 2.5D integration on TSI

While opportunities abound, as is typical with a technology that is on path to wide adoption by industry, 2.5D heterogeneous integration on TSI has yet to address challenges in the design, fabrication, and assembly of 2.5D[9–11] and 3D ICs.[17,18] In this section, we outline the key challenges faced by TSI technology. Through the course of this paper, we shall elaborate on the same and highlight the techniques and continuing developments that address key challenges.
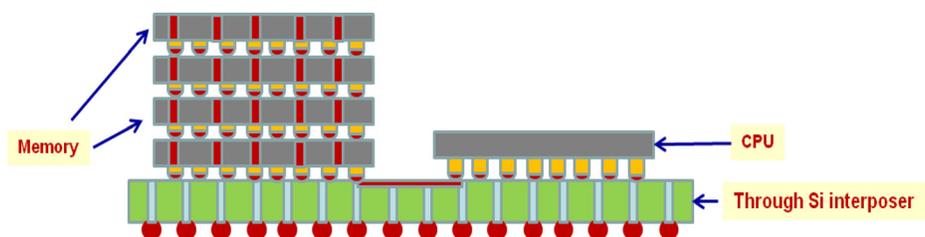

FIG. 5. Cross-section of CPU and 3D memory system showing the die level interconnections.
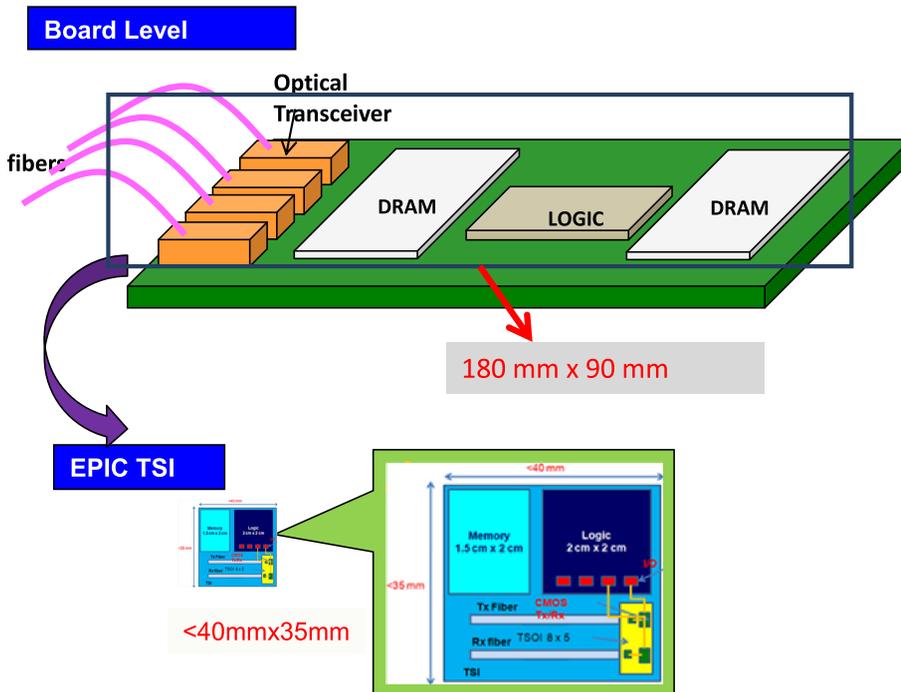
FIG. 6. Electro-photonic integration in TSI in a line card application.

The main technical challenges with designing 2.5D and 3D systems fall in the following areas: (A) Technology planning and design-execution that are necessary for harnessing 2.5D TSI for building systems, (B) processing flow for the fabrication of 100 μm thick TSI at acceptable costs, (C) manufacturing flow for assembling multiple ICs on a 100 μm thick TSI in a repeatable, and reliable manner, (D) thermal management for addressing heat dissipation of 2.5D TSI, (E) thermo-mechanical analysis and optimization for addressing warpage issues, and (F) electrical characterization and process design kit (PDK) for electronic design automation (EDA) flow of 2.5D TSI.

1. Technology planning and design-execution

In designing 2.5D TSI for integrating multiple functions, typically, one needs to start with interconnect planning that would satisfy the design requirements. There are two principle requirements for design engineers: (a) to meet the routing ability requirements of the design and (b) to satisfy the design SI/PI requirements. Routing ability refers to the ability of the TSI to handle the large number of IC-to-IC and IC-to-package interconnections. This is influenced by the available TSI routing area, interconnect size/pitch as well as the number of interconnect layers. More metal layers, larger routing area as well as smaller routing metal size/pitch offer larger routing ability. Increasing the number of metal layers and larger TSI area impose more technology challenges and a concomitant increase in the system cost. In addition, smaller metal size adversely increases the line resistance, giving rise to signal integrity issues. Thus designing a system on 2.5D TSI involves technology planning. For example, there are two fabrication techniques for forming fine-pitch interconnects on a TSI. Typically, two fabrication flows are available to choose from: (1) more expensive Cu-damascene based fine pitch (line width, space $<= 1$ μm; Pitch $<= 2$

μm, Cu thickness $\sim$1 μm with multiple $>$4 levels of interconnects) and (2) less expensive polymer based Cu-redistribution layer (RDL) flow with coarse pitch (Size > 2 μm; Pitch > 4 μm, Cu thickness of 3 μm, with up to 4 levels of interconnects). Thus, a designer needs to optimize the choices based on the application needs of routing and SI/PI requirements versus cost of processing. The next step is the physical implementation[19] of the 2.5D TSI. To do this, one needs accurate electrical models of the TSI (R, L, and C), and a PDK that is implemented on an EDA flow. In addition, testing of 2.5D ICs[20] needs to be addressed as well.

2. Processing flow for fabrication of 100 μm thick TSI

A key challenge with Si processing for TSI fabrication is with the formation of TSVs which involves etching, dielectric deposition, and Cu electroplating to fill the TSVs that are typically formed on the front-side of the TSI. Each of these steps needs to be optimized based on TSV density in the TSI. In addition, processing throughput is also a key challenge to ensure cost-containment for these steps. Another challenge arises from handling thinned 300 mm TSI wafers. Upon thinning, the back-side of the TSI needs specific processing that includes passivation and formation of solder-bumps for attaching to the package substrate. Thin wafer handling is a major challenge in the fabrication of TSI wafers, where industry uses what is called temporary bonding and de-bonding (TBDB).

3. Manufacturing flow for assembling multiple ICs on a 100 μm thick TSI

Upon fabrication of the TSI, individual ICs need to be attached to the top-side of the TSI. This can typically be done in many ways depending on product requirements. One technique involves singulating the TSI into individual dies, and then performing IC to TSI front-side assembly. This is

referred to as chip-to-chip (C2C) assembly flow. After this step, the TSI backside is attached to the package substrate (with multiple ICs assembled on the front-side of the TSI). This assembly flow can be time consuming. Therefore, the industry is moving to a chip-to-wafer (C2W) assembly flow where ICs are attached to the TSI while the TSI is still in a wafer form. Such wafer level packaging (WLP) allows for much higher manufacturing efficiency. Both C2C and C2W approaches have challenges in manufacturing—which need to be addressed to ensure high yields and adequate reliability.

4. Thermo-mechanical analysis and optimization

The TSI with ICs attached to the front-side is assembled on the package substrate using solder-joints as shown in Figures 4(a) and 4(b). The solder-joint is placed under stress due to the fact that Si has a low (3 ppM/°C) coefficient of thermal expansion (CTE) and the organic (laminate) package has a higher (~16 ppM/°C) CTE. The difference in the CTE means that the joined materials expand at different rates during thermal processing and during actual operation when heat is dissipated. This results in solder-joint stress and TSI warpage. Thus, a key challenge in designing a package for 2.5DTSI is to perform accurate thermo-mechanical analysis/finite element-modeling (FEM), and optimize solder joint placement to ensure reliability of the system.

5. Thermal management of 2.5D TSI

With high performance ICs interconnected on the 2.5D TSI, heat dissipation becomes a challenge. This challenge is commonly referred to as thermal management. Thermal management issues can be understood in two aspects. On one hand, the chip-level power delivery could reach high level such as $100 \, \text{W/cm}^2$ for high performance ICs and this requires proximate cooling. Without compromising processing speed, the integration of multi-chips in one interposer on the package tends to generate higher heat density, which in

turn can compromise IC performance. On the other hand, the temperature sensitive chips such as photonic ICs prone to wavelength shifts due to the temperature excursions, which need to be thermally controlled. Thermal management uses passive cooling, or active air-cooling or active liquid cooling. As part of this optimization, one needs to design a thermal solution that meets the needs of the end application.

6. Development of next generation manufacturing equipment

In order to take 2.5D TSI technology to high volume manufacturing, improvements in manufacturing efficiencies are needed. As noted earlier, these improvements are focused on WLP to support TSI fabrication and assembly. Key areas where efficiencies are needed include: (a) TBDB for handling thin TSI wafers. Currently, this process has a throughput bottleneck since just a few wafers can be processed per hour through TBDB steps. (b) Chip-to-wafer bonding— where ICs need to be attached to TSI wafer at high alignment accuracies to support fine pitch (<40 μm pitch) microbumps. Here also, throughput is a key figure of merit.

II. KEY TECHNOLOGY MODULES FOR 2.5D HETEROGENEOUS INTEGRATION

Improvement in VLSI performance by downscaling of device dimensions is faced with limitations in system design due to increased power density, higher I/O count, interconnect bandwidth, and timing closure requirements. Si substrate with TSVs or TSI technology is identified as a solution to overcome these challenges.[21–23] In this section, key 2.5D TSI technology modules and integration schemes are reviewed. Current development status and readiness of each technology modules and the respective processes will also be discussed in detail.

A. TSV module

TSV is one of the essential modules in 2.5D heterogeneous integration. This section will focus on the key TSV
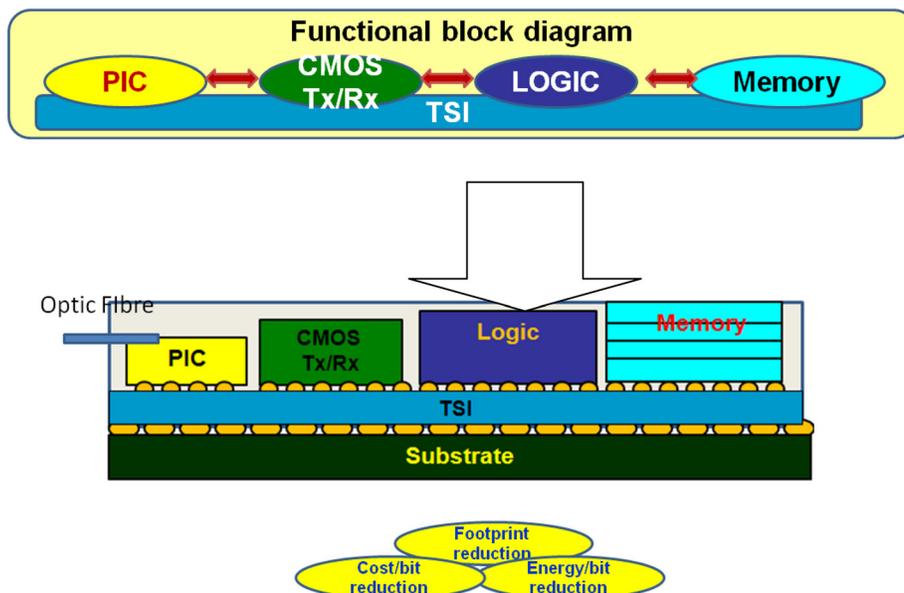

FIG. 7. Functional schematic of electronic–Photonic Integrated Circuits (PIC) on 2.5D TSI.

fabrication processes in a typical TSV integration flow (including TSV etch, liner oxide deposition, Cu barrier seed layer deposition, Cu electroplating, and Chemical mechanical polishing (CMP)).

First of all, there are many approaches to fabricate TSV. In summary, TSV module fabrication can be classified into three main approaches—TSV via-first (VF), TSV via-middle (VM), and TSV via-last (VL). Each TSV approach is defined by the stage (of a CMOS process flow) at which the TSV module is integrated. For via-first approach, TSV is first developed and fabricated before any device fabrication. For via-middle approach, the fabrication of TSV is done after device (contact) and before back end of line (BEOL) process. For TSV-last approach, the TSV is fabricated after device fabrication and BEOL process. In addition, the integration of the TSV-last approach can be further done in 2 different ways: (1) TSV last integration from the top-side of the wafer and (2) TSV last integration from the backside of the wafer.

In any case, the main TSV process modules include: (a) TSV mask, (b) TSV etching, (c) TSV Photo Resists (PRS) and we clean, (d) liner oxide deposition, (e) barrier and seed layer, (f) Cu plating, and (g) Cu CMP. A typical TSV fabrication process flow is as illustrated in Figure 8.

TSV etching, liner oxide deposition, barrier layer and Cu seed sputter deposition, Electro-copper-plating (ECP) and Cu CMP will be described in subsequence.

1. TSV deep Si etch process

TSV etching is a forming of high aspect ratio (AR) Si etch process. Deep Si etching (from a few tens of to a few hundreds of μm) is technically more challenging than shallow, low aspect ratio etching in conventional CMOS Si etching process.[24]

As such, high aspect ratio TSV etching faces many challenges. In particular, high etch rate is required for large volume production. Other challenges relating to deep Si etch include the control of sidewall roughness, tilt, sidewall angle, micro-loading, notching, and micro-grass. Currently, a time-multiplexed process, which is more commonly known as

Robert Bosch GmbH's process (BOSCH Process), has become the main TSV etching process adopted by the industry.[25,26]

Bosch etch process is performed using a multiple inductively coupled plasma etching system. It is an alternating two-step process, consisting of a polymerization step and a Si etch step. The Si etch step rapidly removes the polymer layer on the bottom of the feature while partially removing the polymer layer on the sidewall, protecting the sidewall. Etch and passivation steps are alternated until the desired etch depth is reached. Typically, SF_6 and O_2 are applied as gas source in the Si etching cycle while C_4F_8 is applied as polymer generation source during the sidewall passivation cycle. Due to the strong isotropic nature of the SF_6/O_2 etch chemistry, each etch cycle will form an unwanted sidewall recess known as a scallop. The formation of this unwanted scallop repeats with each etch cycle. The etch mechanism due to SF_6 gases can be explained as follows:[26]

$$SF_6 + e^- \rightarrow SF_5^+ + F + 2e^-. \quad (2.1)$$
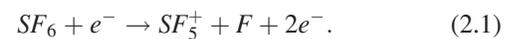
Usually, 10% of O_2 is added to help in liberating more fluorine radicals in the plasma reaction between SF_6 and O_2. Si is then subsequently etched away by the fluorine according to the following reaction:[26]

$$Si\,(solid) + 4F(gas) \rightarrow SiF_4(gas). \quad (2.2)$$
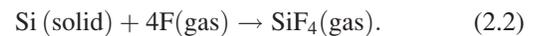
During the passivation phase of the BOSCH process, CF_2 is formed from C_4F_8 as follows:[26]

$$C_4F_8 + e^- \rightarrow C_3F_6 + CF_2 + e^-. \quad (2.3)$$

CF_2 then adsorbs on the surfaces and forms a Teflon-like polymer according to the reaction[26]

$$nCF_2 \rightarrow (CF_2)_n. \quad (2.4)$$

During the etch phase, the CF_2 molecules are removed by a combination of physical ion sputtering and chemical reactions. The physical component in the Bosch process is contributed by the positively charged $S_xF_y^+$, and the chemical etch is mainly due to the F and O_2, which are generated

FIG. 8. Major process modules in TSV formation. (a) TSV mask lithography, (b) deep Si etch, (c) PRS and wafer cleaning, (d) liner oxide deposition, (e) barrier metal and Cu seed sputtering, (f) Cu ECP, (g) Cu CMP, and (h) TSV capping deposition if needed.
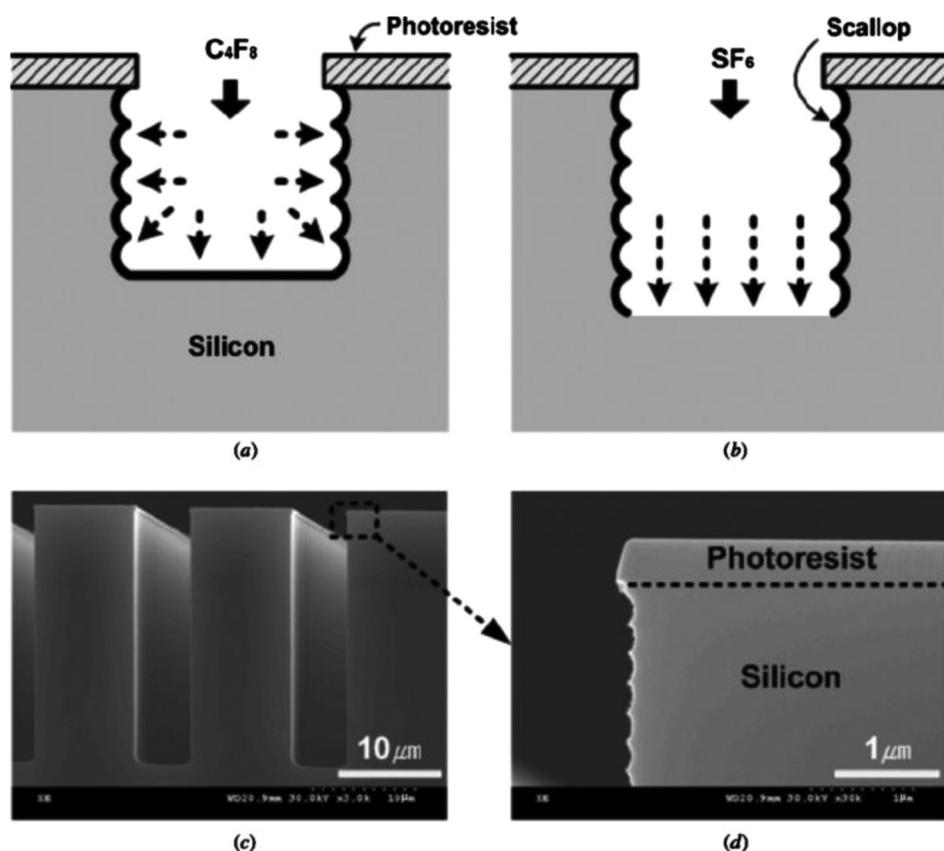
FIG. 9. Schematic of Bosch method: (a) sidewall passivation using C4F8, (b) Si isotropic etching using SF6, (c) SEM images of deep trenches, and (d) magnified SEM image of the sidewall showing nano-scallops.[27]
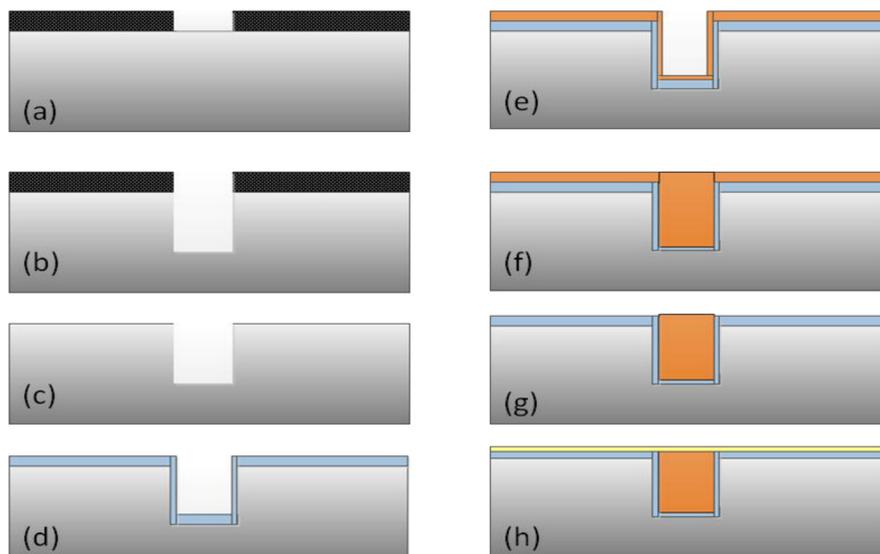
during each etch step. The scallops are due to the isotropic etching mechanism as shown in reaction (2). A schematic of the Bosch etch process is illustrated in Fig. 9.[27,28] Figure 10 shows a 10 μm diameter by 100 μm depth TSV etch profile obtained via Bosch etch process.

Although Bosch process is able to meet the requirements of a TSV etch, there are still issues associated with the process. Some issues in TSV Bosch etch include micro-loading effect, undercut (also known as over-hang), Si grass, undercut, and notching. Wu *et al* did a detailed review on the loading effect and Si micro-grass for TSV etching, with corresponding proposed solutions.[27] The undercut issue had been observed more frequently in via-middle scheme[29] and TSV in SOI wafers.[30] Figure 11 shows SEM images of undercut issues in TSV fabrication. Both undercut and scallop will result in liner coverage uniformity issues, barrier metal and Cu seed step coverage issues, which will then cause incomplete TSV filling or leave voids inside TSVs. This effect becomes more pronounced as the TSV diameter gets smaller. On the other hand, notching is normally observed in via-last scheme when the etching gas hits the boundary between Si and the underlying layer, as shown in Figure 12.[27] The reason is charge accumulation that occurs where Si is underlain by a dielectric layer. Increasing the thickness of polymer during over etch by increasing is proposed to prevent notching issue.[31,32] Another method to control notching is to apply intermittent or pulsed bias RF power to cathode.[33,34]

The post-etch cleaning of the TSV is a critical process. In particular, the F-containing polymers deposited during the passivation cycle of a Bosch process have to be removed fully before downstream process

2. TSV liner deposition

TSV liner deposition is a process that is used to deposit a layer of dielectric film, e.g., typically SiO_2, along the sidewalls of the deep Si via, and it is used as an electrical

FIG. 10. TSV profile after deep reaction ion etching by using Bosch method. The size of TSV shown in the figure is 10 μm in diameter and 100 μm in depth, which has been widely accepted for interposer application.

FIG. 11. Undercut issues of TSV etching. (a) Undercut of TSV in SOI wafer,[30] (b) undercut of TSV in via-middle scheme,[29] and (c) improved etching recipe showing less undercut.
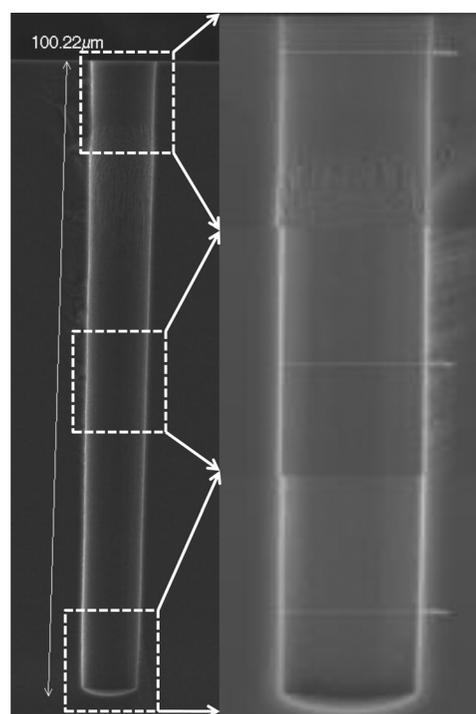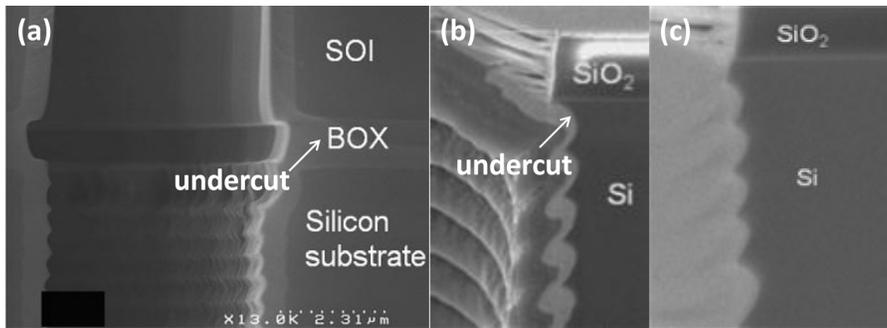
isolation for the TSV structure. It can be done either by using high temperature thermal oxide deposition or by plasma enhanced chemical vapor deposition (PECVD) with the use of silane and tetrathylorthosilicate (TEOS).[35,36] There is wide application of Sub-atmospheric CVD (SACVD) of Ozone (O3)-TEOS as liner in TSV formation.[37–39] Different TSV approaches have different requirements. But the basic requirement that is expected for liner deposition is good step coverage for the TSV insulation from the Si substrate. Thermal oxide is used in the TSV first approach because high temperature process will not have any effect on the active devices since the TSV is fabricated before the front end of line (FEOL) process. SACVD oxide is commonly used in the TSV middle and via last from top-side approach because the active devices are fabricated before the TSV integration. High liner deposition temperature can affect the performances of the active devices in via middle approach and the BEOL in the TSV last from top-side approach. The type of pre-cursor that is more commonly used in the SACVD process for the TSV middle and TSV last from top integration is TEOS. The reason being that using TEOS (as the pre-cursor) will give a better SiO_2 step coverage than silane (as the pre-cursor) in the PECVD process. Low temperature ($<250\,^\circ$C) TEOS-PECVD is normally used in the TSV VL from backside approach due to the thermal budget limitation of the type of bonding material used. SEM images of TSV liner oxide at different depth are shown in Figure 13, and Table I summarizes the liner oxide step coverage (SC) at various TSV depths and wafer locations.

3. Seed layer and barrier layer deposition

Next key process after liner deposition in TSV fabrication is the barrier and seed layer deposition. The purpose of the barrier layer is to prevent any copper (Cu) diffusion from the TSV into the Si during any subsequent high temperature process. The deposition of the barrier and seed layer is normally carried out using a chemical or physical vapor deposition (CVD or PVD).[40] CVD-based process technology (e.g., metal organic chemical vapor deposition (MOCVD)) can cater for barrier and seed deposition in very high aspect ratio ($>$15:1) TSVs but incurs higher cost and is not the mainstream process in the industry. Conventional PVD process is less costly but poses more limitations with respect to step coverage on the TSV side wall. Improvements in PVD equipment have extended the process window for PVD barrier and Cu seed layer deposition.[39,40] Tantalum (Ta) and Ti
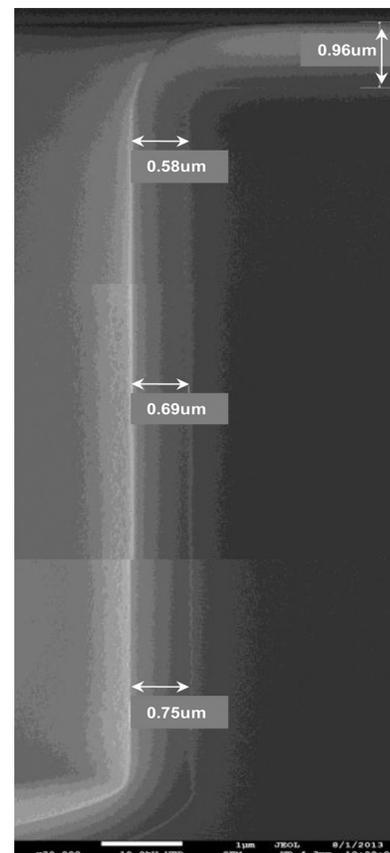

FIG. 12. Notching observed at the interface between Si and SiO_2 layer.[27]

FIG. 13. SEM images of O3-TEOS liner oxide for a TSV with the diameter of 10 μm and depth of 100 μm.

TABLE I. Summary of the liner thickness in various TSV depths and die locations.

Die location	Field (μm)	Invia field (0.21 μm)	Top sidewall (μm)	SC (%)	Middle sidewall (μm)	SC (%)	Bottom sidewall (μm)	SC (%)	Bottom (μm)	SC (%)
Bottom	0.95	0.74	0.62	83.8	0.69	93.2	0.77	104.1	0.75	101.4
Center	0.98	0.77	0.58	75.3	0.73	94.8	0.73	94.8	0.71	92.2
Edge	0.92	0.71	0.62	87.3	0.69	97.2	0.74	104.2	0.73	102.8
Left	0.93	0.72	0.6	83.3	0.68	94.4	0.75	104.2	0.73	101.4
Middle	0.96	0.75	0.58	77.3	0.69	92.0	0.75	100.0	0.75	100.0
Top	0.92	0.71	0.64	90.1	0.73	102.8	0.78	109.9	0.78	109.9

are prevalent barrier metals used. These barrier layers also have the function of improving the adhesion between TSV Cu and the liner dielectric. After barrier deposition, Cu seed is sputtered in a separate chamber. Ar plasma is first applied to the metal target that is used for sputtering. The metal atom is then dislodged from the metal target and deposited onto the bottom wafer surface to form the metal film. SEM images of a PVD barrier metal and Cu seed at various depth in a 10 μm × 100 μm TSV are shown in Figure 14.

The continuity of barrier metal and Cu seed is the basic and most essential requirement of the PVD process. As shown in Figure 14, the barrier metal and Cu seed fully covers the side-walls surface within the TSV. Ti step coverage can achieve 0.63%–5.97% at different depth of TSV. PVD Cu has better step coverage compared with Ti. Typical step coverage of Cu is about 1.06%–6.03% in a 10 μm × 100 μm TSV.

4. ECP

ECP process is another important process step in the fabrication of a TSV. The purpose of this step is to fill up the deep Si etched TSV with either copper or other types of conducting materials (aluminum or tungsten) for the TSV. Via plating defects can have various negative effects on the TSV interconnect properties and subsequent TSV processes. Voids in the TSV fill can cause variations in via resistance, or even electrically open-circuit connections.

ECP is a plating process in which metal ions in a solution is moved by an electric field to coat an electrode.[41] ECP can be done using either by conformal or bottom-up deposition methods, and that will depend on the types of chemistry and electroplating conditions that are used. Conformal Cu deposition for the TSV is fast but will result in a high Cu overburden in the field region and a potential high risk of voids in the TSV. On the other hand, bottom up plating method has lower risk of void formation, and there will be less Cu overburden even though the process time is long. A TSV ECP process encompasses a combination of both conformal and bottom-up methods.

The ECP bath chemistry plays an important role in the TSV filling process. The presence of organic additives in the bath chemistry has strong influence on the Cu deposition process. In summary, there are three main types of organic additives applied to optimize the process of TSV filling—suppressor, accelerator, and leveler. Suppressor is a long
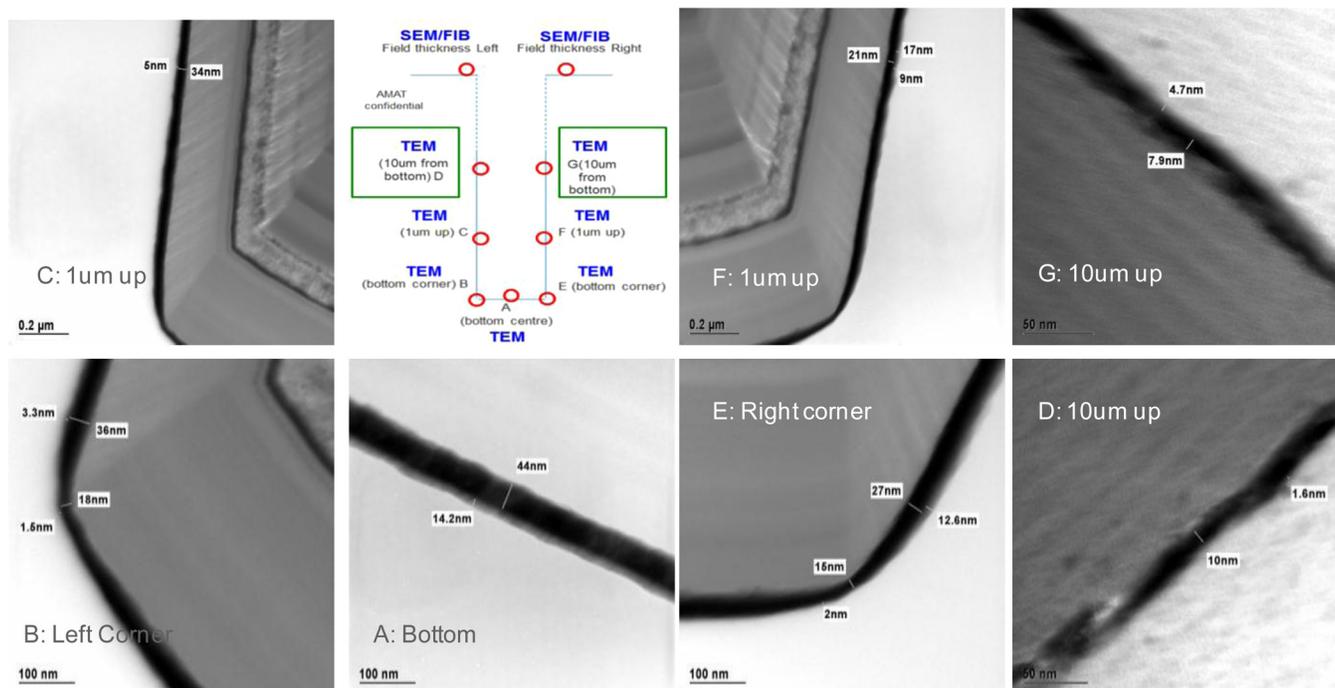
FIG. 14. SEM images of Ti and Cu as barrier and seed layer for 10 μm × 100 μm TSV.
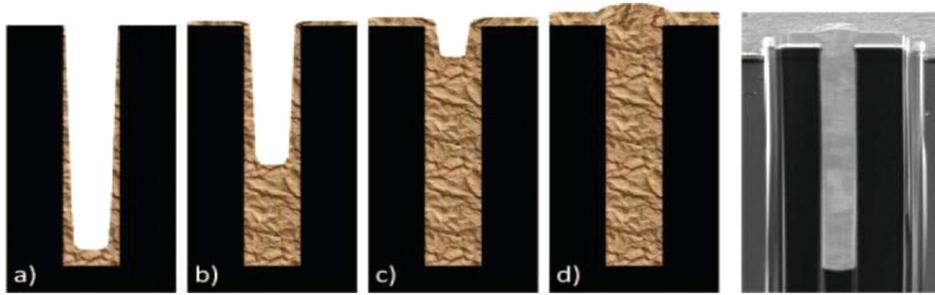
FIG. 15. Cu filling process to form a void-free TSV. (a) Initial stage, (b) intermediate stage, (c) final stage, and (d) void-free Cu filling and the image of actual TSV after Cu filling.

chain polymer and is usually used to coat the Cu surface to create a "blocking layer" during Cu deposition. Accelerator is a catalyst that is used during the Cu deposition process to increase the Cu deposition rate. A leveler is applied to deactivate the effect of the accelerator.[41]

Nowadays, the TSVs are mostly filled with Cu by ECP process. This step is considered as the most critical step for TSV formation, because it determines if the Cu filling is successful. If there are any issues in the process, Cu filling defects, also known as voids, will be observed inside the TSVs. Figure 15 shows the conventional model of bottom up filling for void-free TSV Cu filling when all processes are controlled well.[42] Choi *et al.*[42] and Malta *et al.*[43] have studied and investigated the mechanism of failure and defect generation of TSV filling during ECP process, to realize a low-cost 3D IC based on the TSV. X-ray is a non-destructive method employed to inspect for voids in TSVs. Figure 16 shows x-ray and X-SEM images of TSV with $10\,\mu m$ in diameter and $100\,\mu m$ in depth. Throughput and Cu overburden reduction remain as key challenges to be addressed for cost saving.[44] A thick Cu overburden will not only affect overall throughput but also cause failures due to the serious warpage. In the case of a $10 \times 100\ \mu m$ TSV, a well-optimized TSV Cu filling process by electroplating should typically have a Cu overburden thickness of below $4\,\mu m$. In addition, because the Cu overburden thickness depends on the TSV dimensions, it can be much thicker for bigger dimensions of TSV applications.

5. CMP

After the ECP process of the TSV, CMP has to be carried out to remove any Cu overburden and Cu mounts that have occurred during the ECP process.[45,46] The Cu TSV will have to be exposed by using a CMP process in order to proceed with further process integration.

Conventional Cu CMOS process needs to go through a high temperature annealing step before Cu CMP in order to achieve Cu grain stability. Because most of TSV wafers have thicker Cu overburden, e.g., $>4\,\mu m$, two-step Cu CMP process are employed for surface planarization. Higher Cu overburden will cause wafer to have a higher warpage after TSV Cu CMP. The first copper CMP process is carried out right after copper ECP process, the wafer is then sent for Cu annealing, followed by a second Cu CMP process to remove the remaining Cu protrusion and Cu annealing defects. The mechanisms involve in the CMP process of different types of metals are relatively simple. In general, an oxide of the metal is chemically formed on the metal film surface. It is then removed mechanically with abrasives in the CMP slurry.[46] A hybrid e-CMP/CMP has been proposed by Takeda and co-workers[47] and applied for Cu TSV CMP, and this method shows higher Cu removal rate as well as minimum dishing of $100\,nm$ for TSVs with $100\,\mu m$ diameters. Figure 17 shows typical images of TSV after CMP process.

B. BEOL and RDL scheme

For fine pitch and high density TSV interposer, industry is looking at multiple interconnect layers on the interposer front side with less than $5\,\mu m/5\ \mu m$ L/S and via diameter

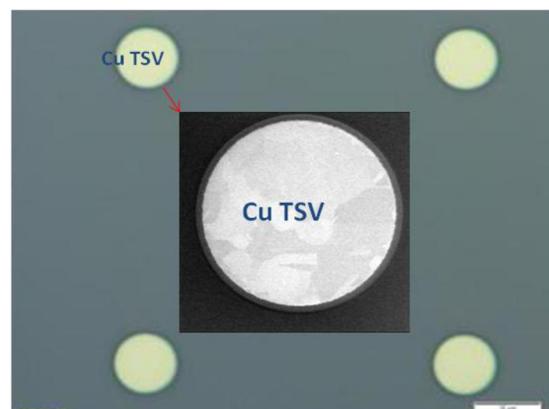FIG. 16. X-ray (a) and X-SEM images (b) of $10\,\mu m \times 100\,\mu m$ TSV after ECP.

FIG. 17. Optical inspection and SEM inspection (inset) results of $10\,\mu m \times 100\,\mu m$ TSV after CMP process.

less than $10\,\mu$m. To achieve fine pitch Cu routing in through Si interposer, the main stream technology adopted is foundry-based BEOL process.[48] BEOL fabrication is based on single or dual Cu damascene process with inorganic dielectric materials, e.g., SiO_2, Si_3N_4, or low-K materials. In damascene process, the underlying dielectric insulator material is patterned and etched with open trenches and vias and a thick layer of Cu is deposited to overfill the etched structures. CMP is then used to remove the Cu overburden leaving Cu filled in the trenches. Cu remaining in the trench forms the conducting traces.

Compared to damascene process, polymer-based Cu RDL process offers lower cost interconnect solution, since it avoids deep ultraviolet (DUV) lithography, plasma etching, and CMP process. The RDL process involved using a semi-additive process to form Cu conducting traces and photo-pattern-able polymer materials are used as the dielectric insulating layer. The contact via opening can be formed directly in the polymer material by photo-lithography and developing the material away. Polymer-based Cu RDL process offers a cost effective interconnect solution, since it avoids DUV lithography, plasma etching, and CMP process. As shown in Figure 18,[49] process step count of polymer-based RDL is reduced by ∼45% as compared with dual-damascene process, and ∼60% as compared with single damascene process. However, current polymer-based Cu RDL processes are normally coarse in terms of L/S and photo-lithography resolution of photo-dielectric materials are often very poor in achieving very small contact via opening. Fine-pitch

polymer-based RDL process is becoming more in demand under the pressure of cost reduction of 2.5D interposer and 3D-IC.

RDL process is a standard process in the packaging area.[50,51] IME has been developing RDL process for packaging application with wider dimension.[52] Later, low temperature damascene interconnect has been developed for 3D interconnect.[53] Shrinkage of RDL has become a popular topic of interest recently. Spin-on photo-dielectric based Cu RDL integrated with TSV interposer was reported with $4\,\mu$m/$4\,\mu$m line/space (L/S) and $10\,\mu$m in via diameter by Kumagai *et al.*,[50] and Ho *et al.* reported $2\,\mu$m/$2\,\mu$m L/S RDL with $2\,\mu$m polymer via diameter.[49] Taiwan Semiconductor Manufacturing Company, Limited (TSMC) reported 0.8-μm/0.8-μm L/S RDL in VLSI 2014.[54] The shrinkage of RDL has become an important research direction in the foundry for cost reduction in TSI application.

$2\,\mu$m/$2\,\mu$m line/space (L/S) RDL was developed and characterized in Ref. 49. Figure 19 shows the cross-section of 2 layers polymer-based RDL meander (a) and daisy chain (b) and (c) structures fabricated on Si wafer. Metal 1 layer consists of $2\,\mu$m/$2\,\mu$m L/S Cu traces fabricated using the semi-additive process. Metal 2 layers consist of $2.5\,\mu$m line width Cu trace with $1.5\,\mu$m/$1.5\,\mu$m line/space in Figure 19(a). The 2 layers are insulated by polymer-based dielectric material. The spin-on polymer-based material shows good gap-filling capability with no voids observed in between the line space. The daisy chain consists of metal 1 and 2 with

Polymer-based RDL
- Polymer lithography
- Polymer curing
- Seed layer PVD
- PR Photo Patterning
- RDL Cu Plating
- PR Stripping
- Seed layer etching

Dual Damascene
- Dieletrics CVD
- Trench lithography
- Trench etching
- PR stripping
- Wafer cleaning
- Via lithography
- Via etching
- PR stripping
- Wafer cleaning
- Seed layer PVD
- Damascene Cu plating
- Cu annealing
- CMP

Single Damascene
- Dieletrics CVD
- Via lithography
- Via etching
- PR stripping
- Wafer cleaning
- Seed layer PVD
- Damascene Cu plating
- Cu annealing
- CMP
- Dieletrics CVD
- Via lithography
- Via etching
- PR stripping
- Wafer cleaning
- Seed layer PVD
- Damascene Cu plating
- Cu annealing
- CMP

FIG. 18. Comparison of process steps of different Cu wiring processes, i.e., polymer-based RDL, dual damascene, and single damascene.
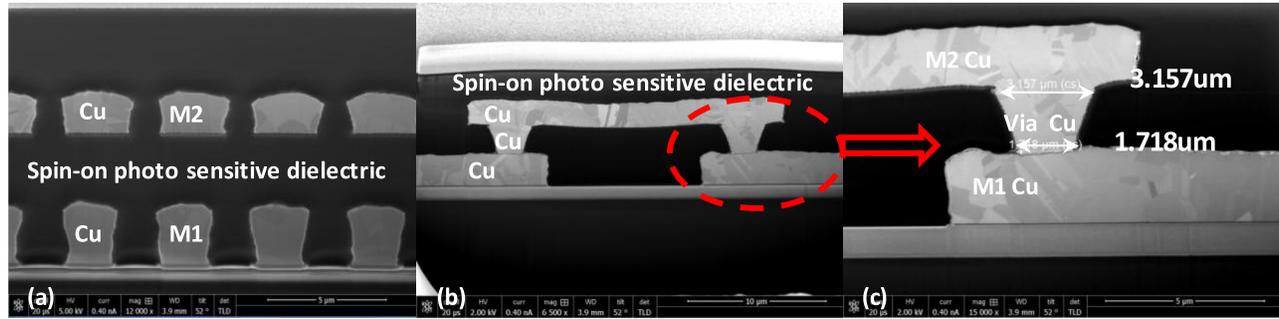
FIG. 19. Cross-section of (a) 2 layer fine pitch RDL meander, (b) daisy chain structures, and (c) enlarged view of via.

vias connecting the 2 metal layers in Figure 19(b). The contact via is enlarged and shown in Figure 19(c) that has a tapered slope profile. The top opening diameter for the contact via is ~3.2 μm, and the bottom diameter is ~1.8 μm. The tapered slope via sidewall is preferred in RDL processing as it allows better step coverage of the PVD seed layer.

C. Bumping

1. Solder bumping and Cu pillar bumps

Solder bumping technology (the process of joining a chip to a substrate without shorting using solder) is first conceived and implemented by IBM in the early 1960s. Fine pitch solder micro-bumps are one of the key elements to form high density interconnections on a through Si interposer or functional dies. To meet Tera-scale computing needs and to reduce power consumption for next generation information devices, short and high density interconnections between high-capacity memory chips and microprocessor unit are required.[55–57] In order to achieve interconnections with low resistance, most frequently solder micro-bumps are made up of Cu and a solder cap, i.e., Cu pillar bumps. Figure 20 shows the evolution map of Cu pillar bumps. Table II below shows summarization of bumping technology for chip to chip interconnects in terms of scaling and bonding technology.

As compared to solder bumps, the pillar bumps are more rigid and thus allow assembly with only a small solder volume on top of pillars. This results in two benefits: (1) the standoff can be kept high even with very fine pitch, and (2) the solder will not spread out much on wettable surfaces Nowadays, fine pitch Cu pillar bumps are applicable in various packaging technologies, from wire bonded chip stacking to chip stacking with TSVs, from system in package (SiP) to 3D IC integration. As a result, Cu pillar bumping technology has attracted intensive attentions. As to the assembly, different metallurgical bonding processes have been developed, such as solid-liquid-inter diffusion method[58] and thermal compression method.[59,60] In IBM, Wright *et al.* developed

solder micro bumping technology.[61] Different solder materials, such as e-PbSn and CuSn systems, have been studied.

Fine-pitch Cu pillar bumps have replaced conventional flip chip solder bumps driven by the need for extremely low profile and high connectivity interconnects. Devices, such as high-end processors, graphics, FPGAs, power amplifiers, MEMS, and High brightness light emitting diode (HB-LED), have incorporated fine-pitch Cu pillar bumps and demonstrated the range of the technology. Figure 21 shows four SEM images of 40 μm pitch copper pillar bumps capped with SnAg solder.[62] The SnAg solder reflows to join the die to the Si interposer. Sub-40 μm pitch has also been demonstrated.

2. Bumps in 2.5D TSI package

To support high speed data transfer and preserve signal integrity between dies, a very fine-geometry circuit board and enabling interconnect solution is required. TSIs and fine-pitch Cu pillar bumps are two representative technologies that have played an integral role in defining the 2.5D package approach. Figure 22 shows the schematic of a typical 2.5D TSI system with two-die side-by-side integration. Interposer inclusion defines the 2.5D approach. It routes thousands of interconnections between the devices. IC1 and IC2 can also serve as TSV-enabled 3D stacks. As shown in Fig. 21, Cu pillar microbumps provide short, low inductance, efficient interconnections (a) between ICs in vertical stacks as well as (b) between and IC and the through Si interposer. Together, the micro-bumps and Si interposer provide a high-speed and high-bandwidth communication high way for side-by-side die (and stack) placement. The interposer bottom fans out to wider pitches that employ conventional solder bumps for connection onto the ball grid array (BGA) substrate.

3. Fabrication of Cu pillar micro-bumps

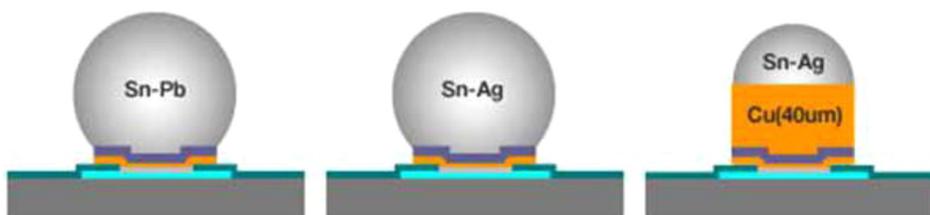The structure and production process of a pillar bump are very similar to an electro-plated solder bump.
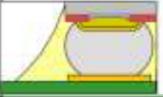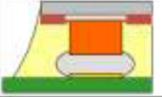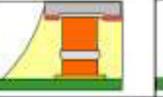

FIG. 20. Evolution map of Cu pillar bumps by Samsung.

TABLE II. Scaling of chip-to-chip interconnect.

Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level
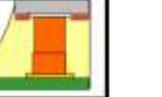
- A thin sputtered adhesion layer (e.g., Ti or TiW) covers the chip pad and overlaps onto the chip passivation.
- A sputtered conductive plating base (Cu) is required as a 2nd layer for the subsequent deposition steps.
- A barrier layer (e.g., Ni or Cu) is electroplated to prevent inter diffusion of solder and pad. In the case of a pillar bump, this layer is extended to a tall pillar of several $10\,\mu$m height.
- Solder (e.g., lead-free SnAg) is plated on top of the barrier or pillar and reflowed to form a solder bump or cap.

In the case of a solder bump, the standoff between chip and substrate, on which the bumps are soldered, is determined by the controlled collapse of the large solder volume.

The surface tension of the molten solder keeps the chip at a distance during flip chip assembly. A solder mask around the substrate pads and the non-wettable chip passivation prevents the solder from spreading out indefinitely. One major benefit of collapsible bumps during reflow is that the formation of the flip chip bonds is very robust and highly tolerant to bump height variations. The pillar bumps, on the other hand, are more rigid and thus allow assembly with only a small solder volume on top of the pillars, which has two clear benefits, i.e., (1) the standoff can be kept high, even at very fine pitch, and (2) the solder will not spread out much on wettable surfaces, even without a solder mask barrier, due to the restricted solder volume. The main drawback of the

FIG. 21. SEM images of Cu pillar bumps.

FIG. 22. Schematic of a typical 2.5D TSI system with two-die side-by-side integration.

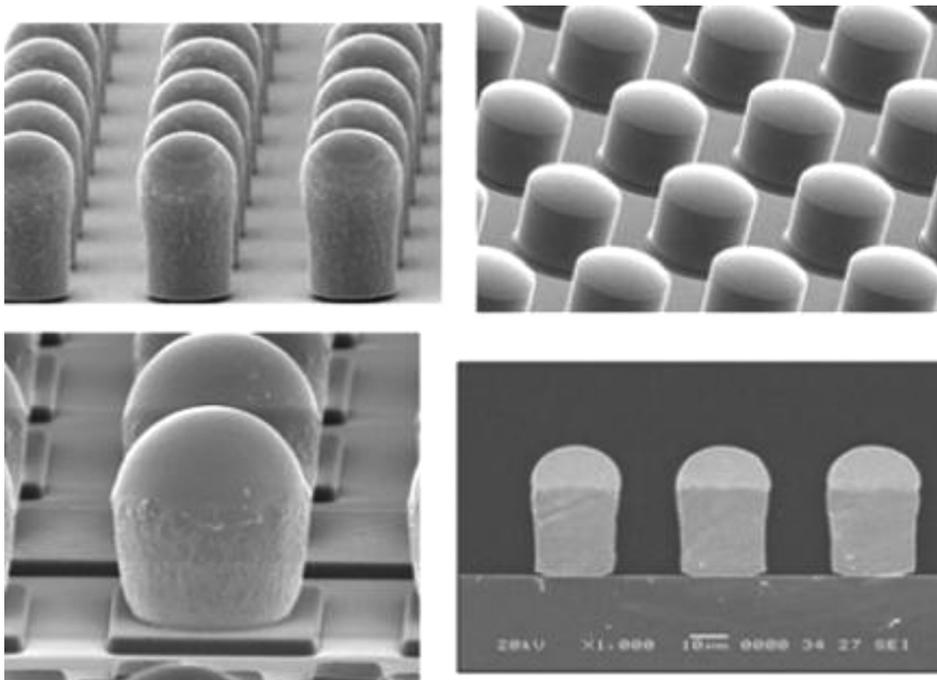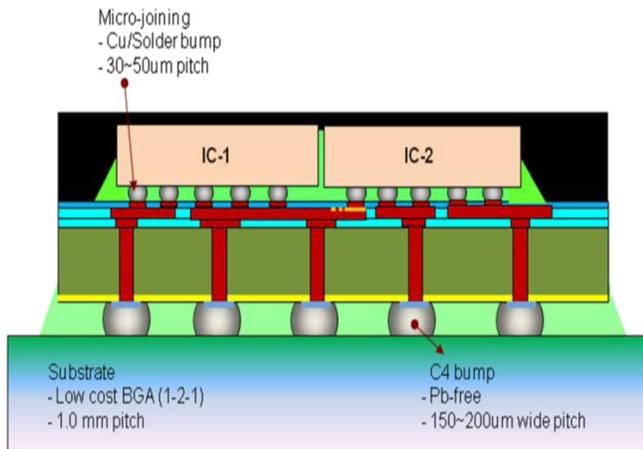reduced collapse of the small solder cap is that it requires tighter bump co-planarity control to prevent non-wetting of shorter bumps.

A tall Cu pillar offers additional advantages: thermal and electrical conductivity are higher than in a solder ball of similar size. Even more importantly, electro-migration (EM) reliability performance is much better in a Cu pillar where current crowding at the corner between chip and pad and bumps is located within higher EM-resistance bulk Cu instead of low-melting solder. A thin under bump metallurgy (UBM) in a solder bump cannot prevent high current densities at bump corner caused by current crowding. This leads to EM induced voids at the UBM/solder interface, which finally causes an open interconnect after high-current stress. The solder cap of the pillar bump makes it possible to use identical assembly process, assembly materials, and assembly equipment as for a solder bump of the same material.

$<50\,\mu m$ pitch Cu pillar bumps are reported by several organizations.[63–71] IME reported their studies on fine-pitch (40 μm) Cu pillar process integration and proposed a combined of wet and dry etching of seed layer removal method to reduce the Cu pillar undercut issue.[66] IMEC reported on 10 μm electroplated CuSn micro-bumps with 20 μm pitch in 2011.[68,69] With further scaling down of Cu pillar bump diameter, seed layer etching was found to be a more and more important processing parameter to form finer pitch Cu pillar bumps. The seed etch process is compared between Ti/Cu and TiW/Cu seed layers. During Ti etch, the etch rate dropped when the Al measurement pads are exposed. In

order to remove the Ti layer between bumps to prevent shorts, the etch time needed to be increased, resulting in a non-uniform attach of Al measurement pads due to severe galvanic effect. With a TiW/Cu seed, no damage on the Al probing pads is observed. In addition, the TiW/Cu based bumps has no undercut, while on the Ti/Cu bump at each side more than 1 μm undercut was observed. TiW was concluded as the preferred seed layer for fine-pitch Cu pillar bump. Based on the yield of the daisy chains, a defective density of the bumps below 50 ppm is predicted. ITRI reported results on their 12 μm micro-bumps (5 μm Cu/3 μm Ni/2.5 μm SnAg) with 20 μm pitch.[70] Severe undercut caused by seed layer etching process is also found. Figure 23 shows the typical undercut of Cu pillar bump and the improved process for minimizing the undercut.[70] Huang *et al.* reported that the reduction of Cu seed layer thickness from 5000 Å to 2000 Å and a dry etching process have been found to improve the undercut performance.[70] Cu pillar bumps with sub-20 μm pitch have also been reported by IME (15 μm pitch)[66] and Tohoku University (10 μm pitch).[67] For IME's 15 μm pitch Cu pillar bumps, traditional electrochemical plating is used to deposit the Cu and Sn sequentially followed by photo resist stripping and seed layer etching which was carried out by a combination of wet Cu etching and dry Ta etching. Tohoku University reported an electroplated-evaporation bumping (EEB) technology to form 10 μm pitch Cu pillar bumps, which is a combination of Cu electroplating and Sn evaporation. Resistance of Cu/Sn bump was measured to be 35 mΩ/bump.

4. Reliability assessment of Cu pillar bumps

Samsung did high temperature storage (HTS) test for Cu pillar bumps with 20 μm in diameter and found that Ni_3Sn_4 intermetallic compound (IMC) formations at interface between SnAg solder and their 4 μm Ni UBM degrade the mechanical properties of solder joint and increase resistance of solder bump.[71] IMC growth rate and Ni UBM dissolution rate are calculated. The IMC changes into thick IMC during HTS as shown below in the SEM images. As shown in Figure 24,[71] thin IMC changes into thick IMC during High Storage Temperature (HST). During 150 °C HST, Ni UBM is converted into Ni_3Sn_4 IMC, but resistance of the microbumps remains unchanged. Resistance started to degrade after 1000 h at 180 °C storage due to void formation at interface between IMC and Al trace line, resulting in open failure upon complete consumption of Ni UBM. Figure 25 presents
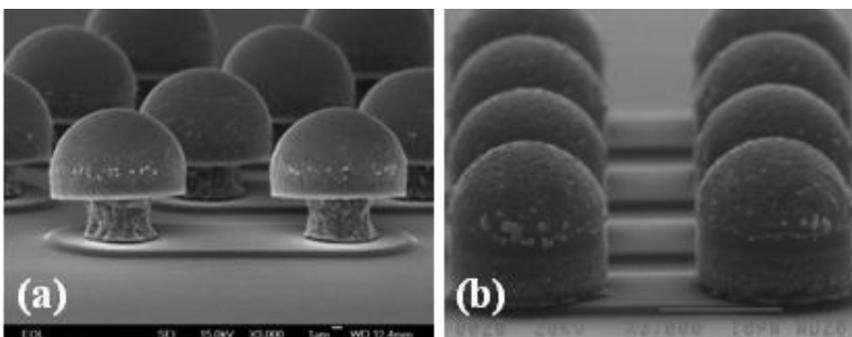

FIG. 23. Cu pillar bumps (a) with severe Cu post undercut and (b) fabricated with optimized process having minimized Cu post undercut.
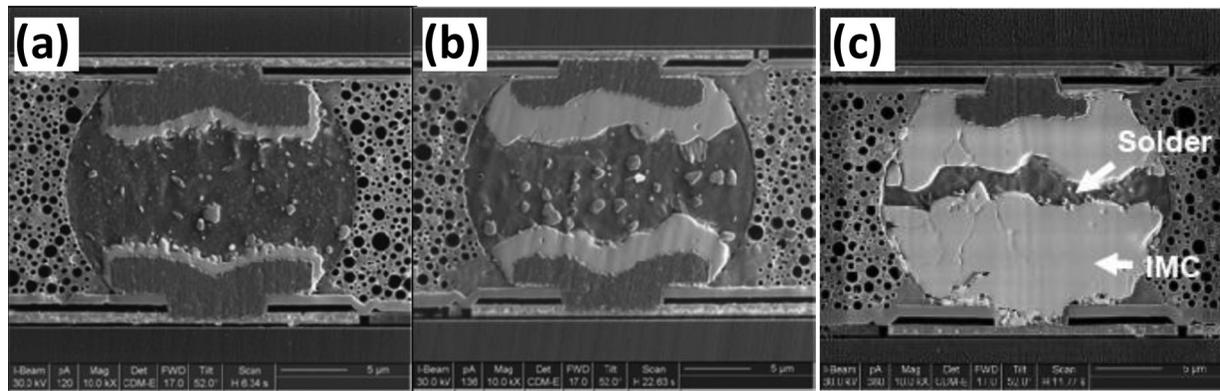
FIG. 24. SEM images of solder joints (a) as reflow condition, (b) HTS 150 °C for 1300 h, and (c) 180 °C for 1300 h.

the resistance evolution with time during HTS test at 150 °C and 180 °C, respectively.

ITRI has also studied the failure mechanism of 20 μm pitch using thermal cycling (TC) test.[70] The IMC formed at the interface is identified as Ni_3Sn_4. The IMC thickness is also found to increase with time and/or temperature, which is consistent with the results reported by Samsung. Ni normally functions as a diffusion barrier to inhibit the reaction of Sn and Cu having very low solubility in Sn. During the bonding process, the bottom interposer is at 100 °C, and the top chip is at 280 °C to melt SnAg solder alloy. It is concluded that the bonding temperature drives Ni atoms to dissolve into the melted solder and saturates the Sn matrix. As Ni has higher density than that of Sn, gravity segregation occurs and causes the Ni atoms to accumulate at the interface and result in the thicker Ni_3Sn_4 formation. It is proposed that the failure mechanism of the micro-joints, as shown in Figure 26, is due to a Sn depletion zone which forms at the interface between Ni layer and Sn solder of the top chip due to the consumption of Sn. Eventually, the crack propagated along the interface and then the micro-joint fails when stress induced by Z-axial expansion of underfill is exerted on the interface.

EM is the migration of metal in the direction of electron flow which results in void formation at the electrons entrance (or current exit, I-) and metal pile-up at the electrons exit (or current entrance, I+). Since void formation is the most detrimental effect of EM, the current exit I- is the most critical interface. While there have been many EM studies of 100 μm and larger bumps, there are not many studies on fine pitch Cu pillar bumps, especially below 20 μm size. It was found that with good Ni barrier structures, CuSn bumps may have EM

lifetimes similar to or greater than eutectic PbSn bumps.[54,61] Samsung reported EM accelerated life time assessment for Cu pillar bumps. Figure 27 shows the microstructure of micro-bumps with 6.4×10^4 A/cm^2 current stressing and without current stressing for 624 h at 150 °C.[71] In Figure 27, polarity effect was observed. During current stressing, the migration direction of Ni is the same as the electron flow, so Ni UBM at cathode side was consumed. Also migrated Ni from cathode to anode enhances IMC growth at anode. It is calculated based on memory device application conditions of 105 °C. The EM life time of Cu pillar bump with Ni UBM achieved more than 100 years based on 0.1% EM failure, as shown in Figure 28.

IMEC has studied on the EM performance comparison between solder flip chip bumps (thin layer of Ni/Au UBM and a SAC solder) and Cu pillar bumps (40 μm Cu pillar with 20 μm SnAg cap) with same diameter, i.e., 60 μm.[72] A clear difference in EM behavior was observed between standard NiAu/SAC and Cu pillar bumps. Figure 29 shows SEM images of solder bumps under thermal stress without and with EM stress for both standard solder bump and Cu pillar bump.[72] Standard bumps with Ni/Au UBM show a consistent failure mechanism of micro-structural degradation through void formation at the interface of solder and IMC, and this occurs for all test conditions used (150–170 °C and 300–500 mA). However, Cu pillar bumps did not show any electrical, nor micro-structural degradation. It was concluded that less current crowding for Cu pillar bumps was expected that that of solder bumps, which causes less local EM damage. The other reason of the outstanding EM performance of Cu pillar bumps is its faster formation of a full intermetallic phase. As soon as all solder materials is transferred into
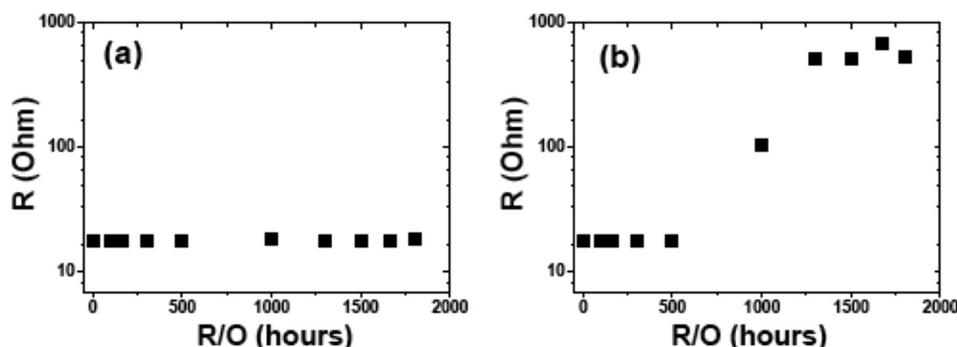

FIG. 25. Resistance as a function of storage time during HTS test at (a) 150 °C and (b) 180 °C.

(a) Before bonding   **(b) Bonding**

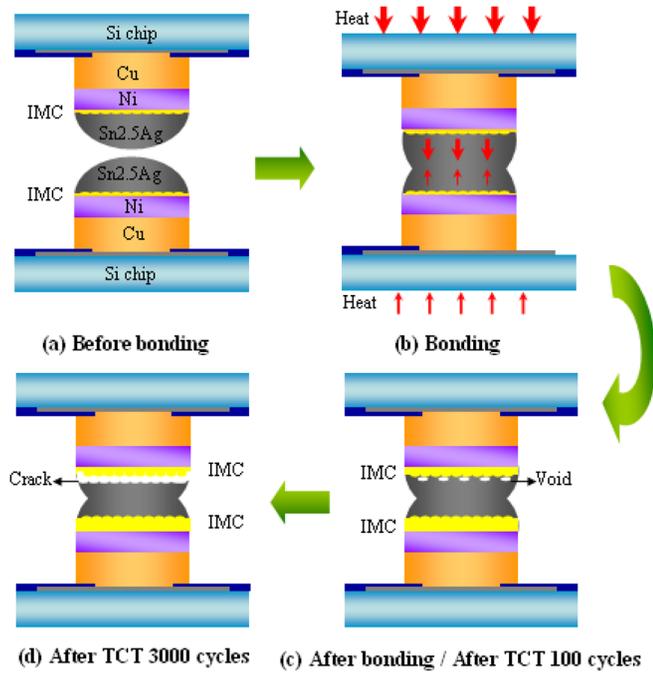**(d) After TCT 3000 cycles**   **(c) After bonding / After TCT 100 cycles**

FIG. 26. Schematic diagrams of the failure mechanism of micro-joint. (a) Before bonding, (b) bonding, (c) after bonding/after TCT 100 cycles, and (d) after TCT 3000 cycles.

FIG. 28. Log-normal distribution of EM failure at 150 °C under various current densities of (a) $6.4 \times 10^4 \, A/cm^2$, (b) $5.6 \times 10^4 \, A/cm^2$, and (c) $5.1 \times 10^4 \, A/cm^2$.

intermetallic phase, the joint is no longer expected to fail at reasonable testing conditions which are compatible with packaging materials.

D. Thin wafer handling

TSVs are continuously being scaled down for various benefits. These benefits include higher I/O densities, smaller form factor, reduced process cost, and smaller keep-out-zones (KOZ) for logic devices. TSV dimensions indirectly determine the thickness of an interposer. However, as TSV dimensions are scaled downwards (in particular TSV depth), wafer handling becomes an issue. For wafer thickness below 100 μm, warpage becomes an issue without any support. As such, the device wafer would have to be temporary supported on tape or on a carrier wafer by means of adhesives.[73,74] Figures 30 and 31 illustrate a typical bonding and debonding process, respectively.

In summary, thin-wafer handling can be simplified into different categories based on (1) type of carrier and handling wafer and (2) bonding and debonding mechanisms.[52,53]

1. Carrier substrates

The substrate used is highly dependent on the temporary bonding/debonding systems used. Si carrier wafer is preferred in most cases when light source or laser is not needed to be shined onto the wafer. For cases where solvent is needed to pass through the carrier, perforations are needed; for cases where light needs to pass through the carrier wafer for debonding, glass substrates will need to be used.

2. Temporary bonding and debonding

As illustrated in Figure 32, current temporary bonding methods encompass mechanical peel-off, thermal slide, solvent and laser (light) release.[73,74]

Mechanical release or peel-off systems make use of adhesives that are bonded and debonded at room temperature. This process is very dependent on the adhesives used. The adhesive should have enough strength to hold the bonded wafers together during grinding and processing but still allow the bonded wafer to be peeled apart. Thermal slide process, on the other hand, uses a combination of heat and pressure to bond the wafers together. The maximum sustainable process temperature and the debonding temperature are limited by the bonding temperature. Si carrier wafer is mainly used for both mechanical and thermal slide-off process and have good total thickness variation (TTV). Solvent release involves the use of a carrier wafer with perforations, which serves to allow solvent to get in touch with the adhesives that bonds the wafer to the perforated carrier wafer.
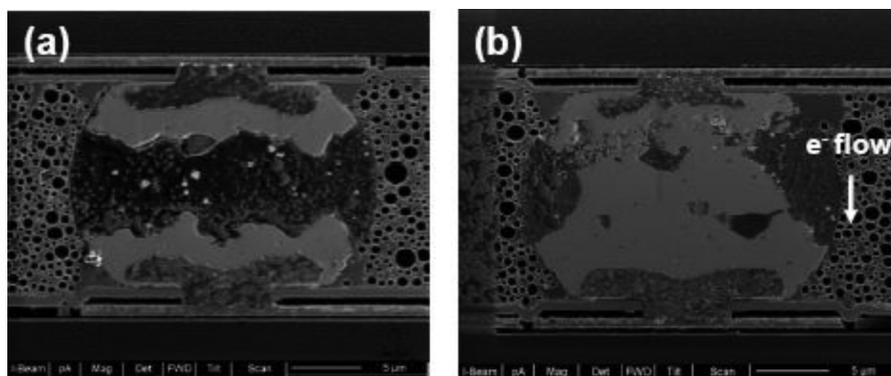
FIG. 27. SEM images of solder bump (a) without current stressing for 624 h and (b) with EM current stressing of $6.4 \times 10^4 \, A/cm^2$ for 624 h at 150 °C.
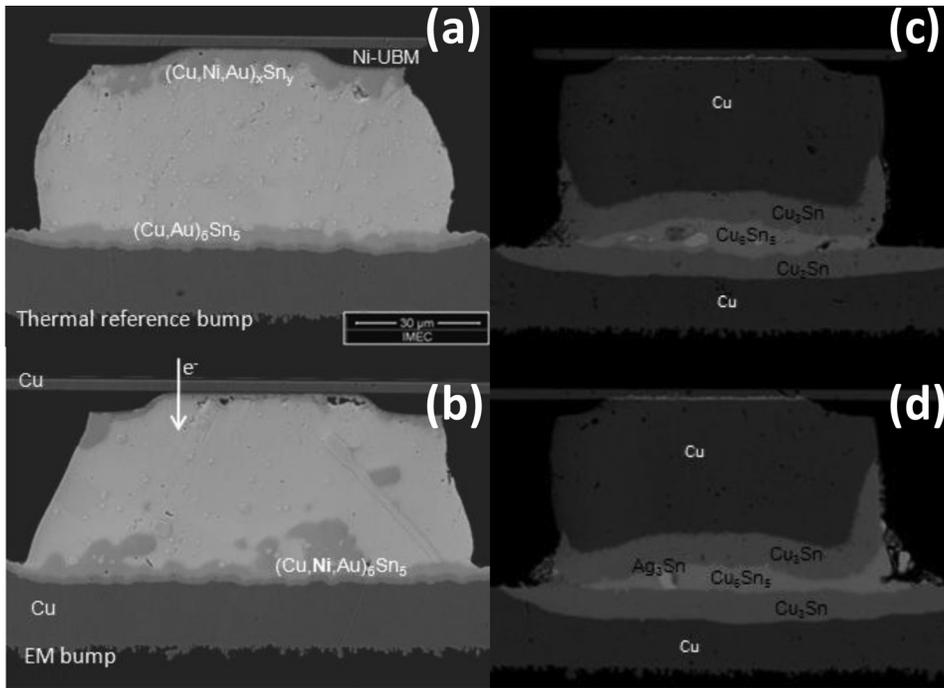
FIG. 29. Cross-sectional images of bumps after EM testing. (a) Thermal reference solder bump at 150 °C without EM stress, (b) solder bumps at 170 °C with EM stress of 500 mA, (c) thermal reference Cu pillar bump at 170 °C without EM stress, and (d) Cu pillar bump at 170 °C with EM stress of 300 mA.[72] Reproduced with permission from Labie *et al.*, "Outperformance of Cu pillar flip chip bumps in electromigration testing," in *Proceedings of the 61st Electronic Components and Technology Conference (*ECTC), Lake Buena Vista, FL, USA (2011), p. 312. Copyright 2011 Institute of Electrical and Electronics Engineers.
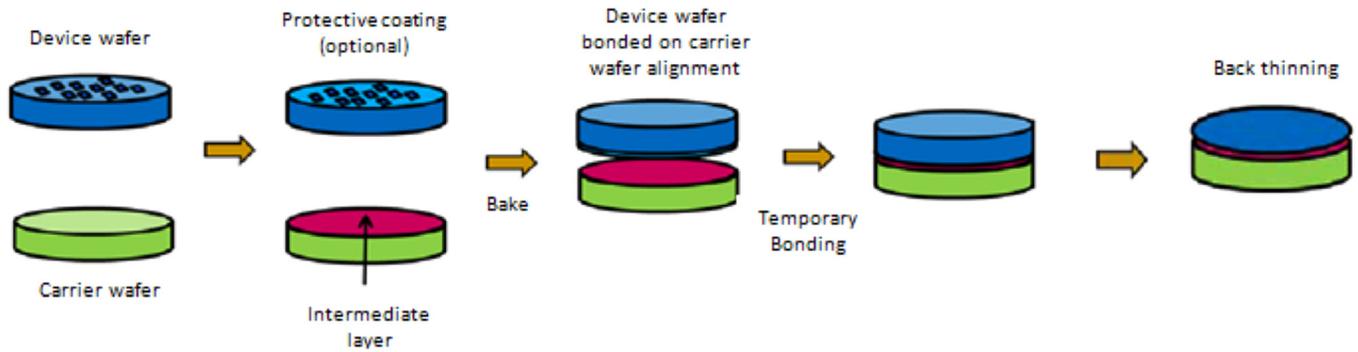
FIG. 30. A typical temporary bonding process flow.
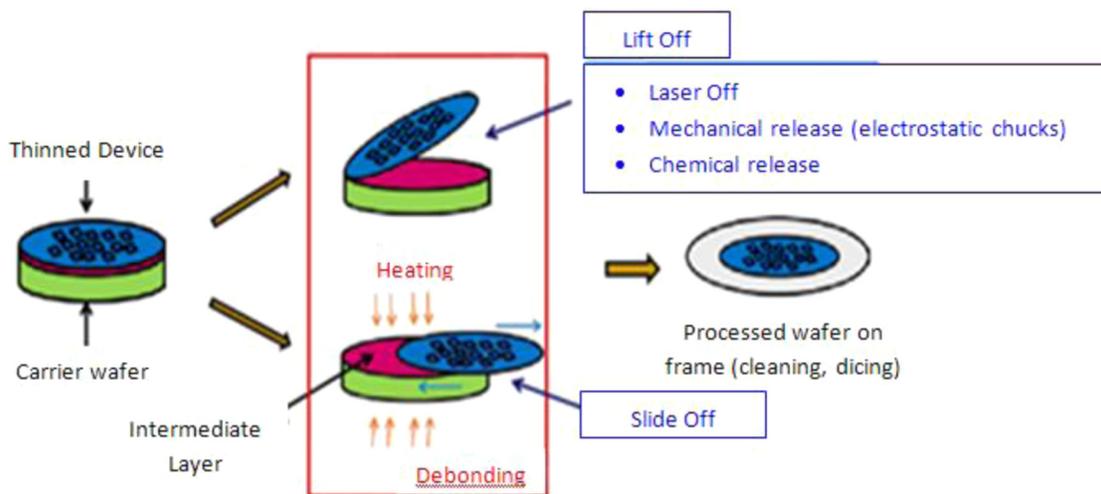
FIG. 31. A typical debonding process flow.
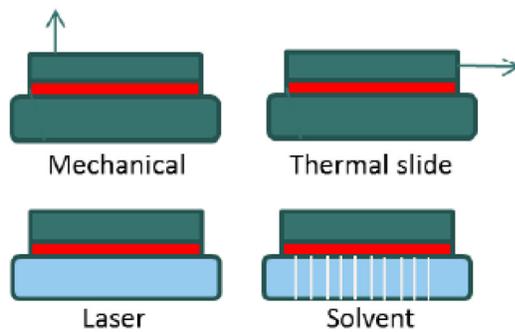
FIG. 32. Temporary bonding and debonding processes.

However, contamination of tool chucks can be a possible issue. In addition, the holes in the wafer can get dirty or clogged over use with time. Lastly, in laser release process, laser/light sensitive adhesives are used for bonding. Laser-bonded wafers are basically debonded by passing laser or light through the backside of the carrier wafer. This approach is thermally stable, however, only glass substrates can be used. Table III shows a summary of the various temporary bonding and debonding systems.

3. Adhesives requirement

High temperature resistance, chemical resistance, high mechanical strength, low TTV capability, low out-gassing, easy and clean removal of adhesives, and costs are some of the key requirements of temporary bonding and debonding adhesives. Depending on the use and application, not all of these requirements are critical. The selection of requirements, the respective adhesives, and bonding systems is very dependent on the user application and subsequent processes.

III. 2.5D TSI ASSEMBLY CHALLENGES

A. Introduction

A typical 2.5D interposer package consists of one or multiple guest dies stacked on top of a thinned TSV interposer, which is in turn assembled on either an organic flip chip BGA (FCBGA) or a ceramic substrate.[75–79] Figure 33

shows an example of a 2.5D interposer package. The two guest chips could be assembled side-by-side on the interposer as shown in the schematics or be replaced by one or more stacks of multiple dies (for example, memory cube). By using the 3D stacking of multiple chips, the total Si area that can be housed in a single package is significantly increased. It also dramatically improves the device performance due to the extremely short interconnect for between die communication. In this section, assembly flow and challenges of 2.5D TSI package are reviewed.

B. TSI package assembly process flow

There are 3 basic 2.5D TSI assembly flow options: chip-on-chip first (CoC-first), chip-on-substrate (CoS-first), and chip-on-wafer first (CoW-first). For each of the flip chip attach process, there are choices of using mass reflow or thermal compression bonding (TCB) to form the solder joints between two tiers of chips or substrate. Upon the completion of the flip chip solder joint connection, underfill is applied to encapsulate the gap between the two tiers of the chip or substrate for the purpose of pro-longing the solder joints fatigue life and creep performance. The underfill also serves as environmental protection agent to avoid solder corrosion. There are several underfill process flow options as well.[80–83] The most commonly used underfill methods for TSI assembly are non-conductive paste (NCP) and capillary underfill (CUF). The NCP is applied during flip chip attach and can only be used in conjunction with TCB assembly, while the CUF is used after the flip chip attach is done and can be used in conjunction with both TCB and mass reflow chip attach processes. Figure 34 shows examples of the block diagrams of two commonly used process flows for CoS-first and CoC-first assembly. The text descriptions of each process flow and the pros and cons are in Secs. III B 1 and III B 2. The CoW-first assembly flow integrates the TSV wafer processing with guest chip attach before completion of the TSI wafer fabrication and is known as chip-on-wafer-on-substrate (CoWoS).[77–79] Section III B 3 describes the CoWoS process and an example of the assembled package.

TABLE III. Summary of carrier wafer and corresponding wafer handling methodologies.

| Carrier type	TBDB mechanisms	Advantages	Disadvantages
Silicon canter	(1)Thermal slide-off (2) Solvent release (3) Mechanical release	(1) Compatible wish semi eqpt (2) Available with good TTV (3) Low cost	(1) Edge trimming for carrier wafer (2) Temperature limited (3) Cannot use UV/laser debondling process
Glass carrier	(1) UV/laser release	(1) Can check wafer after each process (2) Can use UV/laser release	(1) Higher cost to achieve good TTV (2) CTE not matched with Si (3) Easier to break (4) Not compatible with ESC (cannot try mechanical release)
Perforated glass	(1) Solvent release	(1) Allow solvent release	(1) Perforated holes degrade TTV (2) Higher cost (3) Not compatible with ESC (cannot try mechanical release)
Carrierless	No need debonding	(l) No carrier needed. No TBDB (2) Low cost	(1) Non-standard post processing required. Not compatible with some semi process tools (2) Need special grinder
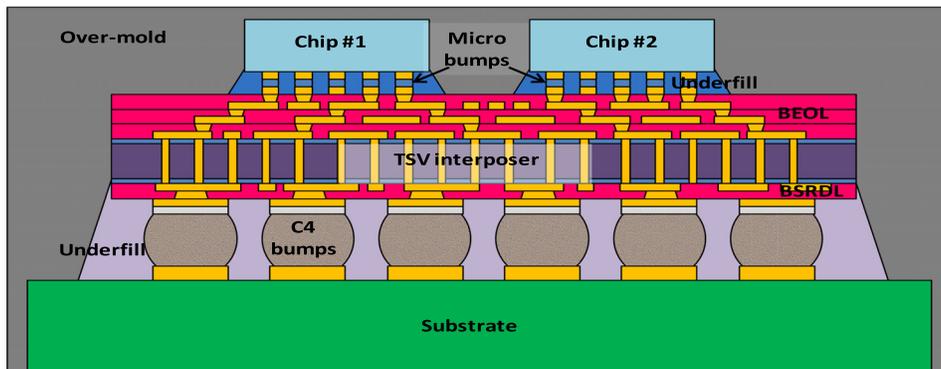
FIG. 33. Schematics of 2.5D package with two guest dies assembled side-by-side on top of TSV interposer.

1. Chip-on-substrate (CoS) first assembly flow

In this process flow, the TSI die is flip-chip attached onto the substrate (CoS) first. The chip attach can be done by either a mass reflow plus CUF or by TCB plus NCP process. Once the CoS is completed, the guest dies are assembled onto the CoS stack by TCB plus NCP process to complete the process for final test. The advantage of this assembly flow is that it allows testing of the KGD (known good dies) TSI before committing to the expensive functional guest dies and avoids wasting of costly functional dies. The disadvantage of this assembly flow is that the tier 2 assembly of guest dies onto the CoS could be challenging if the CoS (i.e., TSI on Substrate) has large warpage due to the difference in CTE between Si (CTE ~ 3 ppm) and organic substrate (CTE ~ 16 ppm) which is further amplified for large size TSI die. A highly warped CoS could hinder successful micro-bump connection between the guest dies and the TSI. It also could hinder underfill flow to successfully fill the gap between the guest dies and the TSI. The usage of ceramic substrate which has similar CTE with Si chip can be used to mitigate the warpage issue.

2. Chip-on-chip (CoC) first assembly flow

In this process flow, the guest dies are flip chip attached onto the TSI chip (CoC) first. The chip attach is done by one of these three process flows: (#1) mass reflow plus CUF, (#2) TCB plus CUF, or (#3) TCB plus NCP process. Once the CoC assembly is completed, the CoC die stack is assembled onto the substrate by mass reflow plus CUF to complete the assembly for final test. While it is easier to control the micro-bump assembly in the CoC-first approach than the CoS-first approach due to smaller virgin-TSI die warpage than assembled CoS stack warpage, the handling of the CoC stack for next tier assembly (i.e., assembly of CoC onto substrate) and post-CoC stack warpage has to be managed for a successful assembly of the CoC onto substrate. Figure 35(a) shows a severely warped CoC die stack failed to make full contact with substrate bondpad after flux tacking and before solder reflow. However, the solder joints were successfully formed between the CoC TSI and the substrate after solder reflow (Figure 35(b)), although the solder joints were stretched at edges of the TSI. The biggest disadvantage of this CoC-first approach is that it is not possible to test the post-CoC joints for a KGD selection to avoid potential waste of expensive functional dies if the TSI itself or the CoC assembly is not good.

3. Chip-on-wafer (CoW) first assembly flow

In this CoW-first assembly flow,[77–79] the guest dies are flip-chip bonded on TSI wafer after the completion of TSV formation, front-side multi-layer interconnect, and front-side micro-bump formation, but before back-side wafer thinning and TSV reveal during the TSI wafer fabrication. After the completion of guest chips attach, the CoW wafer is molded and thinned down to 100 μm or less from the backside to reveal the TSV and is followed by C4 bumping process before it is singulated into individual "CoW" dies for assembly onto substrate to complete the CoWoS process flow. This CoW-first assembly flow is heavily promoted by TSMC and is called CoWoS[77–79] technology. The schematics of the CoWoS process flow are shown in Figure 36. Examples of a TSV wafer which is populated with guest dies (CoW) and an assembled TSI package are shown in Figure 37.[77] The CoW-first flow is favorable for micro-bump joining due to the low

FIG. 34. Assembly flow options for TSI packaging.
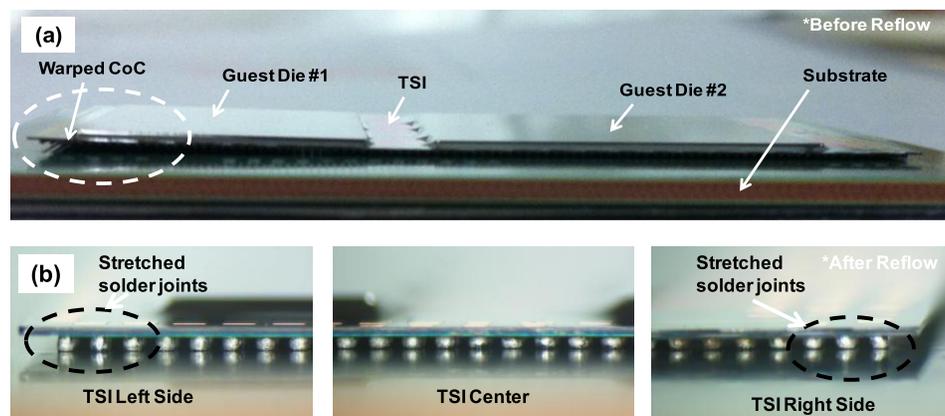
FIG. 35. CoC-First assembly: (a) before reflow and (b) after reflow (Courtesy of Institute of Microelectronics).
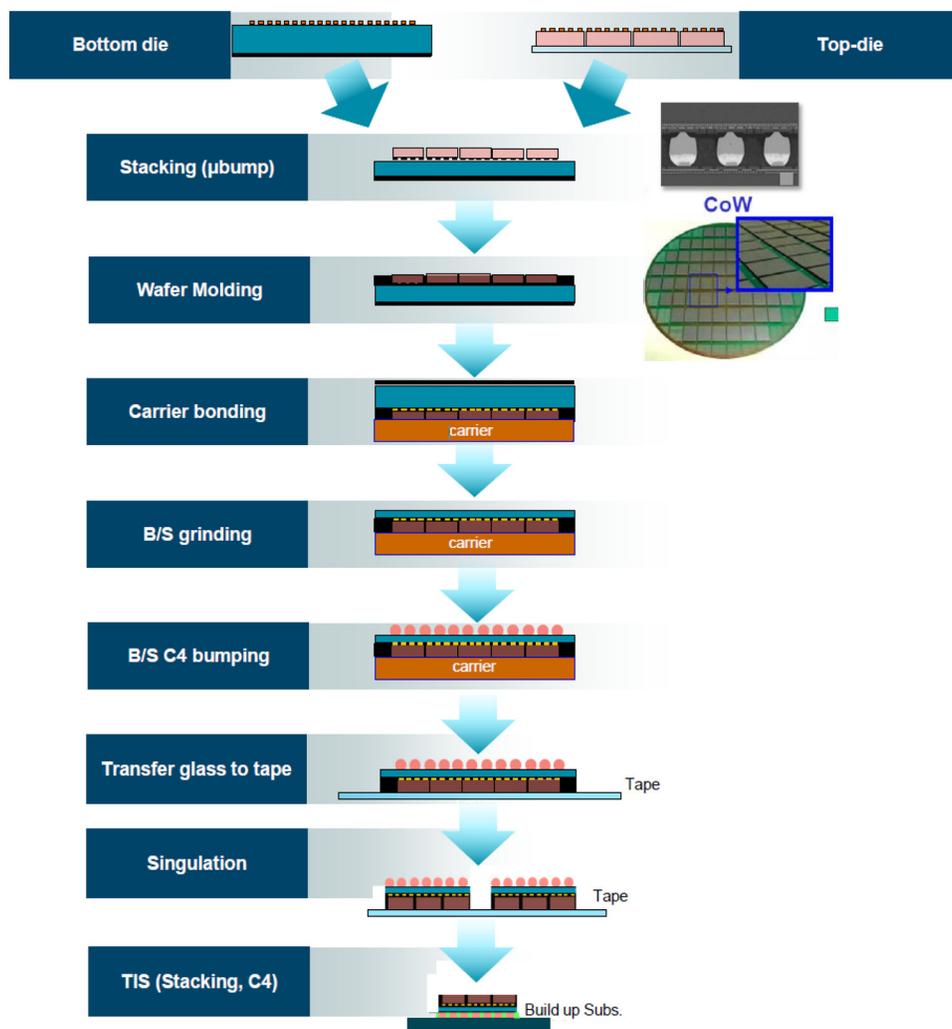
FIG. 36. CoWoS process flow.
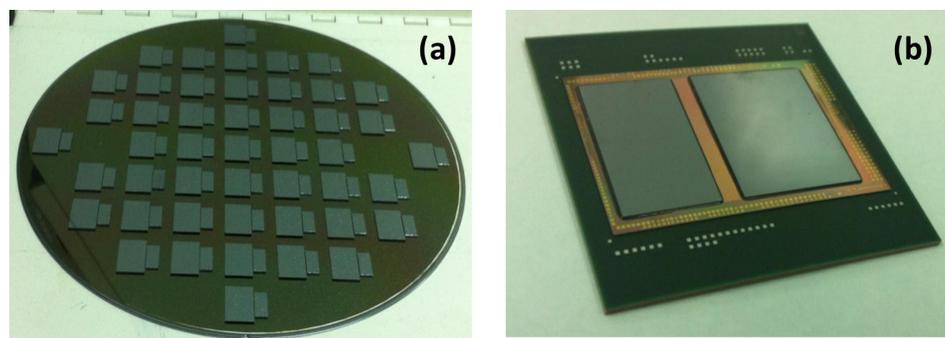
FIG. 37. (a) The top view of chip-on-wafer and (b) chip-on-TSI-on-substrate.

warpage of the full thickness Si wafer, and no need of thin wafer handling during die attach process. However, the wafer level warpage becomes quite severe after the CoW wafer is overmolded with epoxy mold compound for the downstream processing and may require expensive investment in tools for stringent inline warpage control.

C. Assembly Challenges and Warpage Control

Although all the basic steps to assemble 2.5D TSI package (flip chip attach, solder reflow, thermo-compression bonding, underfill, over-mold encapsulation, etc.) are available in the traditional flip chip packaging technology, the integration of these steps coupled with the requirements of ultra-thin die (100 μm and below), super-fine pitch (50 μm and below), small underfill gap (20 μm and below), and three-dimensional stacking have made the 2.5D/3D assembly very challenging for not only materials selection and process development but also assembly tool capability of handling highly warped/stressed and fragile wafer, die, and package. For a successful 2.5D TSI assembly, the multiple levels of interaction among Si chip, bump interconnect, underfill, substrate, and mold compound has to be considered starting with the package physical design/routing and materials selection, the assembly flow sequence selection (CoC-first or CoS-first, or CoW-first), and the assembly tool capability to handle such high level of complex integration.

The warpage issue arises from the CTE mismatch between Si and substrate. By adding underfill between these two components to enhance solder joint reliability and encapsulating the device and substrate with epoxy mold compound to protect the package can make the package warpage either worse or better, depending on the mechanical and thermo-mechanical properties of the underfill and mold compound, and the relative thickness of each components. There is no one-size-fits-all remedy for this challenge. Use modeling and simulation to predict the warpage, especially the warpage at assembly temperature, is a very useful and economic way to help select a suitable assembly process flow for a given package design and material set to minimize the process development time.

Figure 38 is a schematic illustration of the warpage related assembly issues. Three assembly issues can be easily seen from this schematic: (a) Bumps merged at the area
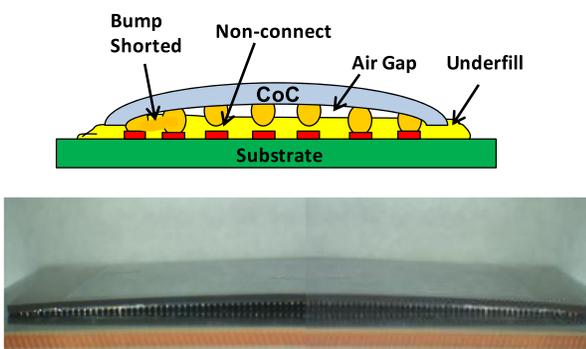
where the space between bumps become small, (b) bumps not connected due to extra distance between bump and substrate bondpad, and (c) underfill fails to fill the gap between chip and substrate due to extra space/height. The relationship of process flow sequence and warpage is experimentally demonstrated by Murayama *et al.*[84] In this study, the test vehicle consists of two guest dies of $10 \times 10 \times 0.75$ mm size and 50 μm size micro-bumps; a TSI interposer of 26 mm $\times$ 26 mm $\times$ 0.1 mm size, 10 μm/50 μm diameter/pitch TSV, 2 metal layers on top and 1 metal layer on bottom side of TSI; and an organic substrate of 40 mm $\times$ 40 mm $\times$ 1 mm size and 0.8 mm thick core and with Sn-57Bi low melting point solder. The resulting warpage profile of the TSI assembly is shown in Figure 39, where it shows the Si-IP + Substrate (i.e., CoS-first) has the worst warpage and is the most challenge for the subsequent guest dies assembly onto this CoS stack. It also shows a significant increase of warpage when the CoC stack is assembly onto the substrate, although it is not as bad as the CoS-first approach. This study also concluded that by using low Tg and high CTE underfill for CoC assembly, and by using low melting temperature solder for the CoS assembly, the warpage can be minimized.

Several other methods have been proposed and demonstrated to have benefits of mitigating the 2.5D TSI assembly warpage issues. Examples are: using ceramic substrate,[85] using TCB for flip chip attach,[86] and using specially design pick up tool.[87] The effect of underfill and warpage on package stress and reliability is also been reported.[88–90]

D. Summary

The 2.5D TSI packaging is a highly integrated system. Although the basic building block is no difference than the traditional flip chip packaging, the multiple tiers of chip, solder, underfill, and substrate stacking and with miniaturization of all physical dimensions inside the package make the assembly of such package extremely challenging. Materials and processing integration alone can no longer satisfy the demand for successful assembly and reliability of the 2.5D

FIG. 38. Warpage related assembly issues: Bump shorted, bump non-connect, and underfill with air gap under the chip (Photo: Courtesy of Institute of Microelectronics).

FIG. 39. Comparison of warpage after bonding.[84] Reproduced with permission from Murayama *et al.*, "Warpage control of silicon interposer for 2.5D package application," in *Proceedings of the IEEE-Electronic Components & Technology Conference* (ECTC) (2013), p. 879. Copyright 2013 Institute of Electrical and Electronics Engineers.

FIG. 40. Cross section view of through Si interposer.
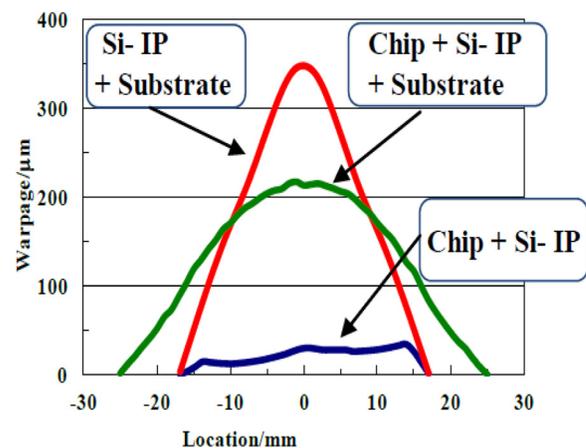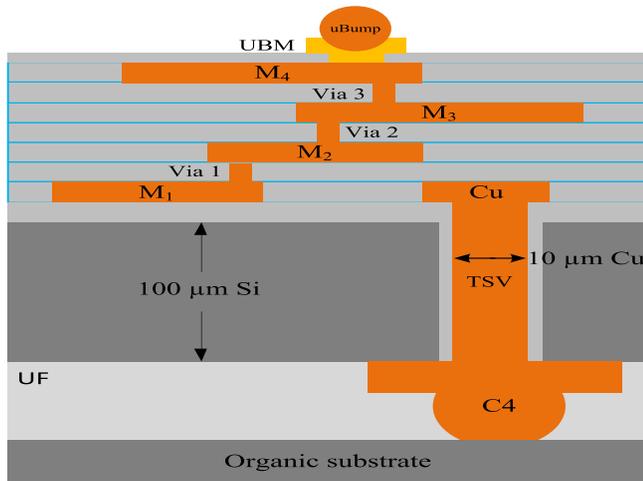
packaging. A new paradigm of packaging integration must start with the TSI design for low stress, low warpage TSI as the foundation for the 2.5D assembly, take into consideration of various process flow sequence and the impacts of interactions among the package materials, including the Si device, the substrate, and everything between them.

IV. 2.5D TSI TEST AND CHARACTERIZATION

Si verified 2.5D TSI PDK[91] is mandatory for the design engineers to achieve first time design success for their high speed/low power 2.5D TSI circuits and systems. At the core of Si verified 2.5D PDK lie a suite of test structures[92] aimed at characterizing the individual components and parasitic elements of 2.5D TSI technology. The objective of test structures is two-fold: (a) To provide an electrical data that can be used to verify electrical models to be incorporated into 2.5D TSI PDK and (b) to enable the debugging of 2.5D process development. This section illustrates various test structures aimed at characterizing individual 2.5D TSI components and parasitic elements followed by characterization results to be incorporated into Si verified PDK.

A. Test structures for 2.5D TSI electrical characterization

Cross-section of a typical passive Si interposer with 4 BEOL metals at the front sides fabricated with Cu-damascene process, and one thick backside RDL processed after TSV revealing followed by back side micro-bump attachment is illustrated in Figure 40. The key technology components and parasitic elements include front-side micro-bumps, front-side BEOL interconnects, TSVs, backside RDL, and back side micro-bumps. To characterize these components, the test structures (Figure 41) consist of: (a) Metal meander-folks for measuring sheet resistance and intra-layer capacitance of every metal layer, (b) four-port Kelvin structure for via and TSV/BEOL via resistance measurement, (c) Daisy chains to check connectivity between different levels of BEOL metals individually and collectively, (d) exclusive M1 – TSV – Back-side RDL – TSV – M1 daisy chains to characterize TSV resistance and debug

the TSV and back side reveal process, (e) exclusive M4 – front-side micro-bump – guest die M1 – front-side micro-bump – M4 daisy chains to characterize Front side micro-bump resistance ensuring the connectivity of guest die to the 2.5D TSI, (f) Exclusive back-side RDL – back-side micro-bump – substrate trace – back-side micro-bump – back-side RDL to characterize back-side micro-bump resistance and connectivity between 2.5D TSI and substrate, (g) parallel plate capacitances for measuring inter-metal capacitance, (h) embedded and de-embedded TSV banks for TSV and back-side micro-bump capacitance characterization, and (i) transmission lines to characterize time domain (eye diagram) and frequency domain (s-parameter) high-speed signal transmission responses across the interposer.

Parametric analyzer set-up is used for resistance measurements while LCR meter is employed for capacitance characterization. RF characterization is performed with network analyzer. With the help of standard resistance and capacitance models,[93] it is ensured that the measureable resistance of the test structure is $\gtrsim 1\ \Omega$ and capacitance is $\gtrsim 100$ fF unless it is a very a sensitive measurement of a single TSV through four-port Kelvin structure. Typical number of vias/front-side micro-bumps and back-side micro-bumps in a typical daisy chain is between ~90 and 1000 such that the same chains can be used for reliability assessment as well. Few characterization results are summarized in Sec. IV A 1 and IV A 2.

1. TSV characterization structures

To accurately characterize the TSV resistance, four-port Kelvin structure is commonly used to measure a single TSV as shown in Figure 41(b). Alternatively, a series of TSVs as a daisy-chain in Figure 41(c) is used as well. With interposer thickness of 100 μm, the TSV diameter is 10 μm (aspect ratio of 1:10). The measured TSV resistance is shown in Figure 42. Its mean value across three wafers is measured to be 23 mΩ matching well with the modeled TSV resistance 21.4 mΩ plus metal contact resistance between TSV and wafer metal layers. (The metal layers are in series with the TSV under test.)

Charge-Based-Capacitance-Measurement (CBCM)[94] is a possible solution for measuring single-TSV capacitance. However, such technique uses active circuits, which is not suitable for the passive interposer. TSV embedded and de-embedded structures illustrated in Figure 41(h) are used to characterize TSV capacitance as well as the back-side micro-bump capacitance. Measured TSV capacitance is subtracted from the TSV + back-side micro-bump capacitance and is normalized to obtain the back-side micro-bump capacitance which is estimated to be ~120 fF. Similarly, we measured de-embedded structure capacitance without any TSVs to capture the BEOL metal capacitance. It is subtracted from the embedded TSV capacitance and is normalized to extract the nominal TSV capacitance. C-V measurements performed at 10 kHz–1 Mhz, −40 to 40 V gate voltage on TSV-to-Si substrate capacitance structure using the thick Si substrate acting as an ohmic substrate contact are demonstrated in Figure 43. In this case, TSV behaves as a metal-oxide-semiconductor (MOS) capacitor
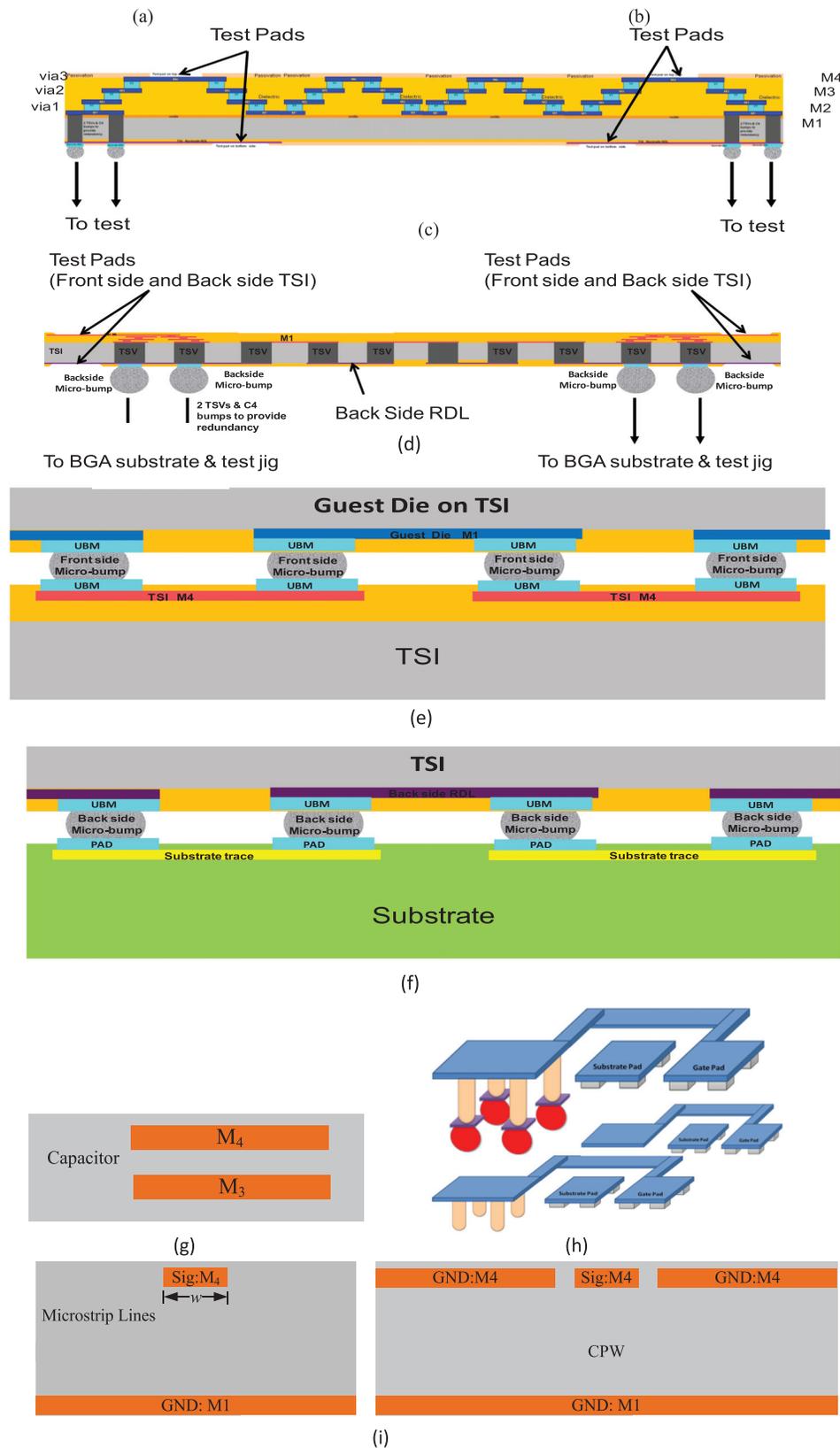
FIG. 41. TSI test structures: (a) meander fork structure, (b) four-port Kelvin structure for TSV/BEOL via resistance measurement, (c) Daisy chain for BEOL characterization, (d) exclusive daisy chain for TSV characterization, (e) exclusive daisy chain for Front-side micro-bump characterization, (f) exclusive daisy chain for Back-side micro-bump characterization, (g) parallel plate capacitor, (h) embedded and de-embedded TSV banks for TSV and C4 bump characterization, and (i) transmission line structure, micro strip (left) and CPW (right).

FIG. 42. Measurement results of TSV resistance.

TABLE IV. Extracted parameters of TSV in TSI.

	Physical specifications/estimations	
ϕ_{TSV} (μm)	12	Measured
L_{TSV} (μm)	100	Measured
C_{ox} (fF)	300	Measured
C_{TSV} (fF)(Ohmic Contact)	180	Measured
V_{th} (V)	−1	Measured
Average oxide liner thickness (nm)	420	Extracted
N_A (/cm^3)	8×10^{14}	Extracted
Q_f (/cm^2)	1.3×10^{11}	Extracted
D_{it} (/cm^2-eV)	4.12×10^{10}	Extracted
Q_m (/cm^2)	2.14×10^{10}	Extracted

demonstrating the accumulation, depletion, maximum depletion (high frequency $\sim$ 1 MHz) or inversion (low frequency $\sim$ 10 kHz) capacitance behavior as the voltage is swept between −tive and +tive gate voltages. The measured C-V curve along with the TSV analytical capacitance model[95] is used to extract key TSV parameters listed in Table IV. TSV FIB images confirm their dimensions as 12 μm outer diameter and 100 μm height. TSV oxide capacitance in the accumulation is measured to be 300 fF, while the capacitance in the maximum depletion region is 180 fF. Using TSV dimensions of diameter = 12 μm and height = 100 μm, the equivalent oxide liner thickness is extracted to be $\sim$420 nm. The measured negative threshold voltage = −1 V is attributed to the extracted higher fixed oxide charges $Q_f = 1.3 \times 10^{11}$/cm^2 and lower $D_{it} = 4.12 \times 10^{10}$ / cm^2-eV.

2. High density wiring characterization

Key aspects of the electrical models as described above are resistance, capacitance, and eye-diagram measurements. Meander-fork structures shown in Figure 41(a) are used to characterize interconnects' sheet resistance and intra-layer capacitance. For 1 μm thick M1 to M4 Cu lines having width = 2 μm and spacing = 2 μm, the measured sheet

resistance and intra-layer capacitance across 5 wafers are illustrated in Figures 44(a) and 44(b) accordingly. The mean sheet-resistance and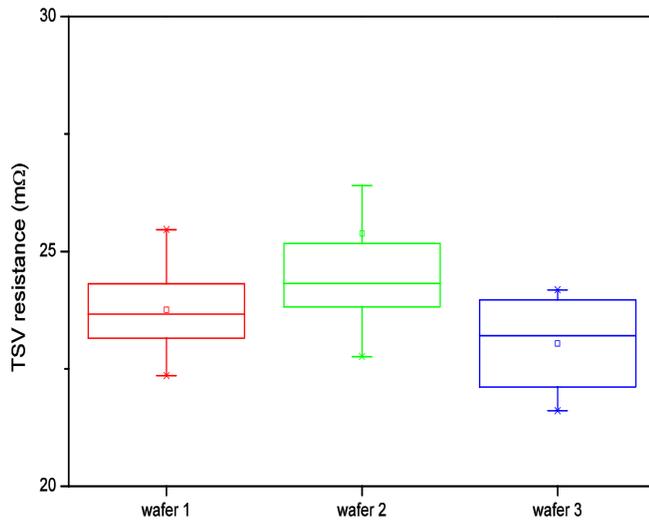 capacitance is 14.2 mΩ/$\square$ and 34.1 fF/mm, respectively. In our 2.5D TSI designs, we typically use 4–10 μm wide interconnects to achieve lower resistance and short "resistance-capacitance (RC)" delay. By using thicker copper traces, such as 3 μm RDL technology, one can achieve lower resistance of 5.7 mΩ/$\square$, which leads to higher data rate due to less parasitics. Large parallel-plate capacitors as shown in Figure 41(g) are used to characterize
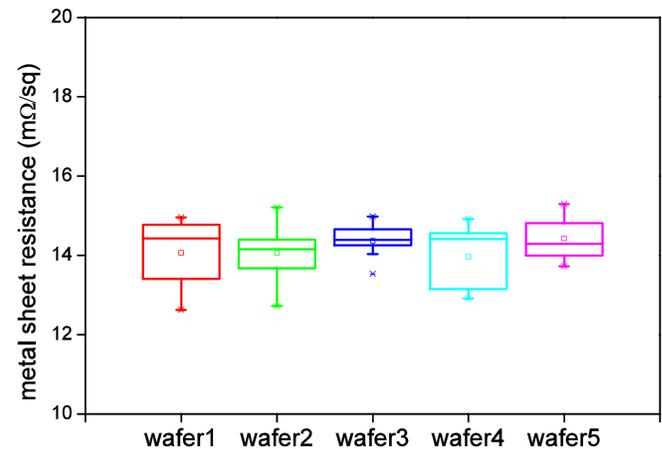
(a)
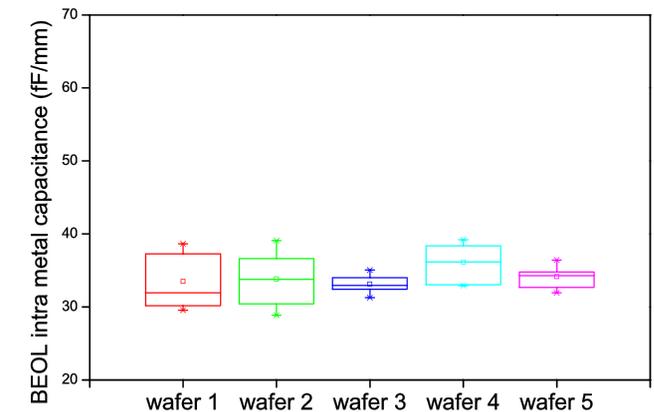
(b)

FIG. 44. Wafer-level (a) sheet resistance on M1/M2/M3/M4 and (b) intra-layer capacitance on M1/M2/M3/M4.

FIG. 43. Measured TSV capacitance result with different bias voltage and frequency.

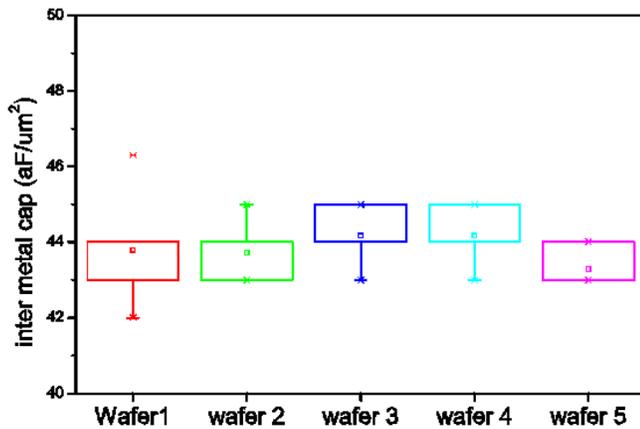FIG. 45. Inter-metal capacitance between M1-M2, M2-M3, and M3-M4.

inter-layer capacitances. Figure 45 demonstrates wafer-level capacitance characterization between M1 and M2 layers, its average value is 43.8 aF/um^2.

3. Chip-to-chip link characterization

Chip-to-chip connections on large size TSI $(40 \times 40 \, mm^2)$ can be as long as 10–25 mm, especially to host GPU and multiple HBM. At transmitted data rates ∼2 Gbps, long interconnects behave as RF transmission lines. To characterize transmission line properties on the interposers, micro-strip lines and grounded-coplanar waveguides (G-CPW) in Figure 41(i) are implemented. Although multiple segments of "RC" models can be connected in series to model long interconnects, this model is only valid for narrow band estimation and transmission line theory is more preferred to fully characterize the behavior at high frequency.[96] Interconnect physical cross-sections are designed for 50 Ω impedance match. For example, 50 Ω microstrip width of M4 layer is 10 μm for the quasi-TEM mode propagation if M1 layer is assumed as an infinite ground plane. If a 50 Ω microstrip lines is implemented in M2 or M3, the widths can be narrower compared to M4 microstrip line due to large parasitic capacitance. Furthermore, narrow width traces incur higher conductor loss, which degrades signal integrity. Their insertion lose (S$_{21}$) for interconnect lengths are simulated and experimentally verified via S-parameter measurement using the Vector Network Analyzer (VNA). The accepted frequency bandwidth for interconnects is generally limited by 3 dB insertion loss.[97,98]

In 2.5D TSIs, there are mainly two categories of connections: (a) on-TSI connections which link I/O pads of one chip on TSI to another chip's I/O pads on the same TSI and (b) off-TSI which link I/O pads of chips on TSI to the external world (organic substrate/PCB) via TSVs. For the on-TSI connections with length over 25 mm, eye diagrams are measured with data rate of 2 Gbps. As seen in Figures 46(a) and 46(b), the signal integrity of RDL interconnect outperforms the BEOL interconnect due to lesser resistance and capacitance. The length and spacing (L/S) for BEOL interconnect here is 2 μm, its thickness is 1 μm, and L/S for backside RDL interconnect is 3 μm, and its thickness is 3 μm.

TSV-back side RDL-TSV interconnect as shown in Figure 47(a) is analyzed for s-parameters using G-S-G structure illustrated in Figure 41(i). The S-parameter results characterized up to 40 GHz are shown in Figure 47(b). Return loss is well below 12 dB for frequency below 40 GHz indicating acceptable return loss. The single off-TSI insertion loss is half of overall TSV-backside RDL-TSV transition. Therefore, the single off-TSI interconnect insertion loss is <2.5 dB up to 40 GHz. Besides the on-TSI interconnects, there are off-TSI interconnects through TSVs and backside micro-bumps. Figure 48 shows the measured eye diagram for 25 Gbps data rate between front side of interposer and the backside interposer. The eye opening demonstrates that circuits, such as serializer/deserializer (SerDes), can be designed using the 2.5D TSI platform.

4. Micro joint reliability characterization

The reliability assessment of the micro-bump joints interconnecting the guest die and the TSI, as well as the backside micro-bump interconnecting the TSI on the substrate is critical to steer the technology mainstream. A daisy chain interlacing between the top metal of the TSI (M4) – to – front side micro-bump – to – top metal in the Guest die as shown in Figure 41(e) is an ideal structure of choice to perform the reliability assessment on micro-bump joints. Daisy chains with varying number of micro-bumps are constructed and evaluated for temperature-cycling (∼1000 cycles) as described in JEDEC standard. Similar daisy chains between the TSI and substrate shown in Figure 41(f) interlacing the back side Cu-RDL – to – backside micro-bump – to – substrate trace are constructed and characterized to evaluate the reliability of the backside micro-bump. In technologies in which the backside RDL is not provided, the daisy chain
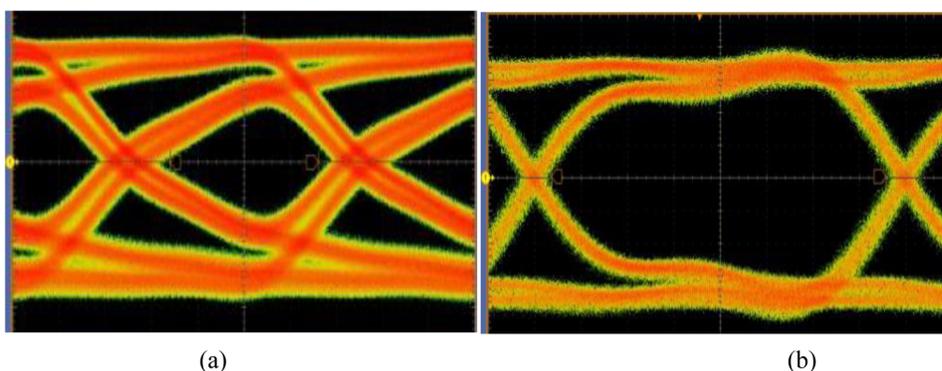

FIG. 46. Eye diagrams of 2 Gbps for 25 mm long (a) BEOL interconnect thickness 1 μm, width 2 μm, and pitch 4 μm and (b) RDL interconnect thickness 3 μm, width 3 μm, and pitch 6 μm.
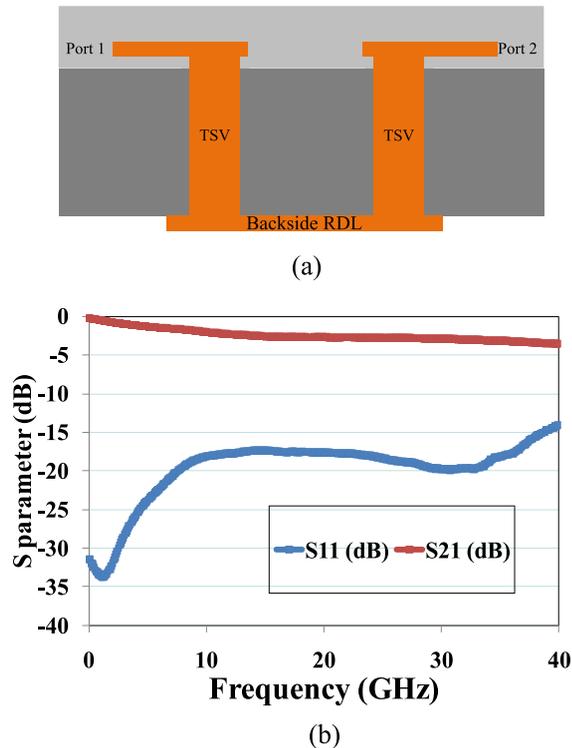
(a)

(b)

(a)

(b)

FIG. 47. (a) DUT and (b) S parameter characterization of TSV-back side RDL-TSV interconnect.

would interlace from M1 – to – TSV – to –backside micro-bump – to – PCB. It can be probed from PCB pads.

5. Decoupling capacitors

Clean power source is required for the ICs on 2.5D interposer.[99] Voltage noise in power/ground planes disturbs the data in latch, logic error, data drop and false switching, and furthermore coupling to signals. Power fluctuation on power distribution network (PDN) must be kept in the allowable range. For example, the maximum allowable voltage deviation in FPGA core power and I/O buffers is typically <5%. Dedicated planes for power and ground are preferred compared to the power/ground grid.[100] The decoupling capacitors temporarily store and provide the electrical charges when currents drawn by ICs fluctuate. Together with
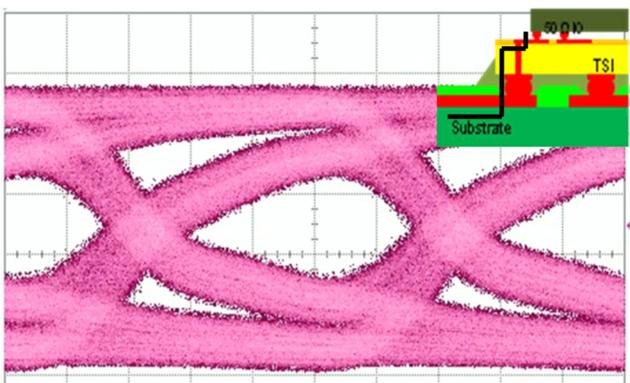
FIG. 48. Eye diagram of 25 Gbps for the off-TSI interconnect: M1-TSV-C4 bump.

equivalent series inductance of PDN, decoupling capacitors function as a low-pass filter to suppress high frequency voltage fluctuation, and thus reduce the voltage noise contributed from the simultaneous transistor switching. As shown in Figure 49,[101] the package impedance Z around 100 MHz is reduced due to 2.2 nF capacitor integrated on interposer. Broad-level decoupling is often implemented with high quality ceramic capacitors range from 1 μF to 10 μF. Those de-coupling capacitors need to be placed close to the targeted chips for optimal de-coupling effect. Die-level integrated high-density metal-insulator-metal (MIM) based on integrated passive device (IPD) technology on TSI are more effective than the package-level counterparts due to smaller equivalent series inductance (ESL). In Ref. 101, Altera demonstrated using on-TSI MIM capacitance in its 10 Gpbs SerDes as shown in Figure 49. With the use of MIM capacitors the package impedance drops (indicating low impedance between power and ground). The improvements in the performance of transmitter jitter, eye height, and width were quite significant, as listed in Table V. The transmitter jitter, eye height, and width are improved by 10%, 20%, and 7.7%, respectively.

V. THERMAL CONSIDERATIONS OF 2.5D PACKAGES

A. Thermal challenges in the context of 2.5D package

Next generation of heterogeneous integration demands for 2.5D and 3D chips in one package for less signal latency, more functionality, and less power consumption. Nonetheless, there are tremendous obstacles in realizing the real 3D based vertical architecture with regards to fabrication and thermal management. Therefore, 2.5D package on TSI has been envisioned as the most viable strategy in the context of heterogeneous integration. In a typical 2.5D package, dissimilar chips such as logic, memory, and ASIC chips, as well as optical components such as laser diode and optical transceivers, can be assembled on an interposer. Wafer level packaging facilitates the manufacturability of the interconnection of multiple chips on the interposer.
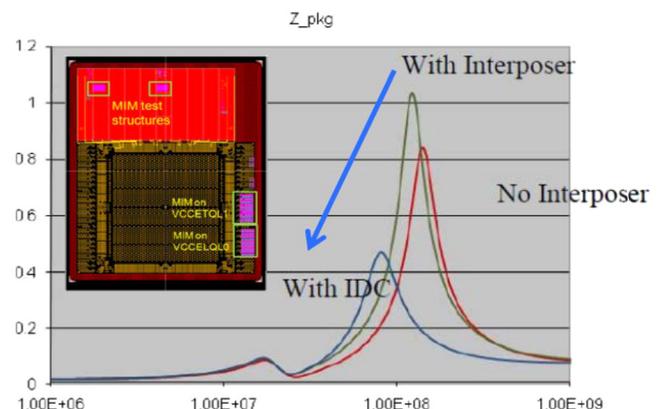
FIG. 49. Effect of decoupling capacitor for 2.5D IC power planes.[101] Reproduced with permission from Zhe *et al.*, "Development of an optimized power delivery system for 3D IC integration with TSV silicon interposer," in *Proceedings of IEEE Electronic Components and Technology Conference (ECTC)* (2012), pp. 678–682. Copyright 2012 Institute of Electrical and Electronics Engineers.

TABLE V. Improvement in transmission Jitter, eye height and eye width due to the use of 2.2 nF MIM CAP for 10 G SerDes.[101] Reproduced with permission from Zhe *et al.*, "Development of an optimized power delivery system for 3D IC integration with TSV silicon interposer," in *Proceedings of IEEE Electronic Components and Technology Conference (ECTC)* (2012), pp. 678–682. Copyright 2012 Institute of Electrical and Electronics Engineers.

	MIM (cap)	RJ (rms) (ps)	DJ (ps)	TJ (ps)	Eye height (mV)	Eye width (ps)
10 G SerDes	2.2 nF	0.76	25.1	35.93	619	70
	None	0.77	28.16	39.2	512	65

The thermal management issues can be understood from two aspects. On one hand, the chip-level power delivery could reach significant levels up to 100 W/cm^2 for high processing chips, which require proximate cooling. Without compromising processing speed, the integration of multi-chips in one interposer on the package tends to generate higher heat density, which needs to be addressed in the 2.5D or 3D package design.[102–115] A schematic of the cooling concepts is illustrated in Figure 50.

On the other hand, the temperature sensitive chips, such as optical chips, are more prone to wavelength shifts due to the temperature excursions, therefore requiring temperature control.[116] While the additional interposer may help to even out the hot spots, it may also introduce thermal cross-talk between chips requiring different operation temperature. To mitigate against thermal cross-talk, thermal management techniques, such as guide ring/heaters or thermoelectric cooling, can be implemented to avoid transmission bit error.[117–120]

In the past decade, substantial efforts have been made to address the thermal management issues and challenges, including passive cooling characterization, thermal enhancement due to Si carriers, thermal enhancement with liquid cooled cold plate, or even microchannel heat sinks built on the backside of chips. The cooling of 3D stacked packages with on chips on Si carriers is studied in Ref. 105. It was identified that, due to package limitation, only 1 W could be dissipated from the two chips stacked on their chip carriers through microbump joining. Due to insufficient passive cooling capacity downward through the PCB, additional cold plate was used to spread the heat from the top of the stack. It is identified that 20 W can be dissipated through the chip carrier, with maximum temperature rise of 48.9 °C. A direct liquid cooling of three stacked chips on Si carriers is presented in Ref. 106, which shows that direct liquid cooling can dissipate 23 W from the chip carriers based on dielectric fluid. Recent research is conducted on the thermal management of two stacked chips on Si carriers cooled by microchannel heat sinks fabricated in the chip carriers.[107,108] A heat flux of 100 W/cm^2 can be dissipated from each chip stack through dual in-port fluidic design.

With more attention paid to the 2.5D package with heterogeneous integration, research work has been conducted on the effect of Si interposer on the thermal performance of the package.[99–102] A comprehensive thermal characterization is conducted on the TSI package with bare-die and overmolded packages.[112] The measured thermal resistance (Theta JA) is 35 K/W under natural convection. When the liquid-cooled cold plate is applied, the thermal resistance drops to 0.82 K/W from the same chip, validating the cold plate's efficiency in removing heat from the 2.5D package. The respective cooling performance will be discussed in Secs. V B–V D.

B. Passive cooling

Passive cooling is defined here as the cooling techniques that do not use any active fluid movers such as pumps and cooling fans. Conventionally, thermally enhanced PCB, lid encapsulation are used as passive cooling techniques. 2.5D package normally consists of several chips on Si or glass interposer with TSVs for electrical interconnections. Compared with conventional package, the 2.5D package has different thermal behavior since interposer with through vias serves as heat spreader for heat dissipation in the absence of active cooling apparatus such as axial fans. Thermal characterization can be conducted under still air condition to extract thermal metrics such as Theta JA or Theta JB. The passive cooling is especially useful in space-tight and energy-limiting applications, e.g., tablets and smart phones. The thermal performances with different design factors for the interposer and TSVs are outlined in Secs. V B 1–V B 4.

1. TSV thermal enhancement

A forest of TSV will have an impact on the interposer thermal performance. The approach for extracting the equivalent thermal conductivity is shown in Figure 51 for modeling of equivalent thermal conductivities of TSV interposer along the through plane z direction and in-plane x and y directions.[109] First, create the geometry of TSV interposer with different TSV design parameters, then set the boundary conditions and simulate the temperature distribution. After obtaining the temperature distribution, the equivalent thermal conductivity can be calculated. The average temperature
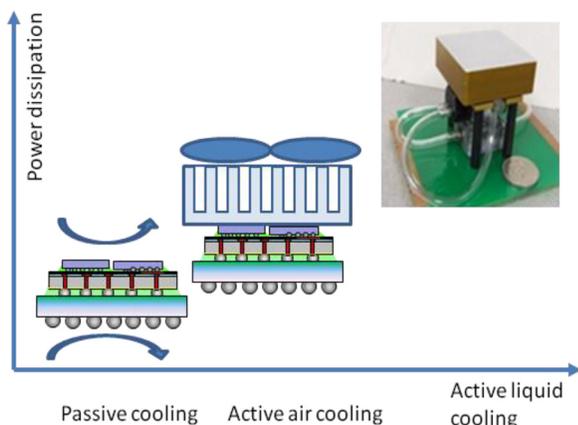

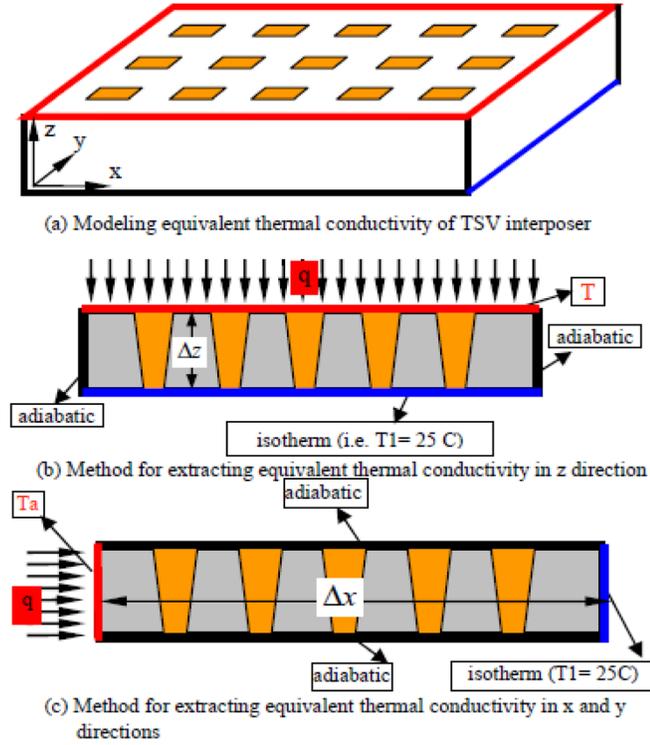FIG. 50. Schematic of the cooling concepts.

FIG. 51. Equivalent thermal conductivity extraction models for TSV interposer: (a) Modeling equivalent thermal conductivity of TSV interposer, (b) method for extracting equivalent thermal conductivity in z direction, and (c) method for extracting equivalent thermal conductivity in x and y directions.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

on the top surface is obtained, and consequently, the equivalent thermal conductivity can be calculated as follows:

$$q = -k_{eq,z}\frac{\Delta T}{\Delta z}, \tag{5.1}$$

$$k_{eq,z} = -q\left(\frac{\Delta z}{\Delta T}\right), \tag{5.2}$$

$$q = -k_{eq,x}\frac{\Delta T}{\Delta x}, \tag{5.3}$$

$$k_{eq,x} = -q\left(\frac{\Delta x}{\Delta T}\right). \tag{5.4}$$

The geometrical dimensions and thermal properties used for detailed modeling are listed in Table VI.

TABLE VI. TSV interposer parameters and thermal properties.

Component	Interposer	TSV
Material	Silicon	Copper
Thermal conductivity (W/mK)	150	390
TSV pitch (mm)	0.15–0.6	
TSV via ratio	2–10	
TSV cu plating thickness (urn)	5–25	
TSV filler material	No filler, polymer based. Aluminum, Copper	

a. Equivalent thermal conductivity with Cu filled TSVs. Figure 52 shows five different TSVs with various aspect ratios A, which A is defined as A = Thickness/Average diameter of TSV. The thickness of the wafer is 300 μm, and the etching angle of the tapered Cu-filled TSV is 85°. Figures 53–55 show that the equivalent thermal conductivity of the TSV interposer varies with TSV aspect ratios and pitches for equivalent thermal conductivity in the normal z-direction, keq,z, and equivalent thermal conductivity in the planar directions (x and y directions), keq,x = keq,y, respectively. It can be seen that for a fixed pitch, the equivalent thermal conductivity of Cu-filled TSV interposer increases when the aspect ratio decreases, which is especially sensitive when the aspect ratio is small—ranging from 2 to 4, and the equivalent thermal conductivity in all directions is greater for larger diameters of the TSV. For engineering convenience, the results have been curve-fitted into the following empirical equations for the equivalent thermal conductivity:

$$k_{eq,z} = 150 + 188D^2P^{-2}, \tag{5.5a}$$

$$k_{eq,x} = k_{eq,y} = 150 + 105D^2P^{-2}. \tag{5.5b}$$

b. Equivalent thermal conductivity with TSVs filled with varying materials. Figure 56 shows the TSV plated with thin layer of copper. Figures 57 and 58 show the variation of equivalent thermal conductivity of TSV interposer with the partially plated copper thickness for different TSV pitch, respectively, in the normal direction (z-direction) and in the planar directions (x and y-direction). It can be seen that equivalent thermal conductivities of the TSV interposer increase with the plating thickness. In addition, the equivalent thermal conductivities of the TSV interposer are more sensitive to the copper plating thickness for smaller pitches of vias. For example, in the case of 0.15 mm TSV pitch, the equivalent thermal conductivity in the z-direction increases
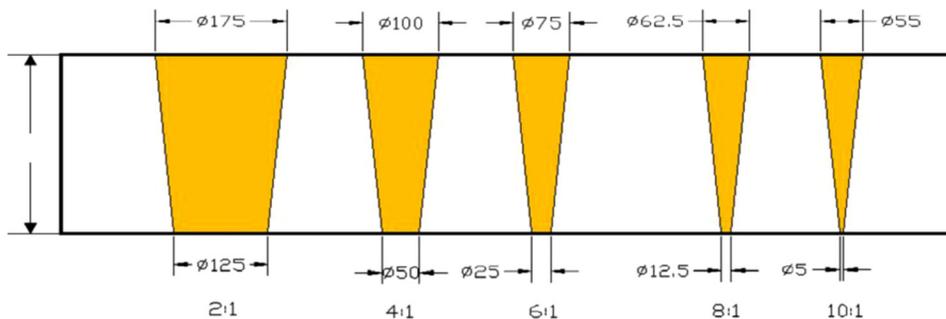

FIG. 52. TSV geometry for different aspect ratios.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

$$k_{eq,z} = 150 + 188D^2P^{-2}; \quad D = (D1 + D2)/2; \quad A = Thickness/D$$

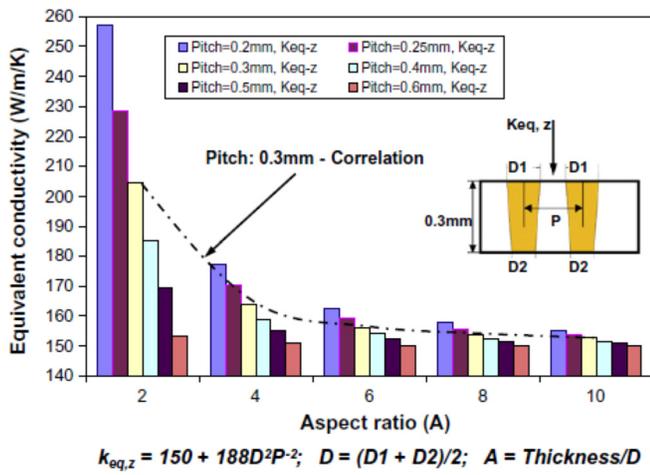FIG. 53. Equivalent thermal conductivity in normal z-direction (keq,z).[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

FIG. 55. Equivalent thermal conductivity of TSV interposer with different TSV pitches.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

from 138 W/mK to 187 W/mK (~40%) if the Cu plating thickness is increased from 5 μm to 25 μm. For the simulated interposer with a fixed size of 25 mm × 25 mm, the finer the pitch, and hence, more TSVs incorporated in the interposer, results in more air or copper material and less silicon material in the interposer and thus a greater influence of the air or copper on the equivalent thermal conductivity. As to the case of 5 μm Cu thickness, smaller via pitch with smaller copper thickness results in more TSVs with more air, but less copper and silicon material. The incorporated more air vias account for the lowest thermal conductivity. By increasing the thickness of copper, more copper can be incorporated due to more TSVs included in the interposer, which suggesting better thermal conduction can be enabled. This is also the reason why TSV interposer with smaller pitch is more sensitive to the copper plating thickness.

2. Effect of TSV interposer on package thermal performance

Figure 59 shows the compact modeling of the 3D SiP with the TSVs in interposer using a compact block with the pre-determined equivalent thermal conductivities. This model consists of a heat generating chip, a TSV interposer, a BGA build-up substrate, a PCB, and the solder joints. Their dimensions and thermal properties are listed in Table VII.

The junction to ambient thermal resistance of the package (R_{ja}) can be expressed as $R_{ja} = (T_j - T_a)/P$, where T_j and T_a represent the junction temperature and ambient temperature, respectively, while P refers to the total power dissipated from the chip.

Figure 60 shows the junction to ambient thermal resistance of packages with different chip power dissipations. It can be seen that: (1) the thermal resistance reduces as the chip power increases (this is because high chip power induces high package temperature, as such high heat transfer coefficient is induced and more heat is removed from the package), and (2) the thermal resistance of the TSV package is lower than that of the package without TSV (this is because of the TSV interposer's spreading effect). The dashed lines in Figure 60 represent the correlations between the thermal resistance and chip power when the junction temperature equals to 85 °C and 125 °C, respectively.[109]

Figure 61 shows the effect of the TSV interposer area on the resistance (R_{ja}) decreases about 14% when the TSV interposer size increases from 21 mm × 21 mm to 45 mm × 45 mm. This indicates that package thermal performance can be improved by increasing the TSV interposer size.

Figure 62 shows the effect of the TSV interposer thickness on the package thermal performance. It can be seen that the thicker the TSV interposer the lower the thermal resistance. This is because of the increasing spreading effect with thicker interposer/ chip. However, for small size interposers, this effect is negligible.

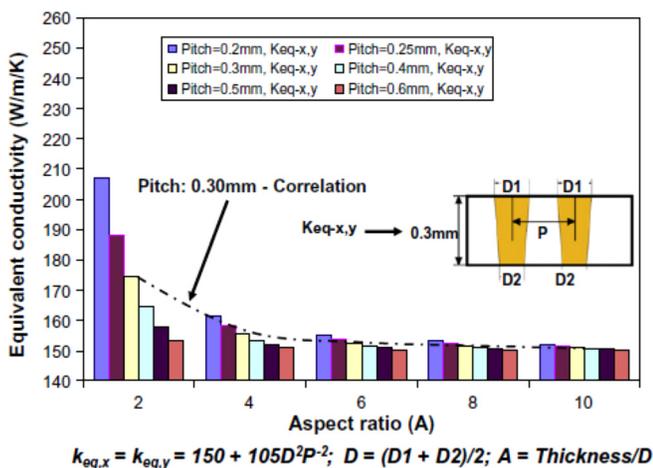$$k_{eq,x} = k_{eq,y} = 150 + 105D^2P^{-2}; \quad D = (D1 + D2)/2; \quad A = Thickness/D$$

FIG. 54. Equivalent thermal conductivity in normal x,y-direction (keq,x) and (keq,y).[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

FIG. 56. Geometry for partially filled TSV.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

FIG. 57. Equivalent thermal conductivity Keq,z for partially filled TSV.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.
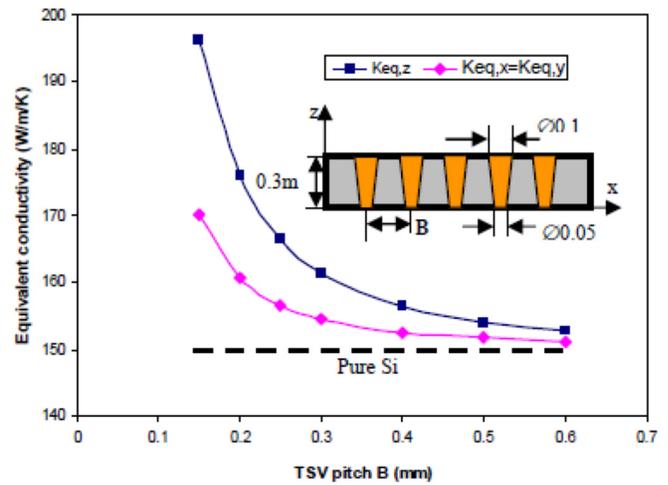
Figure 63 shows the effect of the chip size for different size ratios of the TSV interposer to the chip on the thermal performance of the package. It can be seen that for the same chip to TSV interposer size ratio (b/a), the smaller sizes of chips induce higher thermal resistance of the package.

3. Thermal characterization of stacked chips

The thermal characterization for 2.5D/3D packages with TSVs can be conducted under natural convection condition. A schematic of the 3D stack package developed is shown in Figure 64. The 3D package overall dimensions are $13.5 \, mm \times 13.5 \, mm \times 1.4 \, mm$, having 276 peripheral I/Os. Carrier 1 is designed to mount a flip-chip (chip 1) representing an ASIC device. The chip 1 dimensions are $8.5 \, mm \times 8.5 \, mm \times 0.1 \, mm$ with 1000 I/Os at a bump pitch of 0.25 mm. Carrier 2 is designed to mount two memory chips, chip 2 and chip 3, each having overall dimensions of $4.5 \, mm \times 9.0 \, mm \times 0.1 \, mm$ and 80 I/Os. The two Si carriers were stacked one over other using 8 mil solder balls. Electrical connections through the Si carrier were formed by TSV technology. Some of the advantages of using Si for the interposer are low thermo-mechanical stress, fine line width and spacing, wafer level batch fabrication, and high thermal conductivity.

Thermal characterization requires a test die with heater and temperature sensor. It was difficult to procure test die similar to the die dimensions used in this study. We used a

FIG. 58. Equivalent thermal conductivity Keq,x (=Keq,y) for partially filled TSV.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.
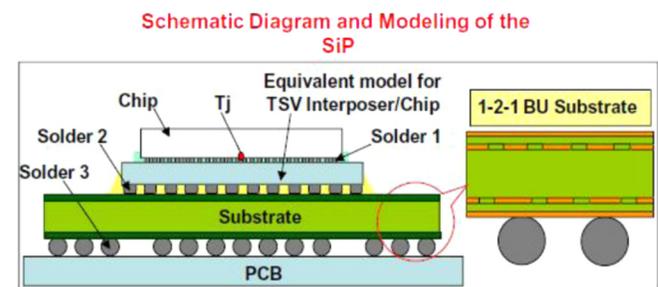
FIG. 59. Schematic diagram and modeling of SiP.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

TABLE VII. Geometry details and material properties for the package.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

Component	Material	Thermal conductivity (W/m/C)	Dimension (mm)
Chip	Si	150	$21 \times 21 \times 0.75$
Solder 1	SnAg	57	Pitch: 0.15
			Height: 0.08
			Aver D: 0.08
Interposer	S_4 + TSV (Cu)	Keq	Variable
Solder 2	SnAg	57	Pitch: 0.5
			Height: 0.1
			Aver D: 0.1
Substrate	Ituikhip	//100 ⊥ 0.5	1-2-1 ($45 \times 45 \times 1$)
Solder 2	SaAg	57	Pitch: 1.0
			Height: 0.6
			Aver D: 0.6
PCB	FR4	//0.8 ⊥ 0.3	$101 \times 114 \times 1.6$

FIG. 62. Junction to ambient thermal resistance for different TSV interposer thickness.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.
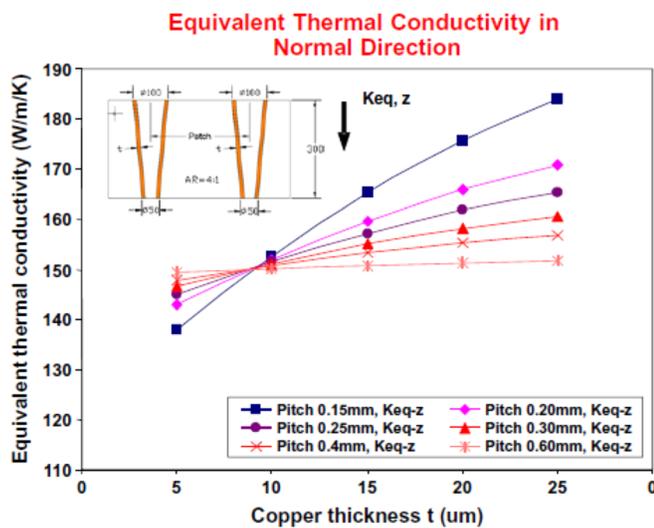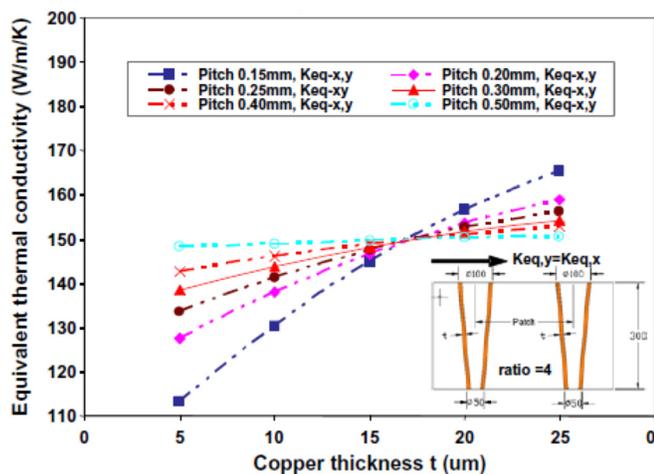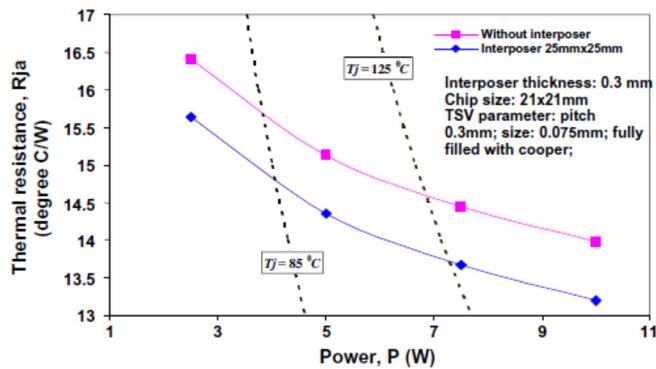

FIG. 60. Junction to ambient thermal resistance for different power dissipations.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

FIG. 63. Junction to ambient thermal resistance for different TSV sizes at different chip sizes.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

FIG. 61. Junction to ambient thermal resistance for different TSV interposer size.[109] Reproduced with permission from Hoe *et al.*, "Effect of TSV interposer on the thermal performance of FCBGA package," in 11th IEEE Electronics Packaging Technology Conference (EPTC) (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.
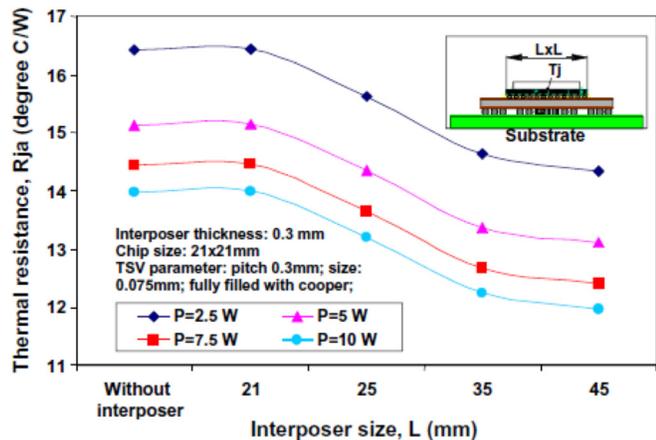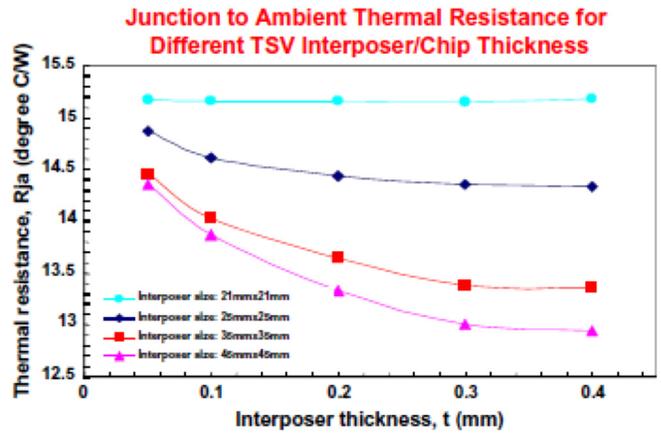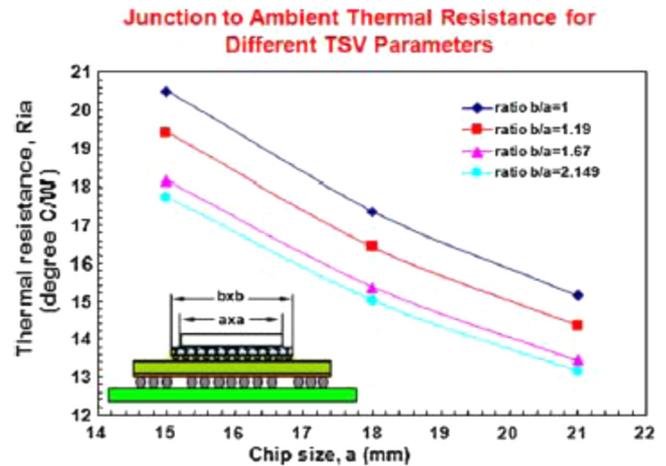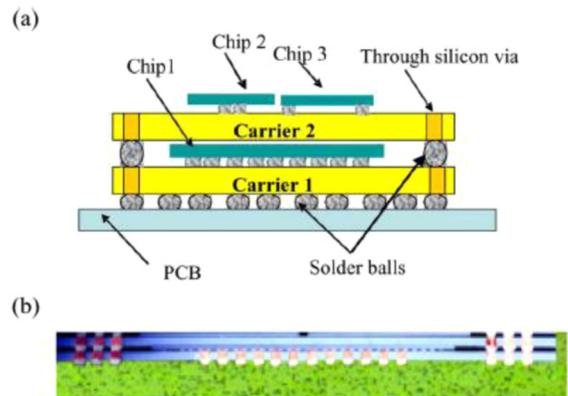

FIG. 64. (a) Schematic of 3D stack package and (b) cross section of 3D stack package.
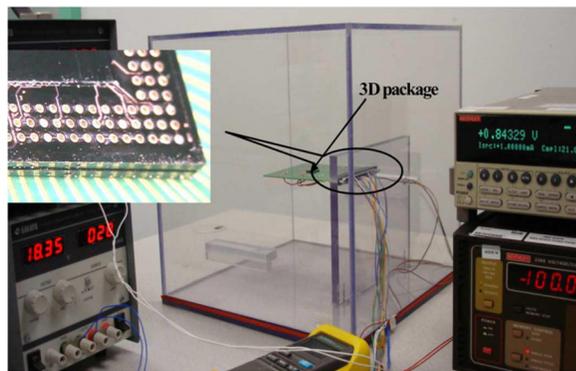
FIG. 65. Experimental characterization of thermal resistance under natural convection condition.

FIG. 66. The schematic of the multi chip module on through Si interposer, with TV1 behind TV3. The SEM image of TSV under thermal chip bumps is also shown. (Unit: mm).[112] Reproduced with permission from Zhang *et al.*, "Thermal characterization and simulation study of 2.5D packages with multi-chip module on through silicon interposer," in 15th IEEE Electronics Packaging Technology Conference (EPTC) (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

test die available in our laboratory, which has dimensions of 8.9 mm. The test die was thinned to 100 μm. Each carrier was assembled with test die. The two carriers were stacked one over another using SnPb eutectic solder balls. The 3D package was assembled onto a four-layer test board. Figure 65 shows the assembled board mounted horizontally inside an enclosed chamber for natural convection thermal characterization as defined in JESD-51 standards.[121,122] The test chips in carrier 1 and carrier 2 were connected to a separate power source and supplied with 0.8 W and 0.2 W, respectively. Four such packages were characterized, and the average of maximum temperature chip 1 is compared. The maximum temperature increase of chip 1 was 24.2 °C, with calculated thermal resistance of 30.3 K/W based on 0.8 W power input.

Two types of thermal enhancements techniques were studied, i.e., through thermal via and thermal bridging using polymer adhesive. Thermal analysis was carried out with a heat load of 2.8 W in chip 1 and 0.1 W each in chip 2 and chip 3, respectively. First, the package thermal performance was studied with 144 thermal vias in the carrier 1. Maximum temperature of chip 1 with thermal via is 77.5 °C as compared to 78.5 °C without thermal vias. Si has good thermal conductivity, therefore, thermal via in the Si carrier is not effective in reducing the package thermal resistance. Another thermal enhancement was done by bridging the gap between chip 1 and carrier 2 using thermal adhesive. A polymer adhesive having thermal conductivity of 2 W/mK was used to bridge the chip 1 and carrier 2. The maximum temperature of chip 1 with thermal adhesive is found to be 73.9 °C. The thermal resistance is calculated to be 17.5 K/W. It is seen that the thermal bridging helps to reduce the thermal resistance by 42% for the chip 1 through the upward thermal path on the carrier 2 by forming a parallel heat flow path. Further improvement may include the heat spreader and cold plate at the top, which however can be categorized into the active cooling technology. It has been shown by thermal simulation that 20 W could be dissipated from chip 1 through the top cold plate cooling method.

4. Thermal characterization of 2.5D package

A thorough thermal characterization of the 2.5D package is done in Ref. 112. The thermal resistance of Theta JA,
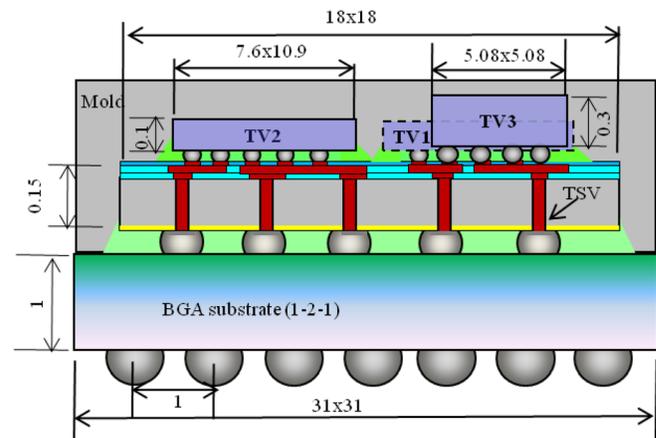
Theta JB, and Theta JC are characterized and compared with the thermal simulation. The concept of the package structure is shown in Figure 66 and the actual packages, both molded and bare die types, are shown in Figure 67. The thermal test die with a size of 5.08 mm × 5.08 mm is laid out on the Si interposer, together with two dummy dies with sizes of 7.6 mm × 10.9 mm, 8 mm × 8 mm. All the dies are fabricated and assembled on the same interposer wafer through microbumps and underfill processes. The two dummy dies represent the logic and memory chips in a typical TSI integration. The interposer wafer was fabricated through processes including TSV, copper filling, and top-side RDL processes on 12 in. wafer to form micro straight vias of 10 μm in diameter and 100 μm deep through the interposer. The interposer of 18 mm × 18 mm × 0.1 mm in size was then assembled
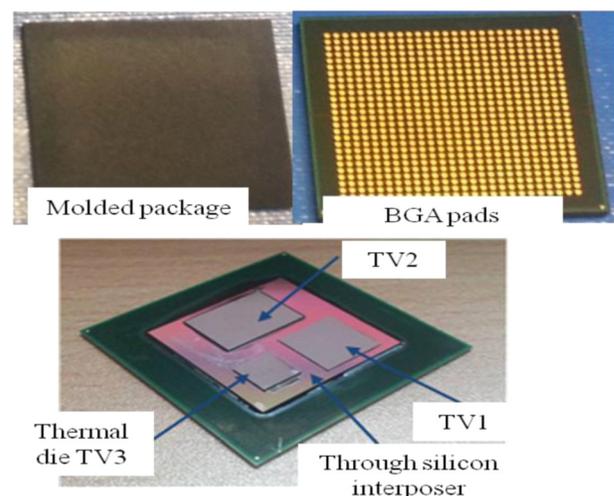
FIG. 67. The molded and bare die TSI package in 26 × 26 BGA format.[112] Reproduced with permission from Zhang *et al.*, "Thermal characterization and simulation study of 2.5D packages with multi-chip module on through silicon interposer," in 15th IEEE Electronics Packaging Technology Conference (EPTC) (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

onto the organic substrate of 31 mm × 31 mm × 1 mm. For the molded packages, additional molding process is conducted on the wafer level to form the epoxy molded encapsulation on the chip package. The molding layer helps protect the die from damage such as mechanical shock. The wafer is then diced into the package size. After the BGA solder ball attach process, the package is assembled on the thermal test board for electrical connections.

For Theta JA test, the test board is arranged in the one feet cubic chamber conforming to the JEDEC standard.[121] The corresponding junction to ambient thermal resistances is plotted in Figure 68 as against the power input.

In Theta JA and Theta JB measurements and corresponding thermal simulation that will be discussed in the later paragraph, the molded packages give consistently lower thermal resistances than the bare die packages. This can be attributed to the enhanced thermal radiation effect due to the molding compound with the surface emissivity ∼0.9, which is larger than that of Si surfaces in the range of 0.1 for the bare die package. Molding on the substrate also assists the heat to be conducted away from the die to the substrate. The thermal models are constructed for the molded packages and the results are compared in Figure 69. Thermal radiation effect is considered in the Theta JA thermal simulation.

The validated thermal model can also be used to predict the maximum power dissipation from the simultaneous heating of TV1 and TV2 dies under passive cooling condition. This can be achieved by assigning power dissipations of 1 W and 2 W on the two dies while keeping the thermal die power to be zero. The interaction of the multi chip heating on the 1s0p thermal board under natural convection condition can be expressed in the linear superposition form, namely,

$$\begin{bmatrix} \Delta T_{j1} \\ \Delta T_{j2} \end{bmatrix} = \begin{bmatrix} A11 & A12 \\ A21 & A22 \end{bmatrix} \begin{bmatrix} P1 \\ P2 \end{bmatrix} = \begin{bmatrix} 33.0 & 19.0 \\ 22.2 & 28.9 \end{bmatrix} \begin{bmatrix} P1 \\ P2 \end{bmatrix}, \quad (5.6)$$

where ΔT_{j1} and ΔT_{j2} are the junction temperature rises in °C, A_{11}, A_{12}, A_{21}, and A_{22} are the influence factors in °C/W
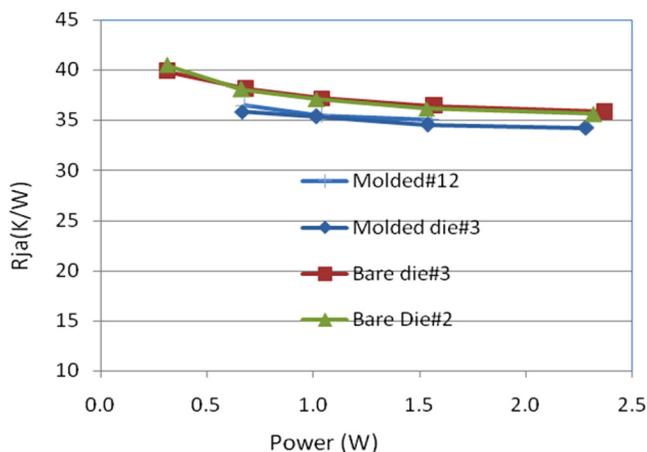
FIG. 68. Measured Theta JA test jig under natural convection condition for both molded and bare die package.[112] Reproduced with permission from Zhang *et al.*, "Thermal characterization and simulation study of 2.5D packages with multi-chip module on through silicon interposer," in 15th IEEE Electronics Packaging Technology Conference (EPTC) (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.
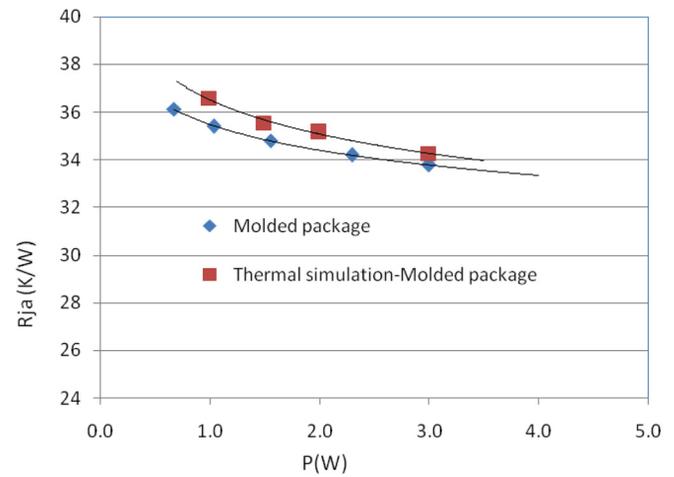
FIG. 69. Comparison of averaged simulation results versus measurements for the junction to ambient thermal resistances under natural convection condition.[112] Reproduced with permission from Zhang *et al.*, "Thermal characterization and simulation study of 2.5D packages with multi-chip module on through silicon interposer," in 15th IEEE Electronics Packaging Technology Conference (EPTC) (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

due to the power dissipations P1 and P2 in Watts for TV1 and TV2, respectively. With the above equation, the present package format could dissipate 2.3 W at the temperature rise of ΔT_{j1}, $\Delta T_{j2} \sim 60\,°C$. To improve the power dissipation without heat sink on top, an immediate method is to use a thermally enhanced 4 layer PCB (2s2p). The computed power dissipation from a 4 L PCB is correlated with the linear superposition approach through thermal simulation. The power dissipation with the two chips on TSI package can go up to 3.5 W with the same temperature window of 60 °C.

C. Active cooling

1. Active air cooling

Typical active cooling involves either fan cooled air cooling or pump-driven liquid cooling technology. Fan cooled air technology assembled with heat sink is commonly used to manage the heat dissipation of high power chips such as processors and graphic chips. Such combination is able to remove heat in the range of 50 W/cm^2. Enhanced air cooling technique such as vapor chamber based heat sink can be utilized to minimize the heat spreading resistance from the small chips to the large heat sink base. For a 3D package, due to the interlayer thermal resistance, the cooling capacity for the stacked chips is limited. Additional thermal resistance is found for the bottom chip, which is mostly a logic die. A study on the shaped lid for cooling of memory dies stacked on logic die showed that the junction to casing thermal resistance is almost doubled with the use of heat sink at top,[113] which may limit the performance of the logic die. On the other hand, inter layer cooling seems to be the only way to follow trend of the 3D high power integration.

2. Liquid cooling

Liquid cooling has a much higher heat transport capability than air cooling. Efforts have been dedicated to develop

liquid cooling in the last decade from flip-chip packages to 3D packages. Chen *et al.* conducted the direct cooling with dielectric fluid such as FC-72 for the direct cooling of stacked MCM as shown in Figure 70.[106] Using minimum flow clearances and maximum flowrate of 25 g/s, the maximum temperature reduces to 31 °C for total power input of 6 W, which is equivalent to a total power input of 23 W if the maximum temperature is increased to 56 °C under the single phase cooling regime. Further experimental work was conducted and more than 40 W power can be dissipated from the 3D stack to maintain the junction temperature below 85 °C.

Integration of interlayer cooling on 3D package has received increasing interests. The technology challenges mainly lie in the design and implementation of electrical TSVs, thermal TSVs, fluidic TSVs, or any permutations of the three. As a result, the interlayer cooling of 3D stacked MCM through fluidic and electrical vias ought to be examined. The 3D package consists of two carriers assembled one over another with a Si spacer. The Si spacer is designed with fluidic and electrical interconnects. Both the carriers mounted with a 10 mm × 10 mm chip having heating and temperature sensing elements. The carrier is built in with microchannels for heat transfer enhancement and extracted the heat generated by the chip. The stacked module was attached to a printed circuit board using 300-µm solder balls. The footprint of the carrier is 15 mm ×15 mm × 0.8-mm. The liquid cooling solution consists of accessory thermal components in addition to the package: a mini-pump, an adapter for flow distribution, and a mini heat exchanger. A schematic of the cooling solution is shown in both Figures 71 and 72. Electrical and fluidic connectivity between carriers were achieved by TSV in the spacer. The cooling liquid is circulated through the carrier, and the heat from the chip is transported to the heat exchanger.

The entropy generation related to the pressure drop and heat transfer are utilized as a selection parameter S*, given by Eqs. (5.7). The S* for different micro-channel spacing is obtained, indicating micro-channel width from 80 µm to 110 µm having better results for various channel depth considered in our design. A micro-channel size of 100-µm width and 350-µm depth was chosen finally for the test vehicle fabrication considering the low entropy generation and ease of fabrication

$$S^* = S_{thermal} \times S_{dP}, \tag{5.7a}$$

$$S_{thermal} = \left(\frac{P}{T_{ref}}\right)^2, \tag{5.7b}$$
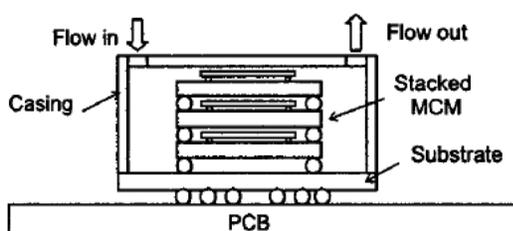
FIG. 70. Schematic of the direct cooling of 3D stacked MCM.
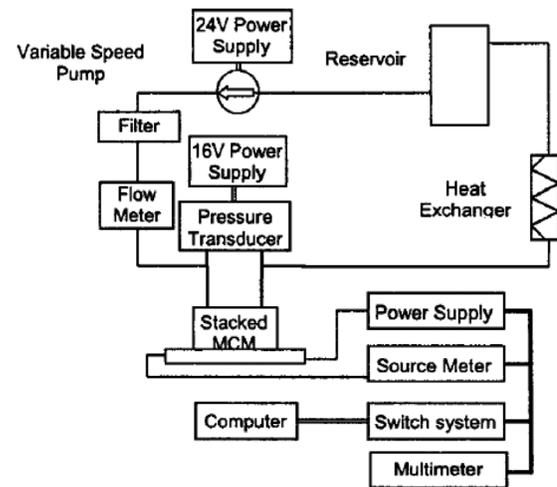
FIG. 71. Schematic of liquid cooling characterization.

$$S_{dP} = \left(\frac{dP \times G}{T_{ref}}\right). \tag{5.7c}$$

A common micro-channel arrangement is single inlet and single outlet arrangement (S1). The pressure drop across a channel is, however, high due to the long flow length, which also leads to higher chip temperature at the downstream. Due to this drawback, a split flow arrangement with dual in-ports is also designed. A schematic of the single in-port and dual in-ports design is shown in Figure 73. D1 is having a constant supply plenum, and D2 is having a reducing supply plenum. This arrangement has the benefit of reduced flow length, with the thermal developing length being a substantial portion of the channel length. We evaluated two types of dual-port design and show results in Table VIII and Figure 74 based on thermal modeling. The channel wall (fin) thickness of 50 µm, the channel width of 100 µm, and the channel depth of 350 µm were used for the heat transfer analysis. The inlet temperature of the water was assumed to be 50 °C, and a uniform heat load of 100 W/cm² was applied. By comparing the single-port and the dual-port designs, it is clear that the dual-port design has lower thermal resistance. The design
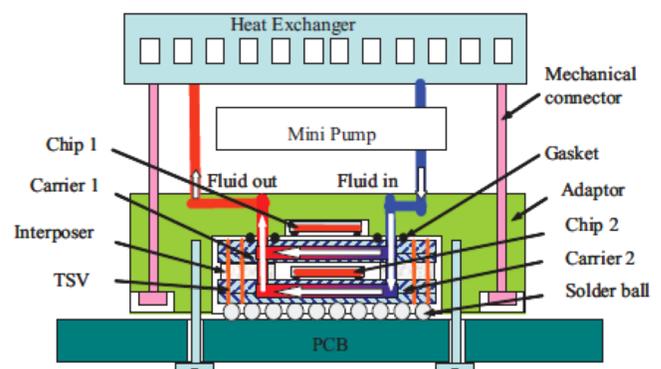
FIG. 72. Scheme of the integrated liquid cooling system for 3D stacked module (no to the scale).[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.
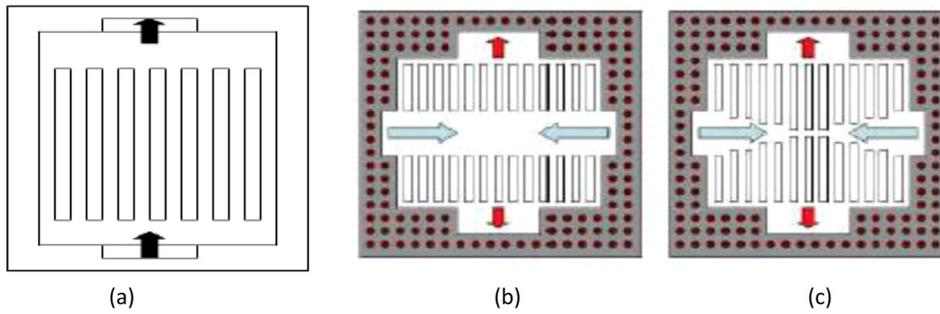
FIG. 73. (a) Single port carrier design S1 and dual port carrier designs, (b) D1, and (c) D2 on the right hand side.[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

S1 has uniform flow distribution, but the long channel length results in large temperature gradient. Comparing D1 and D2, design D2 has uniform flow distributions through the micro-channels and lower thermal resistance (based on peak chip temperature) and smaller temperature variation within the chip. Hence, we have selected D2 for the test vehicle fabrication and thermal characterization.

The developed thermal solution for the 3D stack MCM is shown in Figure 75. The measured thermal resistance is show in Figure 76. Up to 100 W/cm^2 power dissipation is tested based on the present micro-channel design (D2), with a measured thermal resistance of 0.577 kcm^2/W. This value is 40% higher than the simulation result, which could be attributed to the non-uniform flow distribution across the two carriers.

The 2.5D package is viewed as the most viable technology for 3D integration. One of the key reasons is that conventional liquid cooling techniques such micro-channels and metallic foam heat sinks[104,105] could be applied directly since a 2.5D package is essentially planar, compatible with the interposer platform. In this section, the liquid cooling for a 2.5D package shown in Sec. V B is demonstrated. A liquid cooling loop is established, which includes the micro pump (Monarch pump), heat exchanger (Lytron LL510), temperature controlled chiller (Huber K6S-NR), together with the piping and fittings. The coolant water temperature is set to 24 °C, which is within 1 °C variation from the ambient temperature. The exact inlet temperature is measured with a J-type thermocouple mounted at fluid in-port. The flow rate is fixed to be 0.4 ml/min throughout the experiments. A mini channel heat sink made of copper plated with Ni is utilized to remove the heat from the chip top, as is shown in Figure 77.

The measured junction to heat sink thermal resistances (Theta JC) is tabulated in Table IX. It is shown that the Theta JC for the bare die package is one order of magnitude smaller than the molded package. The molding layer, with a thermal conductivity of 0.7 W/mK, unfavorably adds to the thermal resistance. For the bare die package, larger power inputs (8–20 W) are supplied to achieve a junction temperature rise 7–17 °C to minimize junction temperature error in the Theta JC data reduction. A common problem in Theta JC measurement for the bare die package is the misalignment of the cold plate base with the top of the test die. Misalignment would generate additional interfacial thermal resistance and abnormally high on-chip temperature variation.

The simulation model is also conducted and the corresponding heat flux and temperature profiles for the molded package are shown in Figure 78. Since the thermal performance of the mini channel heat sink is not known, the detailed fin/channel structure is modeled together with the inlet and outlet to extract the thermal performance. A comparison of computed and measured Theta JC has been shown in Table IX. Good agreement is found for the bare die package. For the molded package, a relatively obvious discrepancy of 10.4% is found. The molded package is cross-sectioned, and the microscopic view shows a surface roughness approximately 15–20 μm. The presence of roughness is beneficial to the mold release process, but it may cause additional

TABLE VIII. Thermal simulation results for the different carrier designs.[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

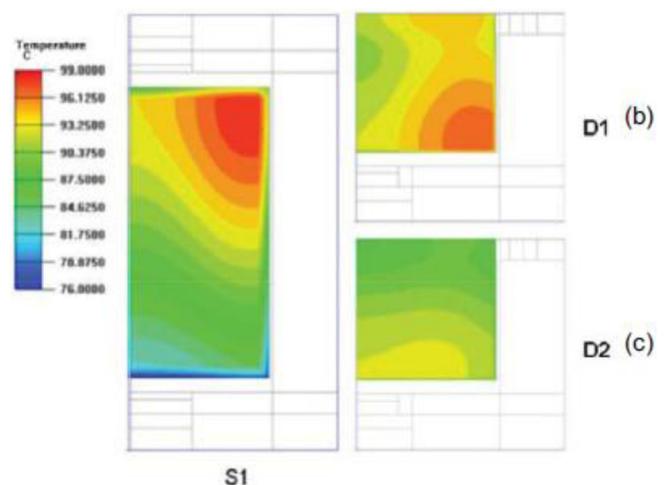| Flow rate (ml/min)	Design	Pressure drop (mbar)	Maximum temperature (°C)	Temperature variation (°C)
100	S1	158.1	98.7	22.5
	D1	55.45	97.2	8.6
	D2	76.7	93.4	9.4
200	S1	398.7	92.1	18.5
	D1	169.7	91.8	9.6
	D2	253.1	87.2	7.8

FIG. 74. Single port carrier design (S1) and dual port carrier designs (D1 and D2).[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.
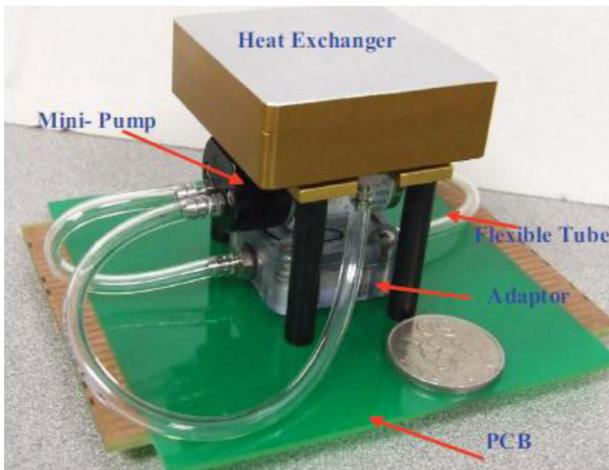
FIG. 75. Photograph of integrated cooling.[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

interfacial thermal resistance. Surface warpage also contributes to the deviation of simulation from measurement. Surface polishing process may be considered to minimize the roughness on the top of the molding compound and to reduce Theta JC.

With the validated thermal model, the thickness of overmolding for the 2.5D package is examined. Figure 79 shows the Theta JC versus the molding thickness based on simulation study. It is seen that, with the increase in overmolding thickness from 0 to 0.6 mm, the thermal resistance increases drastically from 0.82 K/W to 11.76 K/W, mainly due to the thermal conduction resistance across the overmolding layer. If additional thermal solution such as heat sink is applied at the top of the package, a thin overmolding thickness of ~0.1 mm or even bare die package can be applied to minimize the overall thermal resistance.

D. Thermal aware 2.5D design and implementation

With the growing emphasis on high performance and small form factor, and for keeping up with the advancement
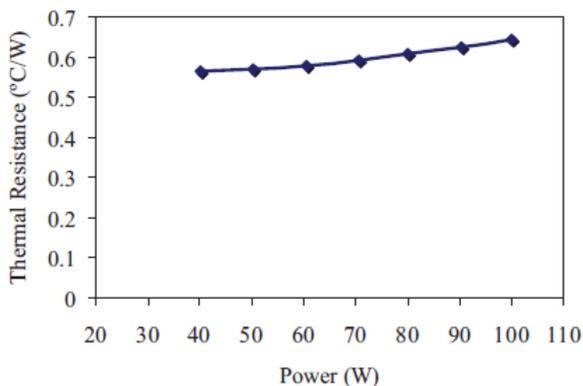
FIG. 76. Thermal resistance versus power input for the 3D package.[108] Reproduced with permission from Khan *et al.*, "3-D packaging with through-silicon via (TSV) for electrical and fluidic interconnections," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(2), 221 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.
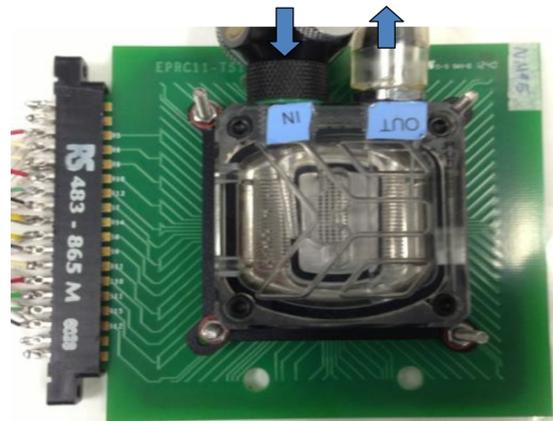
FIG. 77. Liquid cooling of 2.5D package with liquid cooling configuration.

of 2.5D/3D fabrication, thermal design has been indispensable for the implementation of 2.5D/3D integration. For space and energy tight applications, passive cooling is the preferred option. The use of interposer with properly designed TSVs can help reduce the junction temperature and minimize the hot spots on the chip. Design factors to consider include chip size, chip stacks, distributed chip arrangement and hot spot staggering on the chip, type of encapsulating mold compound, heat spreader, thermal bridging with thermally conductive adhesive, and so on.

For high power applications, 2.5D package benefits from existing cooling solutions for 2D planar chips without much change on the package format. On the other hand, interlayer cooling through liquid cooling would become the trend for the stacked high power chips and modules. Microchannels or micro pins can be used as the thermal enhancement structures. The cooling geometry, combined with TSVs and micro-bumps are influencing factors on the thermal and flow performances. Alternative direct dielectric fluid cooling as well as water based fluidic cooling can be considered. Proper liquid sealing methods are required to avoid liquid spilling, evaporation loss and possible damage to electronic circuits. Thermoelectric coolers can also be conjectured, although it is still at early stage due to limited coefficient of performance (COP). CMOS compatible Silicon Nanowires (SiNWs) fabricated on-chip can be an effective means for hot spot cooling in the 2.5D/3D packages, as well as for temperature control. Increase in nanowire number, reduction of thermal conductivity and contact resistance will lead to enhanced cooling capacity.

Thermal aware design is becoming of increasing importance. Thermal simulation shall be utilized in the design stage to examine the on-chip power dissipation and hot spot distribution arising from electrical design, the effects of package formats and material parameters, and the cooling

TABLE IX. Measured and simulation results for Theta JC.

Package types	Power input (W)	Measured R_{JC} (K/W)	Simulation R_{JC} (KAV)	Difference from measurements (%)
Molded package	2	10.9	9.76	−10.4
Bare die package	14	0.34	0.82	−0.024
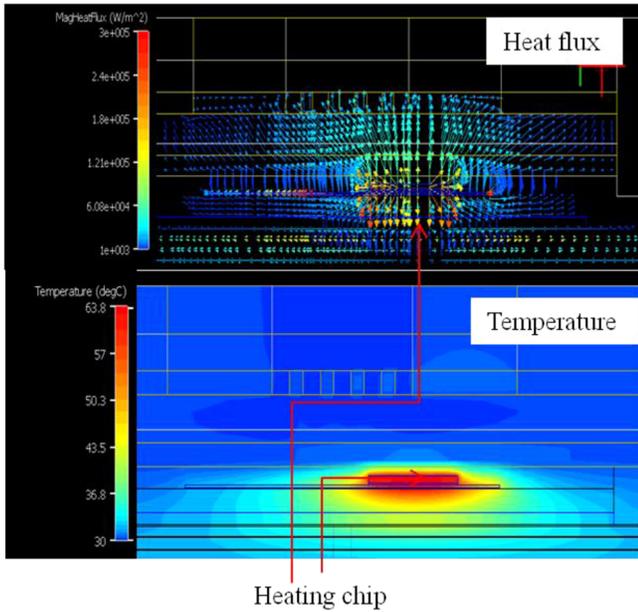
FIG. 78. Heat flux and temperature profiles for the molded package under cold plate cooling for determining the top thermal resistance.

design efficiency and the feasibility. Thermal simulation can be a useful tool in chip, TSV, and package optimization. Commercial simulation tools such as Flotherm, Icepak Comsol multi-physics are typically used for numerical modeling and optimization.

On the other hand, the thermal characterization with specially designed thermal test dies shall be used for model and design validation. In practice, the thermal simulation does not take into consideration certain complexities and tends to overestimate the thermal performance. The overestimation can be attributed to insufficient thermal and fluidic design, unanticipated packaging and process deviation. Therefore, there is a continuous need to establish the thermal characterization methodologies and develop verification cases for simulation models. If the model is validated, the designer can build on the framework to extend the thermal model for new designs and parameter studies, and to provide the optimized designs for various application scenarios. The
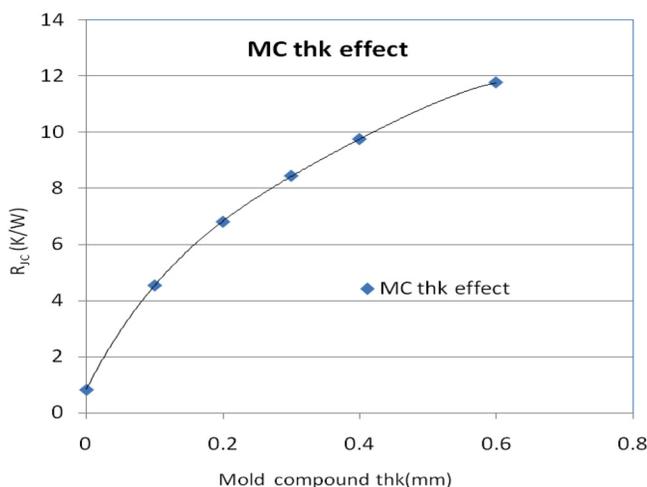
FIG. 79. Effect of molding compound thickness on the Rjc.

interactive processes among electrical, thermal and package design process are illustrated in Figure 80.

VI. THERMO-MECHANICAL DESIGN AND MODELING FOR 2.5D PACKAGING

Thermo-mechanical analysis is a critical subject that cannot be ignored when it comes to the realization of a TSI package. There are a few areas drawing the attention of TSI builders: (a) manufacturability and functionality of TSI, (b) handling of TSV wafers and chips during fabrication and assembling, and (c) packaging and long-term reliability. FEM is now a widely adopted approach for performing thermo-mechanical analysis in the industry. This section outlines the use of FEM in resolving various thermo-mechanical challenges in 2.5D packaging.

A. Manufacturability and functionality of TSI

The CTE of copper and Si are about 17 and 3 ppm/°C, respectively. The large difference in CTE between copper and Si induces a significant level of stress and strain around a copper-filled TSV when it is subjected to a substantial amount of thermal loading. Figure 81 shows the deformation of a copper-filled TSV when it is subjected to a temperature change.[123] During a temperature decrement, the copper inside the via contracts much more than the Si which holds it. The surrounding Si thus experiences, in general, a state of tension in both the radial and circumferential directions and at the same time compression in the axial direction. For the case of a TSI which comprises an array of TSVs, the stress field on the Si is a combined result of individual stress fields around each TSV.

Mechanical failures and alteration in electrical performance are adverse outcomes reported due to this stress field. Wafer cracking and delamination are common mechanical failure modes that could be encountered during the fabrication of TSI. There are design guidelines generated by FEM and we shall discuss them in Subsections VI A 1–VI A 3. The large piezoresistivity of doped Si makes active devices like p-MOSFET and n-MOSFET susceptible to variations in their electrical performance when under the influence of TSVs. The placement of these devices, thus, requires careful
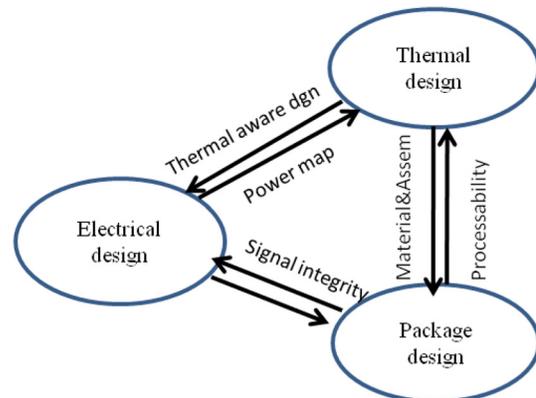
FIG. 80. Interaction among electrical, thermal design, and package design for technology implementation.
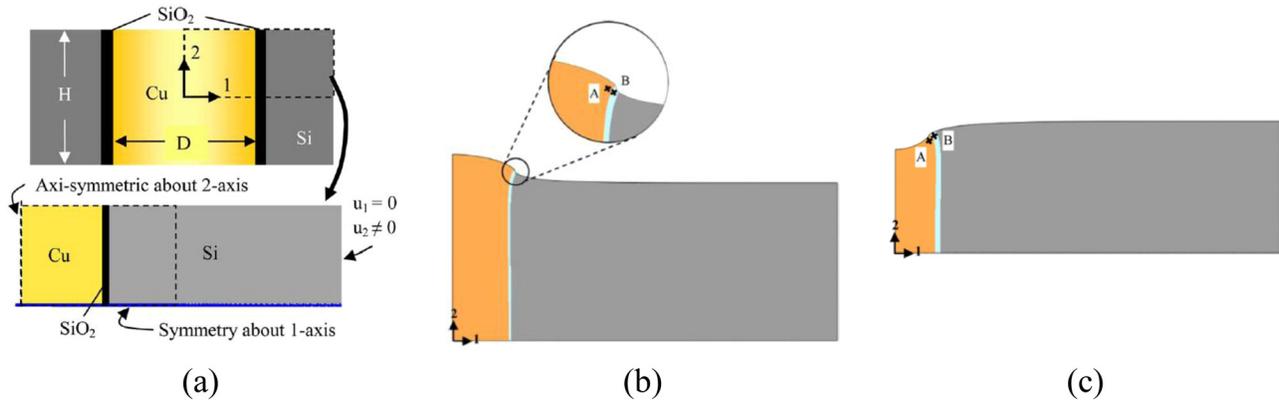
FIG. 81. Modeling of a copper-filled TSV (a) modeling strategy, (b) deformation of via during a temperature increment, and (c) deformation of via during a temperature decrement.[123] Reproduced with permission from Selvanayagam *et al.*, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," IEEE Trans. Adv. Packag. **32**(4), 720 (2009). Copyright 2009 Institute of Electrical and Electronics Engineers.

considerations. These aspects will be illustrated by the example below.

1. Design rules for avoiding wafer cracking

Wafer cracking can occur after the annealing process when the annealing temperature is too high and/or the TSVs are too tightly packed.[124] Accordingly, the chance of this failure can be characterized by the 1st principal stress σ_1 induced on the chip surface at the edge of a TSV as depicted in Figure 82.

Modeling results suggest that the chance of wafer cracking increases with larger TSV diameter, smaller TSV pitch-to-diameter ratio, smaller TSV depth, smaller dielectric layer thickness, smaller barrier layer thickness, larger wafer thickness, and higher annealing temperature. The minimum required pitch-to-diameter ratio $p:d$ for fabricating a TSI at a given annealing temperature T may be estimated empirically by[124]

$$\eta \cdot k \cdot \left[1 + 2.76 \left(\frac{2p}{d} - 1 \right)^{-2} \right] \le 287 \text{ MPa},$$

$$\text{where } k = \frac{E_{\text{via}}(\alpha_{\text{via}} - \alpha_{\text{si}})(T - 25°\text{C})}{1 - 2\nu_{\text{via}} + \frac{1 + \nu_{\text{si}}}{1 + \nu_{\text{via}}} \frac{E_{\text{via}}}{E_{\text{si}}}},$$

$$E_{\text{via}} = f_{\text{Cu}}E_{\text{Cu}} + f_{\text{SiO}_2}E_{\text{SiO}_2} + f_{\text{Ta}}E_{\text{Ta}},$$

$$\nu_{\text{via}} = f_{\text{Cu}}\nu_{\text{Cu}} + f_{\text{SiO}_2}\nu_{\text{SiO}_2} + f_{\text{Ta}}\nu_{\text{Ta}},$$

$$\alpha_{\text{via}} = \frac{f_{\text{Cu}}E_{\text{Cu}}\alpha_{\text{Cu}} + f_{\text{SiO}_2}E_{\text{SiO}_2}\alpha_{\text{SiO}_2} + f_{\text{Ta}}E_{\text{Ta}}\alpha_{\text{Ta}}}{f_{\text{Cu}}E_{\text{Cu}} + f_{\text{SiO}_2}E_{\text{SiO}_2} + f_{\text{Ta}}E_{\text{Ta}}}. \quad (6.1)$$

Here, f is the volume fraction of the corresponding component of a TSV and η is the safety factor advised to be above 1.1. E, ν, and α are the Young's modulus, Poisson's ratio, and CTE of the corresponding components, respectively.

2. Design rules for reducing copper protrusion

Copper protrusion is one major factor causing delamination of BEOL metal layers.[125] Generated by FEM, Figure 83
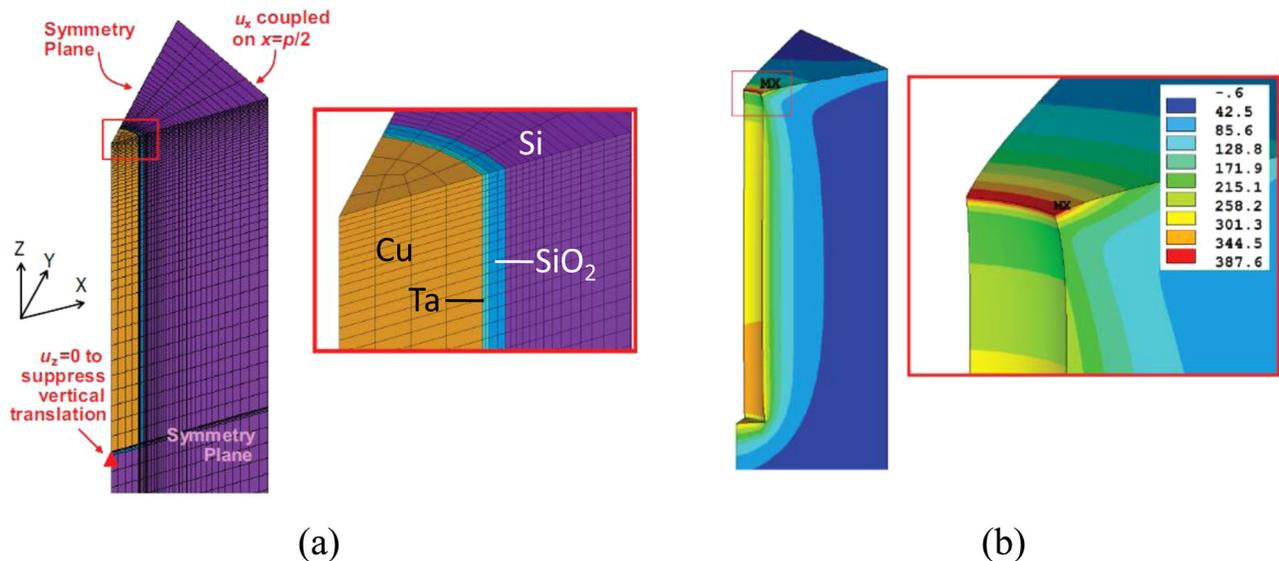
FIG. 82. Modeling of wafer cracking stress induced around a TSV. (a) Finite element model for the analysis and (b) σ_1 (in MPa) induced in Si.[124] Reproduced with permission from Chan *et al.*, "Thermo-mechanical design rules for the fabrication of TSV interposers," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(4), 633 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.
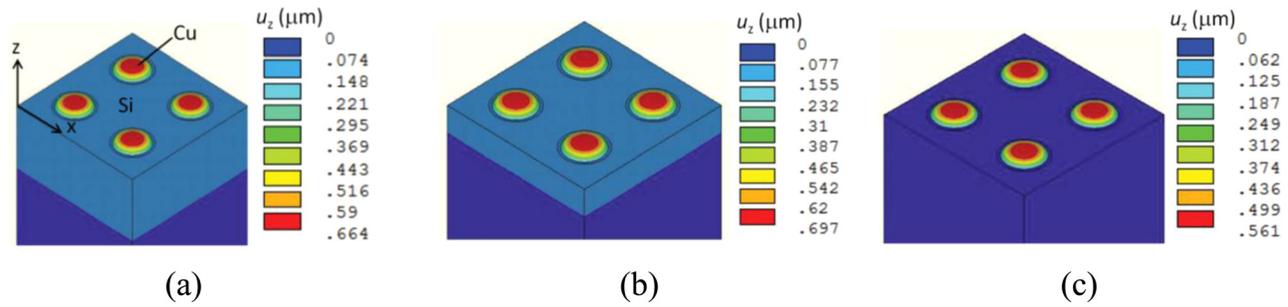
FIG. 83. Copper protrusion FEM results: (a) Right after ramping up to 400 °C, (b) held for 30 min at 400 °C, and (c) cooled down to room temperature.[125] Reproduced with permission from Che *et al.*, "Study on Cu protrusion of through-silicon via," IEEE Trans. Compon., Packag., Manuf. Technol. **3**(5), 732 (2013). Copyright 2013 Institute of Electrical and Electronics Engineers.

illustrates the development of copper protrusion at different stages of an annealing process. Accordingly, copper protrusion grows with higher annealing temperature, longer duration, greater TSV depth, and larger TSV diameter. Hence, smaller and sparsely allocated TSVs are recommended to be adopted for reducing copper protrusion.[125]

As the major manufacturability concerns are raised by the via-filling material copper, there are investigations reported on the use of unfilled TSVs[123] and polymer filled vias.[126] These alternative technologies generally do help to reduce the thermal stress induced at the TSVs. However, they are either incompatible with the current CMOS technologies or are not in favor of the miniaturization trend. Copper, hence, remains the most popular filling material due to its compatibility and high electrical conductivity.

3. Design for reducing mobility change of MOSFETs near TSVs

p-MOSFET and n-MOSFET behave differently under the influence of stress. Specifically, their resistances vary to different extents with respect to different stress components. When a p-MOSFET is oriented along the [110] direction and is placed in between TSVs which are formed along the ⟨110⟩ directions in a rectangular manner, it is found to be more susceptible to mobility change than an n-MOSFET no matter how the n-MOSFET is oriented. This scenario is demonstrated in Figure 84.[127] At these positions, placement of

p-MOSFETs should in fact be avoided. N-MOSFETs oriented along [110] are better devices to be placed at these locations since their mobility change will be negligible (<1%). Active devices, therefore, should be allocated strategically so as to minimize their change in electrical performance when they are placed near the TSVs.

B. Handling of TSV wafers and chips during fabrication and assembling

Warpage is a key challenge to be addressed for handling of TSV wafers. This is again a CTE mismatch problem but more packaging materials can be involved in this case. Wafer warpage can obstruct wafers from being handled properly by fabrication tools. Not only it affects fabrication accuracy but may also detrimental to the entire fabrication process. The modeling of wafer warpage is critical in 2.5D packaging and it will be discussed in the following subsession. The use of TSI involves at least one chip-stacking step. When a chip is to be stacked on one another, the bottom one may crack as a result of the stacking force. An example will be given below with strategies provided to solve the problem.

1. Design for reducing TSV wafer warpage

It is not a straight forward task to model a TSV wafer, due to the enormous amount of TSVs it carries. One methodology
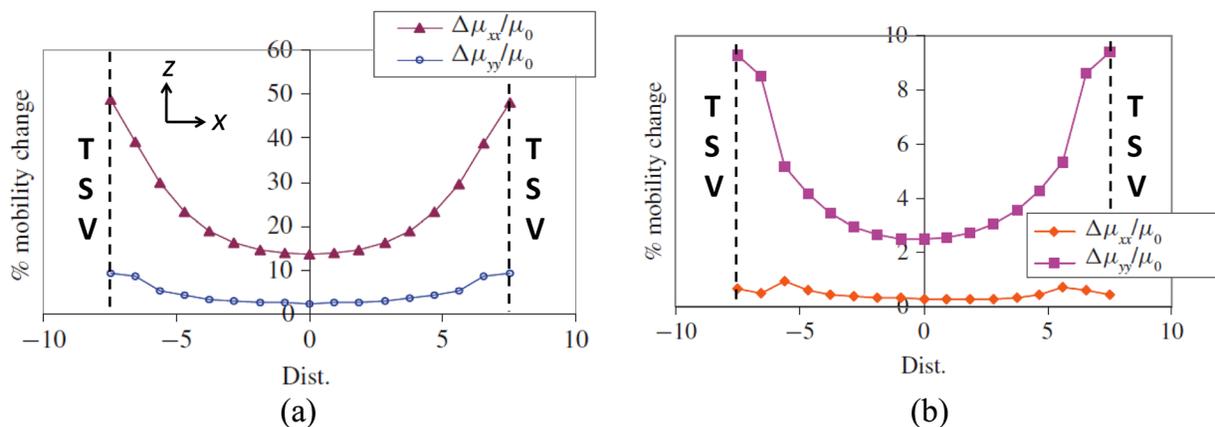
FIG. 84. Percent change in mobility due to the presence of 10 μm TSVs which are 25 μm apart for (a) p-MOSFET and (b) n-MOSFET. TSVs align with [110].[127] Reproduced with permission from Selvanayagam *et al.*, "Modeling stress in silicon with TSVs and its effect on mobility," IEEE Trans. Compon., Packag., Manuf. Technol. **1**(9), 1328 (2011). Copyright 2011 Institute of Electrical and Electronics Engineers.
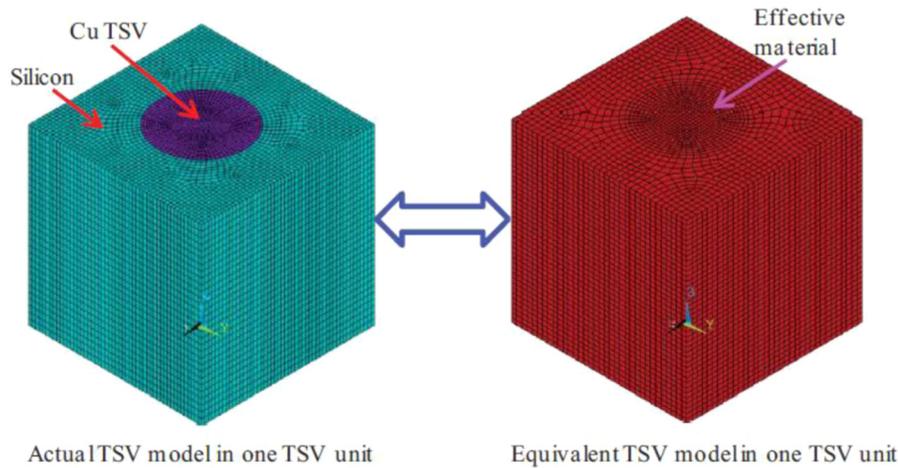
FIG. 85. Use of an effective material to develop an equivalent TSV model.[128] Reproduced with permission from Che *et al*., "Development of wafer-level warpage and stress modeling methodology and its application in process optimization for TSV wafers," IEEE Trans. Compon., Packag., Manuf. Technol. **2**(6), 944 (2012). Copyright 2012 Institute of Electrical and Electronics Engineers.

for achieving this mission is to adopt an "equivalent TSV model"[128] as depicted in Figure 85. The model can be developed by employing an effective material such that the necessary mechanical responses of the original system can be preserved. With the equivalent TSV model, it is found that the warpage of a TSV wafer increases with larger overburden thickness, higher annealing temperature, and smaller TSV pitch-to-diameter ratio. The wafer warpage will be largest when the depth of TSVs equals one half of the wafer thickness. One effective approach for reducing the TSV wafer warpage is to introduce an extra CMP step before annealing the wafer.

2. Design for avoiding die-cracking during chip stacking

Die-cracking may happen to the carrier chip as it bends during a chip stacking process.[129] Accordingly, the loading experienced by the carrier chip depends on the solder bump layouts of both the carrier chip and the stacking chip. Insertion of "dummy bumps" beneath the carrier chip is an effective approach for redistributing the loading exerted onto it. Figure 86 demonstrates the use of dummy bumps for reducing the deflection and bending stress experienced by a

carrier chip. With the knowledge of the die strength acquired by some kinds of bending tests, the issue with die-cracking can be avoided with an optimized design with the aid of modeling.

C. Packaging and long-term reliability

As a result of the fragile low-k material employed today, packaging can be either protective or damaging to the chip depending on the kind of technology adopted. This area of investigation is termed as chip package interaction (CPI). TSI is, fortunately, a protective technology in terms of CPI as will be elaborated below. The long-term reliability of a package is typically characterized by its solder joint thermal fatigue performance when subjected to temperature cycling test (TCT). Critical factors in this area will be discussed as follows.

1. CPI and micro solder bump reliability of TSI

Figure 87 shows a typical TSI package which carries a Cu/low-K chip.[130] If there are no TSIs, the micro-bumps will be subjected to a severe shear loading induced by the large mismatch in CTE between the Cu/low-k chip ($\sim$3 ppm/$^\circ$C) and the bismaleimide triazine (BT) substrate ($\sim$13 ppm/$^\circ$C).
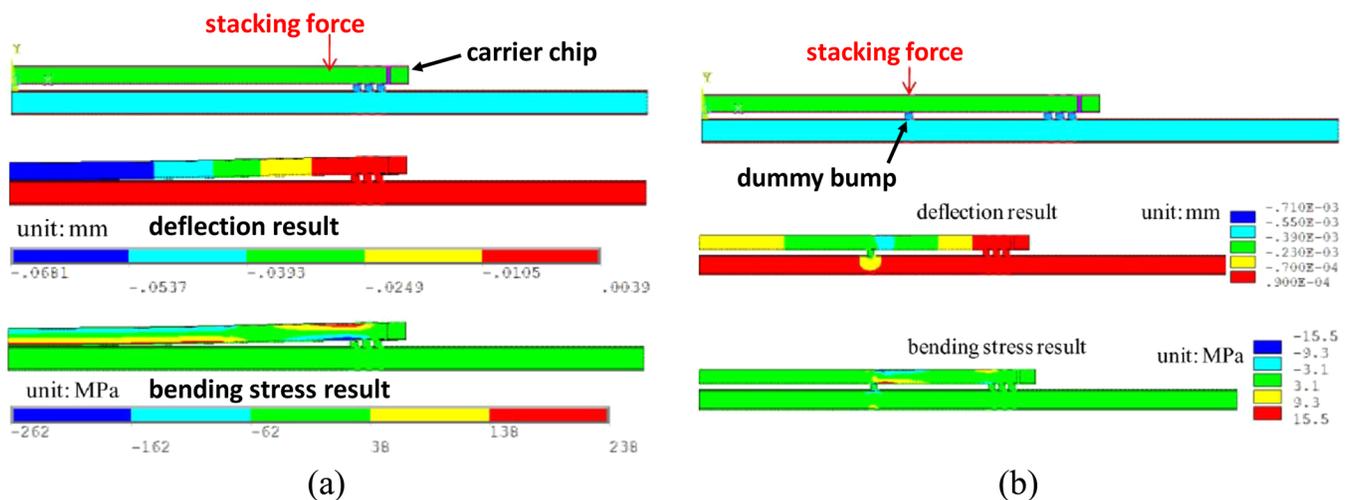
FIG. 86. Die deflection u_y and bending stress u_x results during a chip stacking process for (a) original bump layout design and (b) optimized bump layout design.[129] Reproduced with permission from Che *et al*., "Structure design optimization and reliability analysis on a pyramidal-shape three-die-stacked package with through-silicon via," IEEE Trans. Device Mater. Reliab. **12**(2), (2012). Copyright 2012 Institute of Electrical and Electronics Engineers.
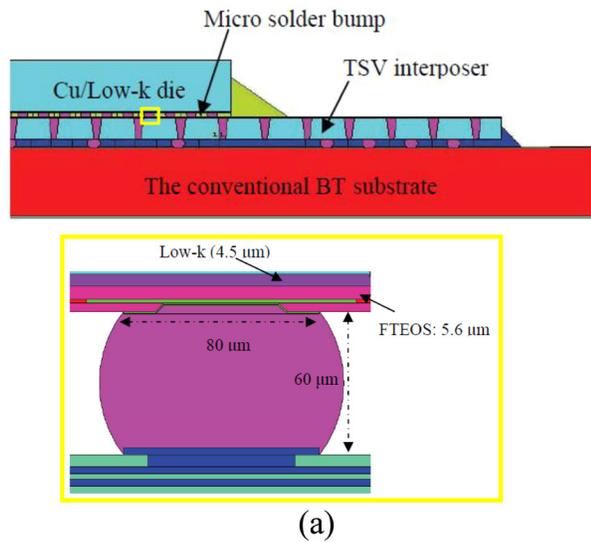
FIG. 87. CPI of a typical TSI package (a) Package geometry and (b) Effect of TSI on low-k stress.[130] Reproduced with permission from Zhang *et al.*, "Development of through silicon via (TSV) interposer technology for large die (21 × 21 mm) fine-pitch Cu/low-k FCBGA package," in *Proceedings of 59th Electronic Components and Technology Conference (EPTC)*, San Diego, CA, USA, May 2009, p. 305. Copyright 2009 Institute of Electrical and Electronics Engineers.

This severe shear loading will be transmitted to the low-k layer and eventually results in its damage. Now with the TSI added which possesses a CTE similar to that of a Si chip, most of the shear loading is expected to be carried by the C4 bumps between the TSI and the BT substrate. The use of TSI, from this perspective, is like putting a barrier (or a stress buffer layer) in between the Cu/low-k chip and the BT substrate. This helps to shield the shear loading induced to the micro-bumps and the low-k layer and hence protecting the chip. Thermo-mechanical simulation shows: (i) the impact of TSV interposer reduces the low-k stress (by more than 50%) and correspondingly decreases the creep strain energy density per cycle (ΔW) in the micro solder bumps (by more than 28%). Thus, he package reliability and micro solder joint reliability can be greatly improved, (ii) more than 60% reduction in the low-k stress and 7% reduction in ΔW have been observed when the underfill between the Si chip and the TSV interposer, as well as the underfill between the TSV interposer and the BT substrate are used. Thus, two underfills which lead to lower stress/strain in the low-k layer and micro solder bumps are recommended, (iii) more than 50% reduction in the low-k stress and 10% reduction in the ΔW in micro solder bumps have been observed when via top diameter/via bottom diameter is decreased from $100\,\mu m/50\,\mu m$ to $50\,\mu m/10\,\mu m$. Thus, a smaller via is recommended, and (iv) 59% reduction in the low-k stress and 35% reduction in ΔW in micro solder bumps have been observed when low-k die thickness decreases from $750\,\mu m$ to $300\,\mu m$. Thus, a thinner low-k chip is recommended.

2. Design for enhancing solder joint reliability of packages with Si carrier

It is understood that TSI plays a role in enhancing the solder joint reliability of micro-bumps.[130] However, the C4 bumps that connect the TSI to the BT substrate are now more prone to failure. Underfill is the remedy to this

problem,[131] as shown in Figure 88. Accordingly, low CTE and high glass transition temperature T_g are favored properties for this underfill.

3. Demonstration a low stress bond pad design for low temperature micro bumps on TSVs

The proposed design of the pad (Figure 89) is one in which there is no direct contact between the pad and the copper-filled via.[132,133] The pad is shaped such that it surrounds the via, but does not touch it. The positioning of the pad with respect to the via is such that they are coaxial. Electrical connectivity between the via and the pad is provided through the presence of traces. One possible design is
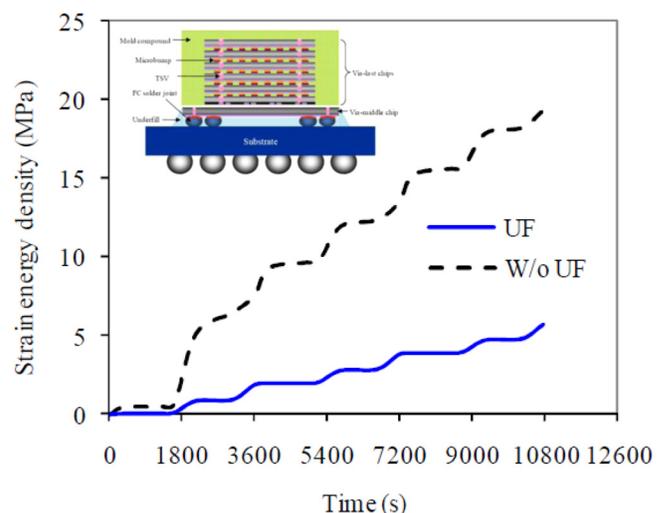
FIG. 88. Effect of underfill on C4 bumps of a 3D package.[131] Reproduced with permission from Che *et al.*, "The study of thermo-mechanical reliability for multi-layer stacked chip module with through-silicon-via (TSV)," in *Proceedings of 12th Electronics Packaging Technology Conference (EPTC)*, Singapore, December 2010, p. 743. Copyright 2012 Institute of Electrical and Electronics Engineers.

FIG. 89. Schematic diagram showing dimensions used in mechanical modeling for (a) the full pad and (b) the proposes pad (i.e., the ring pad).[132] Reproduced with permission from Zhang *et al.*, "A low stress bond pad design for low temperature solder interconnections on through silicon vias (TSVs)," IEEE Trans. Compon., Packag., Manuf. Technol. **1**(4), 510 (2011). Copyright 2011 Institute of Electrical and Electronics Engineers.

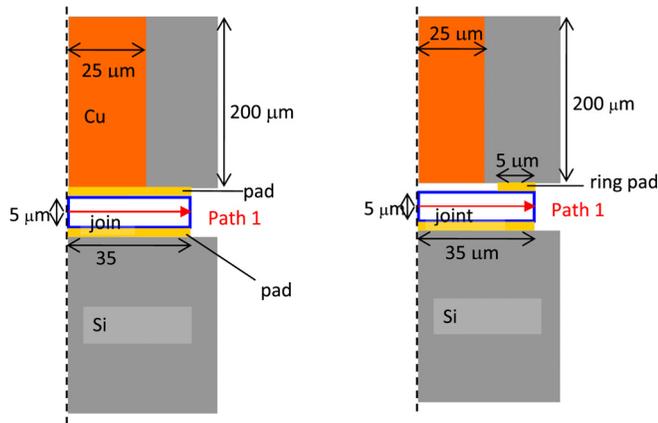a ring-shaped pad. In this structure, the joint wets only to the pad and not the traces or via in between. Such a design will effectively decouple the via from the micro bump, such that the micro bump is unaffected by any contraction of the TSV. This proposed design does not involve any additional fabrication or material cost. Fabrication of the pads only requires a change in the mask design to implement. Figure 90 shows that with the proposed pad design, the maximum tensile stress in the micro bump decreases by 50%. Reliability assessment has also been done in order to compare the proposed pad design with the conventional design. It is found that the samples with the proposed design have a better drop impact reliability performance than the samples with the conventional full pad design. In this paper, a double-sided multilayer metallization process on 200 μm TSV wafer with the low temperature and low volume lead-free solder (Sn (0.5 μm)/In (2 μm)/Au (0.05 μm)) has been demonstrated. Low temperature micro bump process for C2C has also been established, which is highly desirable for next generation IC
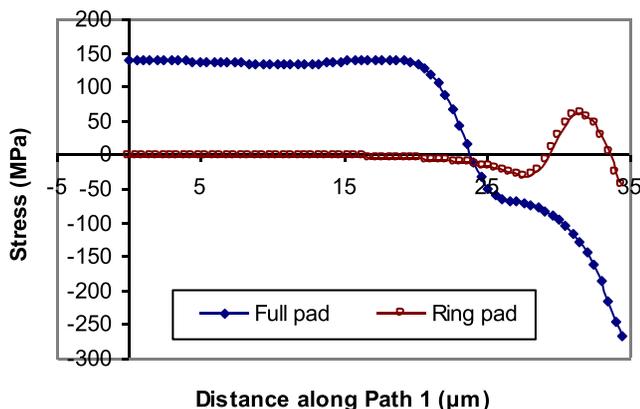
FIG. 90. Graph of stress (S33) along mid plane of bond for the full pad and the ring pad.[132] Reproduced with permission from Zhang *et al.*, "A low stress bond pad design for low temperature solder interconnections on through silicon vias (TSVs)," IEEE Trans. Compon., Packag., Manuf. Technol. **1**(4), 510 (2011). Copyright 2011 Institute of Electrical and Electronics Engineers.

packaging, where multifunctional chips such as memory, logic, and MEMS devices are used.

VII. EDA CONSIDERATIONS AND READINESS

As with conventional ICs, readiness of the EDA tools is essential to sign-off TSI based 2.5D ICs. While choosing EDA platforms for 2.5D IC design, designers typically face a choice between using dedicated 3D EDA tools (i.e., 3D IC compiler[134] and 3D system-on-chip (SoC) Encounter[135]) and making necessary enhancements to existing industry-standard and proven 2D EDA platforms. In our work, we have relied on the latter since 2.5D ICs are a mid-point between traditional 2D ICs and 3D stacks. Moreover, we have developed a methodology to enhance existing 2D IC design tools to achieve 2.5D IC design closure on TSI which contains TSVs in a floating TSI substrate. In this section, we describe the methodology to incorporate various components of TSI technology (i.e., uBumps, BEOL/RDL lines, TSV, C4 bumps, etc.) in 2.5D TSI PDK using (1) technology layout-entry-format (LEF) files, (2) Parasitic Extraction (PEX) rule decks and TSV extraction, and (3) design Rule Checks (DRC)/Layout Versus Schematic (LVS) rule decks. TSV design rules along with TSV and C4 bump parasitic extraction form major modifications to enable 2D EDA tools to perform 2.5D IC design closure. PDK provides an infrastructure to support a reference EDA flow that enables the designer to sign-off 2.5D ICs. 2.5D TSI design flow composing of: (A) design import, (B) floor planning and placement, (C) routing on 2.5D TSI, (D) SI and PI verification, followed by (E) DRC and LVS verification is described. A sample case-study consisting of FPGA and memory foot print on 2.5D TSI is illustrated as well.

A. 2.5D IC PDK

2.5D PDK predominantly consists of (1) technology LEF files, (2) PEX rule decks and TSV extraction, and (3) DRC/LVS rule decks. These will be elaborated below.

1. Technology LEF files

The technology LEF files detail the routing and via layers description. Concurrently, viewer files are built to aid the viewing of the layers for some tools. The layer map is then used in the EDA flow to construct test chips as well as physical designs of 2.5D TSI. In addition to the technology LEF, block level LEF files describing physical co-ordinates of the I/Os corresponding to every block are also required during the physical design flow.

2. PEX rule decks and TSV extraction

The major difference between 2.5D TSI technology and traditional 2D IC technology is that the Si substrate is not grounded in 2.5D IC technology but is floating. The floating Si substrate acts as pseudo metallic plate for a typical Si substrate resistivity of 1–100 Ω-cm. TSV is also different compared to the traditional BEOL wires as it is surrounded by Si substrate rather than the usual SiO_2 or low-k dielectrics. The lumped "RC" model[136] of the TSV is used to extract TSV as
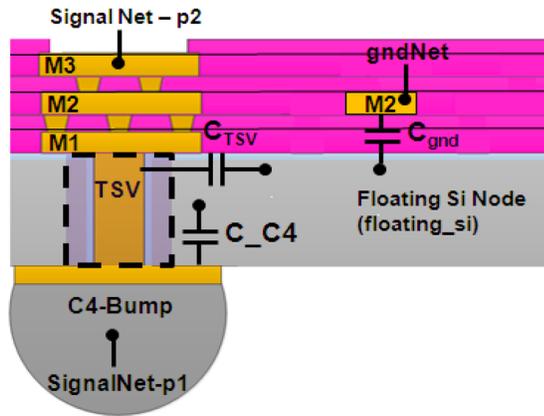
FIG. 91. Parasitic capacitances associated with TSV, C4 bump and ground net in 2.5D TSI.

a device. The R_{TSV} and C_{TSV} are obtained from the TSV daisy chain as well as the TSV embedded and de-embedded bank characterization structures detailed in Sec. IV. Temperature dependent TSV "RC" models derived through modeling[136] or measurements can also be employed. Parallel plate model or characterized capacitance values for C_C4 are employed for C4 bumps. Parasitic capacitances associated with TSV, C4 bump, and ground net in 2.5D TSI are illustrated in Figure 91.

The process of building the PEX rule deck for front side BEOL or RDL interconnects is similar to traditional 2D interconnects and the characterized RC values of different routing layers and the via layers are incorporated to achieve parasitic extraction. However, the extraction methodology for TSV and C4 bump is different and follows a two-step extraction process that is described in this paper. The two step extraction methodology consists of (a) extracting TSV as well as the C4 bumps with respect to the floating Si substrate and (b) merging the netlist with other front side extracted nets with floating Si as a common node is employed. In an actual extraction netlist TSV and C4 bumps are modeled as lumped RC elements. Front side interconnects are extracted and merged with TSV and C4 bump extraction using the floating Si node. Consider a signal net starting from the C4 bump point Signal Net—p1 and ending on M3 at Signal Net—p2. The ground net is located at M2 with gndNet as a terminal. The resulting parasitic extraction model of the Signal Net is illustrated in Figure 92. The extracted TSV capacitance (C_{TSV}) and C4 bump capacitance (C_C4) and C_{gnd} are merged on the

floating Si node using the 2 step extraction methodology. The front side interconnects are extracted using the usual 2D extraction methodology. The associated paths on M1, M2, are extracted as R_M1, C_M1 and R_M2, C_M2, respectively, while vias V1 and V2 are extracted as resistances alone, R_V1 and R_V2, respectively.

3. DRC/LVS rule decks

• DRC rule decks

Similar to 2D ICs, 2.5D IC DRC are important to verify the manufacturability of the 2.5D IC. Similar to 2D ICs, minimum size and spacing constraints on the routing and via layers are captured as design rules in the 2.5D IC design rule decks. The design rules for the traditional BEOL and front side RDL technology are implemented in addition to the design rules for the TSV ($\varphi_{TSV} = 10\,\mu m$; Pitch = $50\,\mu m$) as shown in Figures 93 and 94, respectively. In addition, due to resulting dishing during via manufacturing for typical via size >5–$7\,\mu m$, stacked vias are difficult to manufacture and staggered vias are recommended as shown in Figure 95. With reduced via dimensions $<2\,\mu m$, it could be likely to achieve stacked vias if dishing can be controlled.

• LVS rule decks

As in 2D ICs, the LVS rules decks in 2.5D are critical to capture the errors in the 2.5D layout such that 2.5D physical design is in sync with 2.5D schematic/netlist. The connectivity information is obtained from schematic/netlist while the physical connections form the layout. LVS rules are essential to identify open/short errors in the layout.

B. 2.5D IC EDA flow

2.5D TSI design flow built leveraging existing 2D design tools is illustrated in Figure 96. The flow leverages the PDK elements along with the design inputs such as design netlist and the design constraints to accomplish the 2.5D IC design closure. The description of each major step is as follows.

1. Design import

A synthesized netlist is obtained from the front end design sign-off and is used to import the design. As the 2D IC netlist consists of gate-to-gate connections predominantly, 2.5D IC netlist describes the chip-to-chip connections
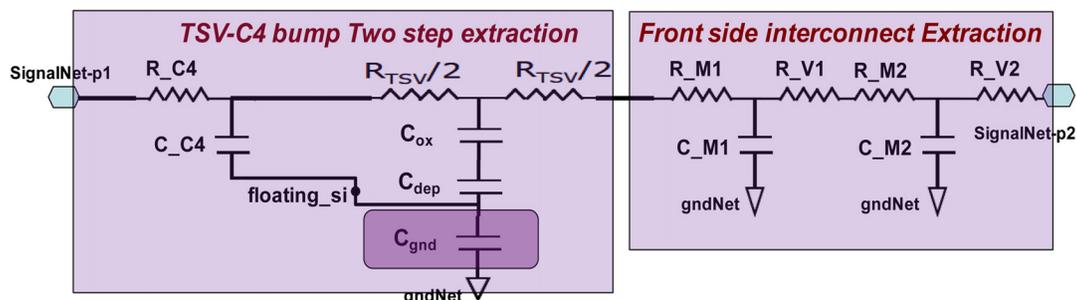
FIG. 92. Line extraction model in 2.5D TSI extracted using 2 step extraction methodology.

FIG. 93. Schematic illustrating the design rules for TSV.

as well as the chip-to-package I/O connections. Once the design is imported, the floor planning and placement of the chips on 2.5D TSI is performed as described in Sec. VII B 2.

2. Floor planning and placement

Floor-planning and placement of the guest dies are performed before routing the netlist. Floor planning, as well as Placement and Routing (PnR) require technology LEF and individual Library Exchange Format (LEF)/Design Exchange Format (DEF) description of the desig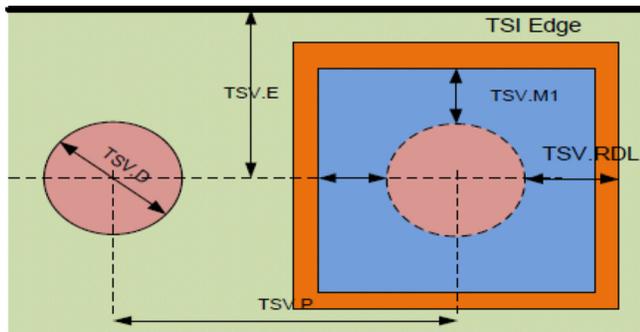n blocks (i.e., FPGA and Memory blocks) for confirming the relative front-side micro-bump locations of individual blocks. Once the design is floor planned, the I/O terminals of the design are assigned to the back-side C4 bumps spaced regularly such that the routing distance between the back side C4 bumps and the front side micro-bumps is minimized. Once the location of the I/O terminals on the back side of the 2.5D TSI as well as the front-side micro-bump locations of the individual blocks is confirmed, the design is ready for routing.

3. Routing on 2.5D TSI

The connectivity of connections is specified in the synthesized netlist provided while the micro-bump locations specify the x-y co-ordinates of the end points to be routed. The designers have an option to impose area constraints on the design in case certain area needs to be dedicated for power routing, etc. The infrastructure enables the designers to layout 2.5D circuits as seamlessly as they are used in layout 2D circuits. Moreover, TSVs are routed automatically and the environment can be leveraged to explore the impact of disparate wiring sizes and pitches on the design routing ability.

4. Parasitic extraction

Parasitic extraction is another critical step before SI and PI verification are performed. Two-step extraction methodology detailed in Sec. VII B is used for accurate TSV and C4 bump extraction. The post-layout extracted netlist is further used for Signal Integrity (SI) and Power Integrity (PI) verification.

5. SI and PI verification

To verify the SI of the design, the shortest, most typical, and longest lines in the design are extracted and simulated using spectre[137] to perform eye-diagram simulations. System design constraints are considered for simulations as well. Static IR drop analysis is performed to verify the low resistance Power Delivery Network (PDN) for a specified current carrying the capacity of the chip.

6. DRC and LVS verification

After SI/PI verification and DRC/LVS confirmations, the sign-off.gds is generated for manufacturing purpose.

C. 2.5D functional vehicle design—A case study

FPGA and DRAM integration[138] is now shown to demonstrate the EDA flow that uses the 2.5D TSI PDK. Figure 97 shows the schematic of the design. Figure 98 depicts the results achieved at various steps in the EDA flow. Design import in step (a) is achieved prior to the FPGA and DRAM memory placement performed in step (b). The back side C4 bumps minimizing the routing distance is planned as well. Once the connectivity is known through the netlist and x-y coordinates are determined after the placement of the FPGA and DRAM memory chips together with the back side C4 bumps, design is ready for routing. The resultant auto-routing with RDL technology (thickness $= 3\,\mu$m, width $= 5\,\mu$m, and pitch $= 10\,\mu$m) achieved is depicted in step (c).

The schematic used to simulate the SI for timing verification is shown in Figure 99. Z_{driver} denotes the driver impedance while C_{tx} and C_{rx} denote the capacitance at the transmitter and receiver ends, respectively. The post layout extracted spice netlist of chip-2-chip interconnect line between the FPGA and DRAM memory blocks is used for spice simulations. Length of the extracted 2.5D TSI interconnections is $\sim$25 mm. Eye diagram spectre[137] simulation results for different data rates, Z_{driver} and I/O capacitances are shown in Figure 100 while Table X lists the eye height, eye width, and jitter estimated for these data rates. It could be readily seen that the eye width, eye height, as well as the jitter for the chip-2-chip interconnect line deteriorate with

Symbol	Description	Min	Max
TSV.D	TSV diameter	10 μm	10 μm
TSV.P	TSV pitch	50 μm	N.A.
TSV.E	TSV center to TSI edge distance	300 μm	N.A.
TSV.M1	M1 overlap of TSV pad	2 μm	12 μm
TSV.RDL	RDL overlap of TSV	4 μm	200 μm (When with the C4 bump)
TSV.d	TSV density	N.A.	1%

FIG. 94. Design rules for TSV.

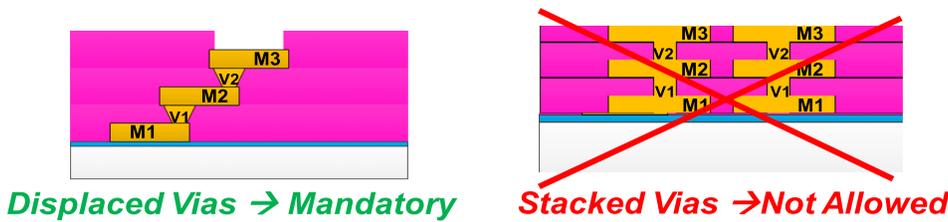**Displaced Vias → Mandatory**   **Stacked Vias →Not Allowed**

FIG. 95. Stacked vias are not allowed for front side RDL technology.

increasing data rates. Moreover, driver impedance as well as I/O capacitances tuning are required to reach the desired speed of 2 GT/s. The data-rate could further be improved by optimizing interconnect technology parameters such as width and spacing.

Constructing a robust PDN needs a strategic approach as it should be ensured that the resistance of the PDN is as minimal as possible. Dedicated metal layers mimicking the power and ground planes are constructed. The ground C4 bumps are connected to the ground plane directly using TSVs while the ground plane is slotted to realize the connection between the C4 bumps and the ground plane through parallel TSVs, as well as BEOL vias if required. Similarly, the power/ground plane is connected to the front side micro-bump using multiple vias and minimal routing on the metal layers. After PDN construction, post layout extraction of the PDN is performed and is simulated using the schematic view illustrated in Figure 101. Simulation results are used to validate the static IR drop on Voltage Drain Drain (VDD) as well as Voltage Source Source (VSS) rails. Current source mimicking the chip current consumption is a key input parameter to evaluate the IR Drop_VDD and IR_Drop_VSS obtained at the micro-bump of the FPGA and Memory guest dies.

For the given test case, current carrying capacity of the chip is considered to be 3 A with $V_{dd} = 1$ V and $V_{ss} = 0$ V biasing the back side C4 bumps. Test bench (.dc) simulation results at the front-side micro-bump locations estimate the IR drop of the V_{DD} net to be 3.97 V, while the IR drop at VSS net is estimated to be 1.02 mV. Thus, minimal IR drop ($\sim{<}10\%$ Vdd) suggests that PDN performance is acceptable, provided that the IR drop falls within desired limits. Such low value of the IR drop is due to highly conductive PDN constructed through slotted cheese architecture and low impedance vias.

FIG. 96. 2.5D IC physical design flow.

VIII. REVISITING APPLICATIONS AND BENEFITS OF 2.5D TSI TECHNOLOGY

Application requirements and technology development are significantly interlaced. While advanced state-of-the-art application requirements drive technology nodes for numerous advanced technologies, advanced technologies in many domains do act as a catalyst realizing niche applications. In this section, the application roadmap that could potentially leverage 2.5D TSI technology is addressed followed by 2.5D technology component specifications and integration schemes to enable novel applications.

A. 2.5D TSI technology—Application space

The proliferation of electronic devices has been unprecedented in a modern day human life. The growing demands of connectivity/internet along with smart applications in various industrial/business sectors, such as media, gaming, automobile, industry, bio, defense, and space, have lead to a mammoth growth of data generation and increased the storage and processing requirements. As a cliché, mankind is generating more data in two days than we did from the dawn of man until 2003.[139] It is forecasted that the diverse and exploding digital universe is experiencing the information doubling every 18 months.[140] Today, existing number of digital bits is more than stars in the universe and the data is growing at a phenomenal factor of 10 every 5 years. Big data storage, processing/analysis, etc., can only be supported through continuous technology innovations and semiconductor industry supporting the foundation of the pyramid of electronic innovation needs to enable efficient (i.e., low power and low area/form factor) and high data rate data centers, communication fabrics, mobile, as well as sensing device networks.

At subsystem level, the demand for moving large volumes of data translates into the ability to exchange information between logic ICs and Memory ICs. 2.5D TSI technology provides a new way to interconnect ICs in a manner that provides higher performance at lower power consumption. Over the next few years, this technology will enable design and manufacture of (a) Graphics Processing Units, smartphones, tablets which need longer battery life, (b) data-centers that handle larger volumes of information, yet consuming
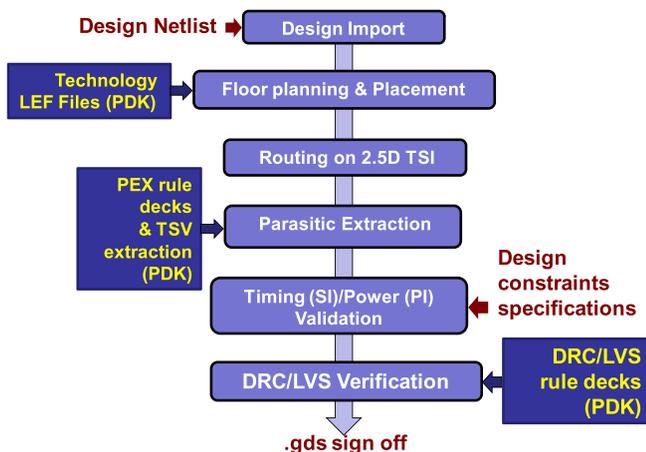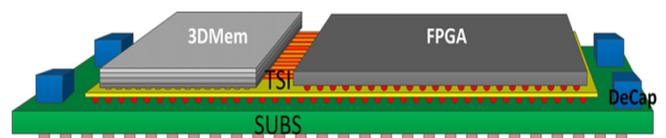
FIG. 97. Schematic of the FPGA and DRAM memory integration on 2.5D TSI.

(a) Design Import   **(b) FPGA & Memory placement**   **(c) Auto-routed 2.5D TSI design with TSVs**
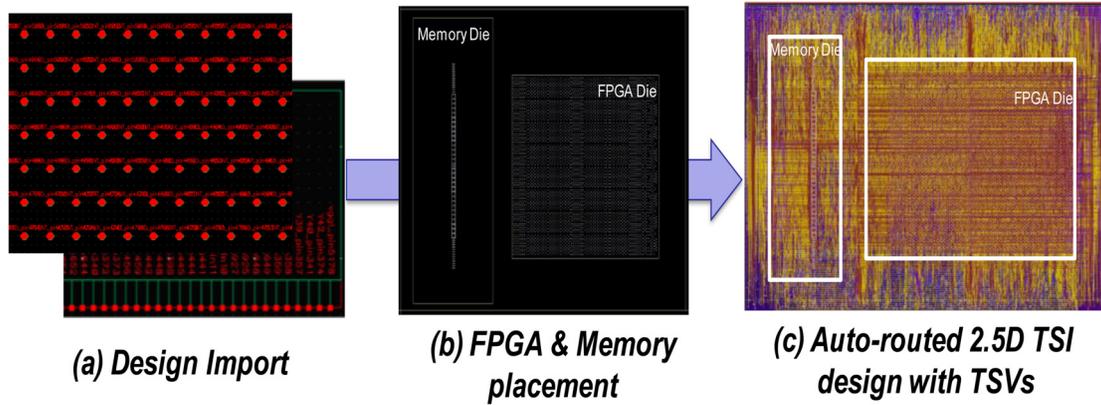
FIG. 98. From Netlist entry to auto routed design with TSVs. (a) Design import, (b) FPGA and memory placement, and (c) auto-routed 2.5D TSI design with TSVs.
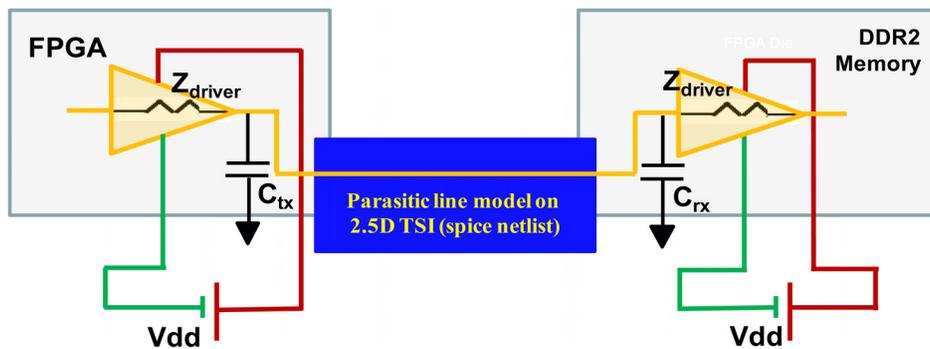
FIG. 99. Schematic to simulate the SI of a line in 2.5D TSI.

(a) $C_{tx} = 0.5$ Data rate = 0.26   **(b) $C_{tx} = 0.5$ Data rate = 1.06**   **(c) $C_{tx} = 0.5$ Data rate = 2.1**
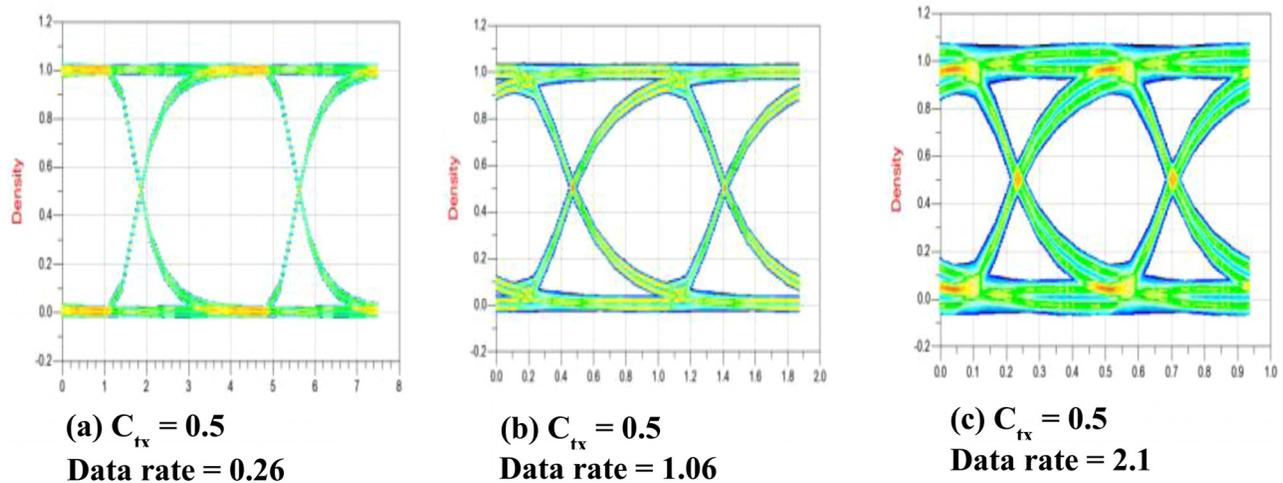
FIG. 100. Eye diagram simulations for various data rates and driver impedances (0.26 GT/s–2.1 GT/s). (a) $C_{tx} = 0.5$ data rate = 0.26, (b) $C_{tx} = 0.5$ data rate = 1.06, and (c) $C_{tx} = 0.5$ data rate = 2.1.

TABLE X. Eye diagram simulation results analysis for FPGA-DRAM interconnect lines at various data rates/frequencies.

Z_{driver}; bit rate @ $V_{dd} = 1$ V	C_{tx}/C_{rx} (pF)	Eye height (% V_{dd})	Eye width (%)	Jitter (%)
(a) 50Ω; @0.26 GT/s	0.5/2	91	99	1
(b) 20Ω; @1.06 GT/s	0.5/2	68	96	4
(c) 10Ω; @2.12 GT/s	0.5/0.5	59	91	9
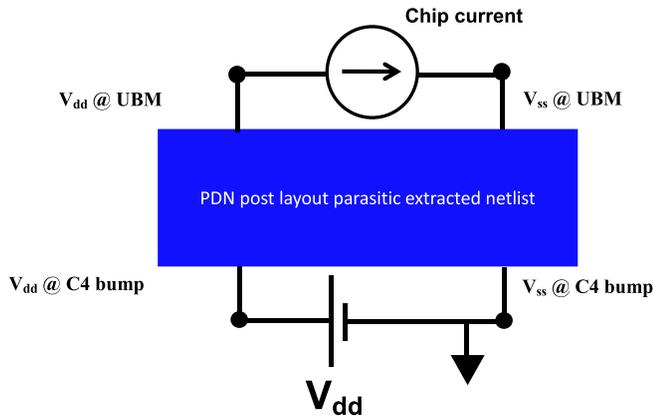
FIG. 101. Schematic for static IR Drop analysis.
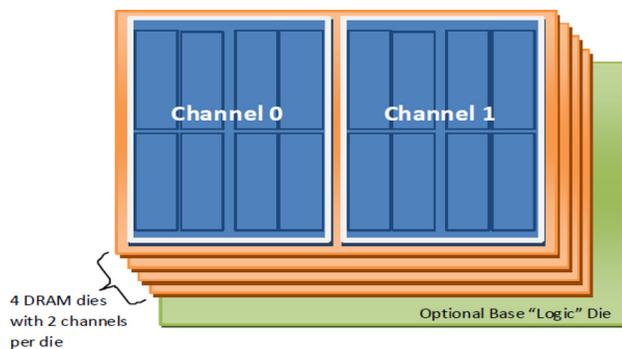
FIG. 102. Schematic diagram of an 8-channel high bandwidth memory.[14]

lower power compared to its earlier generations, and (c) high performance supercomputers. As with a technology, that is in its early adoption phase, 2.5D TSI has challenges which the industry and R&D community needs to address. These challenges stem mainly from the cost of transitioning from a well established semiconductor IC manufacturing flow to allow for designing, fabricating, and assembling 2.5D ICs on the TSI platform. With rising amounts of internet data traffic that needs to be handled, over the next decade, 2.5D TSI technology will gradually gain market adoption.

B. Application roadmap

Over the next 5 years, state of the art GPU, FPGA, and data centers applications will drive the density of electrical interconnects on TSI. In 5–10 years, high-end data centers and high performance computing applications will drive the adoption of optical interconnects on 2.5D TSI platform. This was depicted in Figures 6 and 7. Availability of HBM[14] (see Fig. 102) DRAM devices will drive the adoption of high density electrical interconnects on TSI. Such high density electrical interconnects will drive the use of multiple HBM devices that can be stacked around a GPU device[141] as shown in Figure 103. The figure indicates the increasing processing capability that can be supported by a GPU that uses 2.5D TSI technology.

With increasing volume of data traffic in servers and data centers, optical interconnects become a critical element in a Data center. A typical data center consists of servers that receive data, switches that route the data, and storage systems that keep data in storage (for example, emails, video, photographs, etc.). In such cases, multiple channels each with data-rates of 100 Gbps will be needed between racks across the data center (over interconnects that are between 10 m and 300 m). Continuing to use Cu interconnects will drive up power consumption in data centers. In such cases, optical fibers will need to pipe data to and from logic ICs. Around 5–10 years out, this will drive extensive adoption of electronic photonic integrated circuits which bring the ability to convert high-speed SERDES electrical signals into optical signals inside the rack-unit lowering power consumption significantly.

IX. FUTURE OUTLOOK/CONCLUSIONS

A. 2.5D TSI technology roadmap

The next generation VLSI applications project the number of transistors double every 18 months (Ref. 2) and I/Os also increase in tandem as per Rent's rule.[4] As these next generation chips are mounted on the interposer, the wiring density and infrastructure demands increase as well. The key
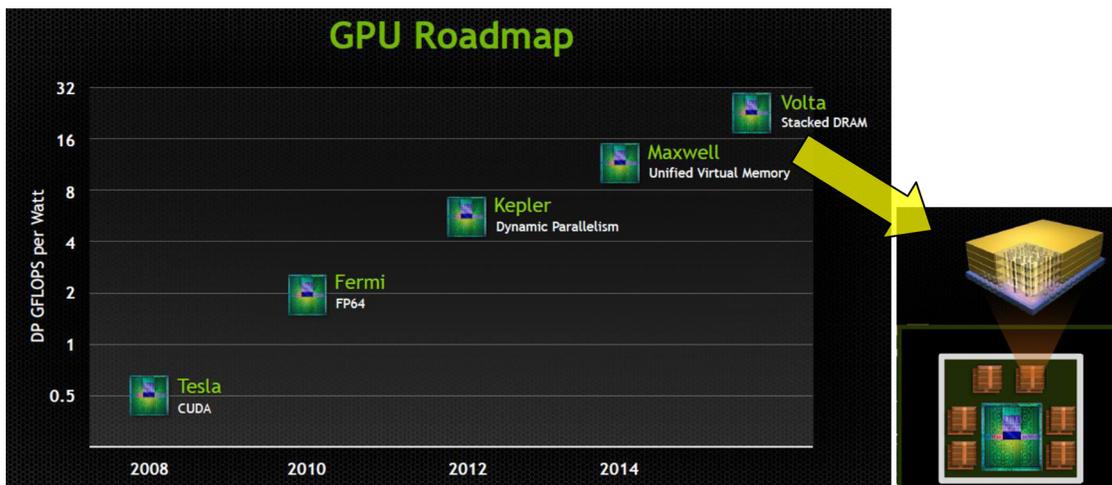
FIG. 103. Graphics processing unit (GPU) roadmap from Nvidia.[141] Reproduced with permission from *J.-H. Huang*, "Connecting people with ideas," paper presented at GPU Technology Conference, Nvidia, 2013. Copyright 2013 Nvidia Corporation.

Frontside microbump Pitch (Solder ubump) in um						
50um		20um		10um		
Front side microbump Pitch (Thermo-compression) in um						
20um		10um		5um		
Backside microbump Pitch						
300um		250um		200 um		
TSV (diameter/depth) in um						
10um/100um 5um/50um		3um/40um		2um/20um		
Cu RDL (L/S) in um						
L/S=3um/3um; 3 ML	L/S=2um/2um; 3 ML	L/S=1um/1um; 4 ML	L/S=0.8um/0.8 um; 4 ML	L/S=0.5um/0.5 um; 5 ML		
Applications (Heterogeneous)						
Large size 2.5D TSI	Optical TSV on TSI Active 2.5D TSI	Polymer Waveguide on TSI	Photonic Integration	Electro-photonic Integration	Si Photonics on TSI	Line-card-on-a-chip
2014	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**

FIG. 104. Roadmap for different components of 2.5D TSI technology.

technology components, such as micro-bumps, Cu-RDL and dual damascene BEOL line width and pitches, via and enclosure sizes, TSV, back side micro-bump, and size of the interposer, need to be scaled concurrently. In sync with the ITRS roadmap,[3] the proposed TSI component technology road map detailing the time lines for component scaling is illustrated in Figure 104.

Contemporary TSVs with $10 \, \mu m$ diameter and $100 \, \mu m$ height in 2.5D TSI are projected to be scaled to $2 \, \mu m$ diameter and $20 \, \mu 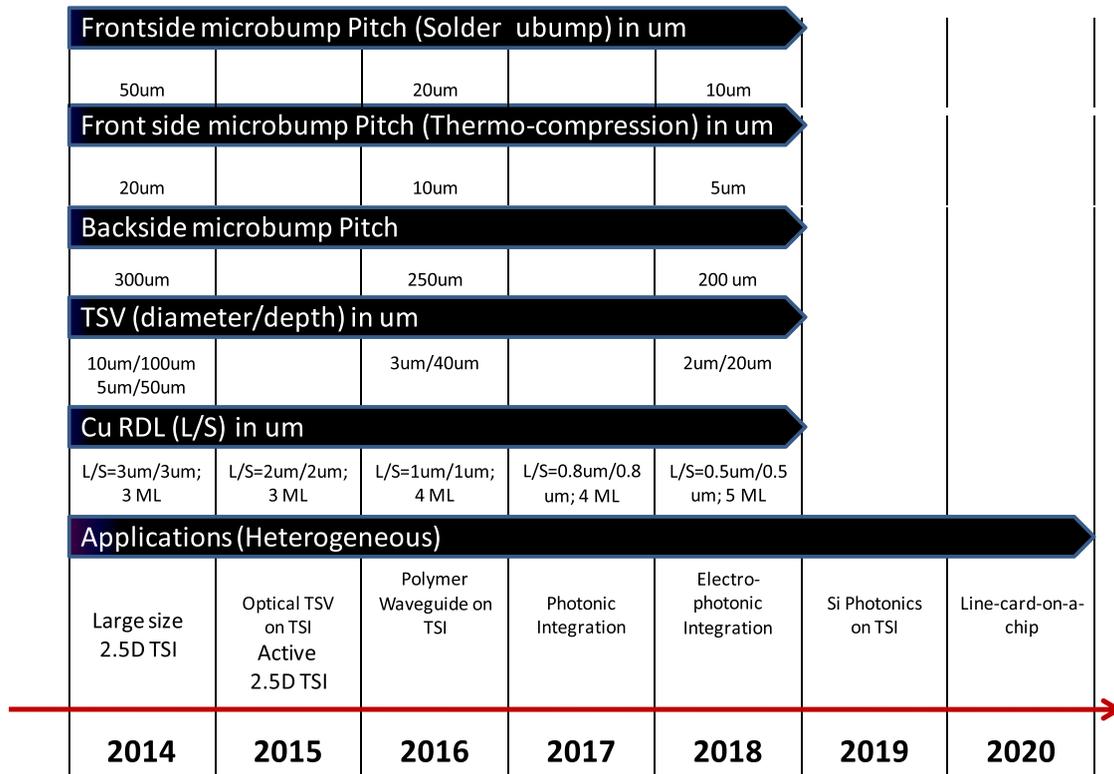m$ height in the future. The technology scaling imposes challenges to etch and fill small diameter high aspect ratio TSVs as well as to handle the thin wafer processing.[142,143] While the sub-micrometer Cu-damascene BEOL interconnects already exist, the emerging polymer based Cu-RDL[9] approach provides an alternate low cost outsourced semiconductor assembly and test (OSAT) based manufacturing approach. The existing dimensions of $3 \, \mu m$ width and $6 \, \mu m$ pitch with 3 metal layers stack are projected to be scaled to $0.5 \, \mu m$ width, $1 \, \mu m$ pitch, and 4–5 metal layers stacks on interposers by 2018. As via could form a bottle neck for potential routing, existing $7 \, \mu m$ via sizes and $12 \times 12 \, \mu m$ enclosures in Cu-RDL technology is recommended to be scaled to $3 \, \mu m$ via size and $5 \times 5 \, \mu m$ enclosure or finer. Front side micro-bumps are usually staggered with $25 \, \mu m$ size and $50 \, \mu m$ pitch should progressively scale to $15 \, \mu m$ size and $30 \, \mu m$ pitch while the back side micro-bumps forming a $150 \, \mu m$ diameter and $300 \, \mu m$ pitch arranged in as a full array are likely to scale to $100 \, \mu m$ diameter with $200 \, \mu m$ pitch. The area of the interposers is expected to be as large as $40 \times 40 \, \mu m$ with $50 \, \mu m$ thickness Si wafer to accommodate large size 2.5D system designs.

The warpage as well as reliability challenges[144] associated with building up the large size thin 2.5D TSI should be confronted as well.

Collectively, there are numerous challenges in manufacturing next generation 2.5D TSI. Few of them include correct bonding technology and materials, method of reducing TSV related stress, under-fill materials and method of application, as well as process reliability and yield. Increase of interconnect density requires a concomitant decrease of TSV diameter, increase of aspect ratio, and several layers of BEOL/RDLs. Thinning Si wafer in order to reduce TSV aspect ratio has reached to its limits at around $20 \, \mu m$ upon consideration of wafer or chip handling viewpoints. Also, the effect of mechanical stress and crystal damage is found to be enhanced when the Si thickness is reduced to below $20 \, \mu m$.[145] Possible causes include wafer thinning that introduces crystal damages, various films deposited on Si that introduces stress, and CTE mismatch between bonding agents and Si as the bonding is performed at higher temperatures. This imposes new requirements in finding improved process flows in making TSV, particularly with aspect ratio exceeding 10. Development of highly conformal etching and stress-free thin film deposition requirements in making high density TSV interconnects is mandated as well.

1. Solder technology

Conventionally, stacking one chip on the other is carried out using solder based bonding. With the trend of scaling down of interconnect pitches, the solder based bonding evolved from reflow BGA to thermo-compression Cu pillars with solder. Use of Cu pillar with solder with thermo-
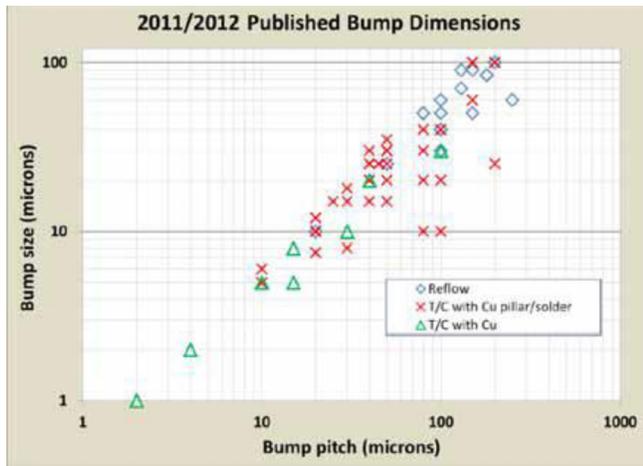
FIG. 105. Chip stacking bump sizes and pitches.[146] Reproduced with permission from Bersch *et al.*, "Cu-Cu direct bonding for ultra-high density chip-to-chip interconnects," in *Chip Scale Review Magazine*, Jul/Aug 2013, p. 20. Copyright 2013 Chip Scale Review.

compression bonding is found to have a limit with the scaling down of interconnect pitch below 20 μm. Melting solder under force tends to squeeze out and bridge with neighboring interconnects, causing reliability issues. This shows the limit of solder-assisted chip stacking and paves the way for metal-metal diffusion bonding. The trend of chip stacking methods is summarized in Figure 105.[146]

There are numerous publications targeting to extend the solder-assisted chip stacking such as the development of bump-less technology and low-temperature eutectic bonding.[147–149] The work carried out by Lin *et al.*, wherein solder paste reflow or electroplated Cu is applied with fan-out configuration for Comic-Con International (CCI). However, this approach is more focused on low-cost manufacturing process than scaling down of the interconnect pitch.[148]

Generally, Cu pillars come with few microns solder layer for thermo compression bonding. The advantage of thick solder layer is that it absorbs any height variation of Cu pillars during thermo compression bonding. Minimizing solder thickness can prevent inter-bridging of interconnect. With the thinning of solder layer, the height uniformity of Cu pillar has to be improved as thin solder layer cannot absorb any height variation. Surface planarization before solder deposition can meet this requirement. From technology point of view, this method extends the applicability of Cu pillar for further scaling down to 10 μm or below. However, from fabrication point of view, it adds additional processing steps leading to higher manufacturing cost.

The industry has already completed the transition from solder reflow to thermal compression bonding (TCB) with solder, which is usually referred as TC with Cu pillars. Transition from Cu pillar to direct Cu-Cu bonding without solder is evident but there are many technical hurdles before realizing a commercially viable solution. This is expected to take place with 5 μm Cu pillar at about 10 μm pitch. The timeline and pitch limit for the actual transition in high volume manufacturing is hard to predict as it depends on many factors such as infrastructure, cost, reliability, and most importantly application drivers.

2. Metal-metal bonding

The transition from solder based thermos-compression bonding to solder-less metal-metal diffusion bonding is essential in realizing high density micro-bumps. To date, Au-Au and Cu-Cu are the most studied metals for chip stacking with metal diffusion bonding.[150,151] Gold has no surface oxide thus eliminate surface cleaning issues before bonding. Conversely, Cu is more susceptible for surface oxidation and requires additional processing steps for surface cleaning.

There are many work reported on Cu-Cu diffusion bonding for CCI at various conditions.[151–153] Cu-Cu bonding essentially comes with Cu pillars with diameter smaller than 10 μm and aspect ratio below 1. Cu can get deformed during bonding and absorbs minute changes in height variations. Nevertheless, as the overall height is below 10 μm, there is no room to absorb higher height variation particularly of that generated during Cu electroplating. This can result in cold or un-bonded joints. Thus, surface planarization before bonding becomes an essential step. There are two methods for surface planarization of Cu pillars, namely, CMP and bit grinding. CMP yields smoother surface with surface roughness below 1 nm although the operation cost is relatively higher. Bit grinding technology provides low cost approach for surface planarization but needs to trade off in terms of greater surface roughness. Under the optimized conditions, surface roughness can be as low as 15 nm. This surface roughness gets easily deformed under the bonding force, thus it does not pose a challenge for Cu-Cu bonding.

Normally, there is a thin layer of Cu oxide on the Cu surface. The brittle oxide layer breaks down during diffusion bonding under applied bonding force and creates diffusion centers wherein Cu atoms mutually diffuse into the other side of the Cu pillar. The oxide layer is a barrier for the diffusion and retards the diffusion rate. To overcome this drawback, Cu-Cu bonding is usually carried out at higher temperature, usually over 350 °C providing adequate thermal energy for diffusing Cu atoms.

Removal of surface oxide before Cu-Cu bonding can lower the bonding temperature even below 200 °C. There are several methods in removing surface oxides such as (i) use of H_2 at 350 °C or over, (ii) use of H_2 plasma at low temperature ($<$100 C), (iii) Ar sputter cleaning, (iv) use of formic acid gas, and (v) wet etching. Hydrogen plasma and the formic acid gas treatment are by far the most used techniques to date in removing Cu oxide.

Surface planarization before Cu-Cu bonding is found to have two advantages.[152] First, owing to the uniform Cu pillar height bonding, reliability is improved. Second, during the planarization process using bit grinding, the Cu surface approaches more amorphous-like structure.[152] Thickness of amorphous-like layer is observed to be over 100 nm. Electroplated Cu usually comprises Cu grains and this further recrystallizes after thermal annealing at or over 200 °C, which is a normal practice to harden the Cu to prevent electro-migration. Cu diffusion during Cu-Cu diffusion bonding occurs through grain bounders or through damaged grain surfaces. Use of electroplated and thermally annealed Cu yields smaller effective surface area for diffusion

bonding. Generation of amorphous-like layer after bit-grinding is therefore a beneficial feature to increase the effective diffusion surface area. Moreover, this feature also assists in reducing the bonding temperature even below 200 °C. It has been observed that the amorphous-like Cu layer generated during surface planarization is only created by bit grinding process. The CMP process does not yield such an amorphous like structure.

As-deposited Cu begins to recrystallize at 200 °C or over.[143] Some work has observed that the recrystallization process can initiate even at 180 °C.[142] Accordingly, the amorphous-like Cu layer can again recrystallize during surface de-oxidation step if the de-oxidation is performed at a temperature above 180 °C. Recrystallization negates the advantage of generating diffusion-friendly amorphous-like layer. The surface de-oxidation with H_2 plasma is usually carried out at low temperature, for example, at room temperature. The wafer gets heated slightly only by the plasma, which does not exceed over 50 °C. Therefore, there will be no effect on amorphous-like layer with this de-oxidation method. The surface de-oxidation with formic acid gas begins at around 150 °C but is most effective at 200 °C. However, in order to prevent Cu recrystallization, formic acid treatment has to be carried out below 180 °C.

The decision to port an application to a particular technology depends on the routing ability requirements and SI/PI demands of the design. The designs with large number of I/Os exhibiting larger signal and power routing requirements would prefer fine Cu-Damascene BEOL routing to meet the routing requirements. Polymer based Cu-RDL technology, offering coarse pitch although provides better SI performance and enhanced data rate per wire compared to Cu-damascene technology, is better suited for designs where their routing requirements are satisfied.

As contemporary 2.5D TSI does not have any active elements on Si, it is prudent and certainly economical to utilize the Si real estate for 2.5D system design. A potential 2.5D system schematic illustrating the memory and App processor integration on TSI is shown in Figure 106. Peripheral blocks, such as I/O, electrostatic discharge (ESD) protection, power management, RF and analog components, and IPD, can be housed in the Si substrate of active 2.5D TSI.[154–158] Integrated Voltage Regulators (IVRs) can be used for improved power integrity while active transistors in TSI's Si substrate can be used for repeater insertion to build inter-block optimized interconnects. TSVs built using Via-last technology are preferred for active interposers as the active devices can be manufactured in the foundry end and the wafers can be passed to OSATs or other lower cost

packaging houses for TSV manufacturing and assembly. The impact of TSV-last[146] technology on the transistor performance[147,148] should be evaluated as well.

Moreover, as 2.5D TSI technology would be catering to sensor as well as optical technologies co-existing with 2.5D electrical systems, the process integration schemes to accomplish such integration will be developed. Process flows integrating optical TSVs as well as polymer based waveguides to 2.5D TSV and Cu-damascene and RDL integration flow will be developed. The infrastructure to analyze and design the opto-electrical as well as the electro-mechanical systems would be developed in parallel too.

While development and integration of new technologies on 2.5D TSI technology platform is an enabler to port new applications on 2.5D TSI, identifying the ownership of individual component makers is crucial for the success of steering 2.5D TSI technology to manufacturing mainstream. The testing and debugging methods to evaluate the components and process at every stage are likely to play a very important role. Ultimately, the 2.5D TSI is envisioned to be treated as a well-tested package before the expensive and off-the-shelf guest dies and components are mounted on it though an assembly and package flow.

B. 2.5D/3D EDA outlook

Although we have been able to design the 2.5D IC designs using the existing industry standard 2D IC design tools, it would be extremely useful to have dedicated 3D design tools for the technology path finding as well as design planning. There are industry standard 3D IC tools made available from Cadence[135,159] and Synopsys.[134] However, designers face the following shortcomings while employing them for 2.5D/3D IC sign-offs.

1. Inability of existing 3D EDA tools to analyze unified 3D netlist

Analysis of the 2.5D/3D power and clock distribution schemes is an important design component for 2.5D and 3D ICs. The 3D EDA tools unfortunately, do not allow the analysis of unified 3D netlist as it deals with the netlist on each stack of 3D IC individually. It would be beneficial to have a 3D design environment that is able to analyze unified 3D netlist. Moreover, it would enable automatic Clock Tree Synthesis (CTS), repeater insertion, etc., towards building a reliable 3D IC tape out. The infrastructure can then be leveraged to build the methodologies to formulate the 2.5D/3D clock and power distribution networks benefitting the 2.5D/3D system performance.
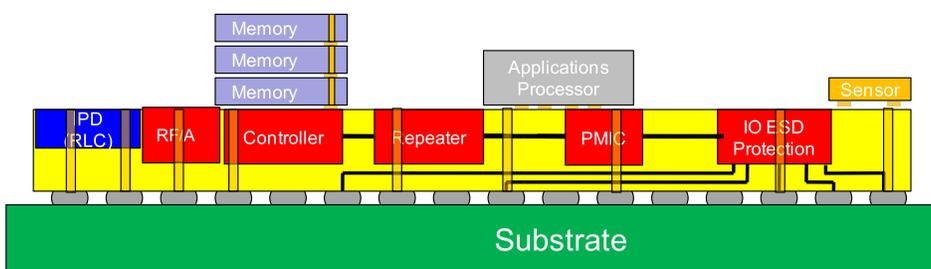

FIG. 106. Different design components on 2.5D active interposer—A schematic.

2. Employing calibrated TSV lumped "RC" model

The EDA tools support the BEOL via resistance to be specified in technology files detailing the interconnect layer descriptions. However, specifying via capacitance is not permitted in the technology description format. In case of TSV, as a part of 2.5D and 3D circuit, the TSV capacitance is the most dominant electrical parameter[95] and hence it cannot be ignored. The present 2.5D and 3D tools do not allow an easier way to consider the TSV capacitance. This inhibits comprehensive 2.5D/3D circuit and system analysis. The EDA tools enabling the incorporation of TSV/via capacitance in the technology description format would aid in the analysis of complex 2.5D/3D systems and is desirable. An alternate way to consider TSV capacitance is to treat TSV as a three-terminal device instead of via. While TSV implemented as a device can be used to analyze small 2.5D and 3D circuit paths, the same methodology becomes slower for analyzing and back-annotating larger circuit blocks ($>$1000 gates).

X. SUMMARY

In this paper, we outline the advantages of implementing 2.5D ICs on TSI along with the key focus areas in implementing TSI technology. In addition, we highlight the solutions to surmountable challenges faced by this technology on its path to high volume adoption in mobile devices and servers/data centers. Logic and memory VLSI systems are the first and foremost applications that are ideally suited for steadfast 2.5D TSI implementations. Fabrication flow illustrating the TSV module development and its integration with the BEOL and/or RDL technology are presented in addition to various plausible assembly schemes and challenges. Electrical test characterization structures for technology characterization as well as PDK model development are described along with the EDA flow leveraging existing industry standard 2D IC tools to design, verify, and manufacture 2.5D ICs. Thermal modeling and simulations to alleviate the heat dissipation providing adequate cooling are analyzed for 2.5D TSI systems. FEM based thermo-mechanical analysis of the 2.5D TSI technology to address the manufacturability, warpage, and solder reliability challenges are performed as well. A suggested roadmap of individual 2.5D TSI components is presented so that the 2.5D TSI technology can potentially cater to numerous VLSI applications. For volume adoption of 2.5D TSI technology, the industry needs to focus on providing an end-to-end manufacturing platform for seamless integration of PDK, design, fabrication, test, and assembly of 2.5D system on TSI. This will enable high performance, low power designs at reduced design and manufacturing costs, as well as drive start-ups, fab-less design houses, integrated device manufacturers (IDM), OSATs, and foundries to design and manufacture 2.5D TSI products that meet/exceed market expectations.

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